

Broadband Small Signal Amplifier MMIC

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Abstract

This report describes the design, simulations and layout for a five stage GaAs MMIC distributed amplifier. The amplifier is designed to be operated from 2.305 to 5.875 GHz while limiting the gain ripple to less than ± 0.5 dB. The broadband small signal amplifier design is a project for the MMIC Design (EE525.787) Fall 2007 class. The TriQuint process is utilized for this design. Each stage of the amplifier utilizes an enhanced pHEMT device.

Introduction

Broadband performance for amplifiers is desired for small signal amplifiers (SSA), low noise amplifiers (LNA) and power amplifiers (PA). The goal in each case is to produce the desired performance over the greatest bandwidth possible. This report presents a broadband SSA design approach. Two different designs were investigated; the first is a five stage distributed amplifier and the second is a two stage feedback amplifier. Only the distributed amplifier will be presented in this report.

The SSA described here is to operate over a bandwidth of 3.575 GHz while meeting the performance specifications listed in table 1 (page 3). The greatest challenge in this design is to obtain the desired performance while limiting the device power per pHEMT to 10 mW or less. The design is also limited to a single power supply. Later in this report it will be shown that amplifier size, device power and small signal gain were compromised to meet the bandwidth and gain ripple specifications.

Agilent Technologies, Advanced Design System (ADS) 2006A software was used to design, perform simulations and produce a layout for the distributed amplifier. The TriQuint Semiconductor TQPED pHEMT process was utilized for this design.

Design Approach

The design specifications for the broadband SSA are listed in table 1 (page 3). Two possible designs were considered for this project. The first was to use a cascaded feedback amplifier design. This design limits the number pHEMT devices in order to limit the power consumption of the amplifier while meeting the gain and bandwidth requirements. The other design is a distributed amplifier; distributed amplifiers have good gain-bandwidth performance. Distributed amplifiers don't have the high gain or low noise performance of other designs. However, this type of amplifier can produce similar gains over a wider bandwidth. The distributed design was chosen for this project.

Initially 60 μm (4x15) Emode pHEMT devices were used. These devices were biased at 3.3 VDS, 0.5 VGS and 3 mA IDS. In order to meet the small signal gain requirement a cascaded four stage design (8 total pHEMT devices) was used. While limiting each device to 10 mW per device the designer was unable to meet the bandwidth and gain ripple requirements. However, when the device size was increased to 300 μm

(5x20) devices it was trivial to meet all of the specifications except for device power. Specification relief was given in order to move forward on the design. The output power, small signal gain and device power requirements were lowered to best effort. Authorization was given by the instructor to use up to 60 x 90 mil ANACHIP layout.

Parameter	Specification	Goal
Frequency (MHz)	2305 – 5875	-
Bandwidth	> 3575	-
Gain small signal (dB)	> 18	22
Gain Ripple (dB)	±0.5	-
VSWR,50 Ohm	<1.5:1 input & Output	-
Supply Voltage (VDC)	3-3.6	3.3
Size	60 x 60 mil ANACHIP	-
Power (mW)	< 10 per device	-

Table 1 – Broadband small signal amplifier design specifications. The first column on the left lists the design parameter and the units of the parameter. The middle column lists minimum design specifications. The right column lists the design goals that exceed the specifications.

When designing the amplifier first ideal inductors were utilized. TQPED resistors and capacitors were utilized during the entire design process. A voltage divider network is used to provide both the drain and gate voltages from a single power supply. A large inductor is used in all of the simulations to represent a long wire from the supply to the circuit. The RF is blocked from the DC power supply by large 20 pF capacitors.

The amplifier circuit consists of six inductors on the gate line. One inductor is placed before the first pHEMT and one after the final pHEMT. An additional inductor is placed between each device. Both the drain and gate lines have the same number of inductors. The inductors on the drain line are distributed similarly to the gate line. There is an additional inductor that matches the voltage divider to the drain line of the circuit. These inductors along with the device size of each pHEMT were adjusted independently to compromise between small signal gain, bandwidth and gain ripple. Each of these components can be seen in figure 8 (page 8). Additionally, terminating resistors are used on both the gate and drain lines to minimize disruptive reflections in the circuit.

Simulation using ideal inductors produced a small signal gain performance in excess of 17 dB across the target band. Next, the TQPED inductors were substituted in the circuit for the ideal components. The Induct_fndy1.exe program was utilized to compute the number of segments and dimensions of the inductor to produce the target inductance. After the replacement of the ideal components with the TQPED comments the circuit was optimized for best performance.

The last step in the design process was to place the amplifier components into the layout. The traces of the appropriate lengths were then placed into the schematic and re-simulated. This process took several iterations to produce the final design. After adjusting the inductor dimensions the trace length were updated.

Simulations

Each of the simulation in figures 1 – 5 (pages 4-6) were performed using the amplifier design with TQPED components. Figure 1 (page 4) is a plot of the gain (S21), input match (S11) and output match (S22) verses frequency. Five markers were used to examine the gain ripple. The markers were placed at 2.3, 3, 4.8 and 5.9 GHz. The greatest difference in gain is 0.91 dB. Therefore the gain ripple is less than ± 0.5 dB. Notice also that the output match is optimized for 4.1 GHz with a match of greater than 35 dB. The input match is greater than 15 dB for the entire bandwidth of interest. Also, the amplifier has a gain and ripple that is consistent down to approximately 1 GHz. A bandwidth of over 4.5 GHz has been achieved. However, the minimum small signal gain specification was missed by almost 3 dB at 5.875 GHz and 2 dB at 4 GHz.

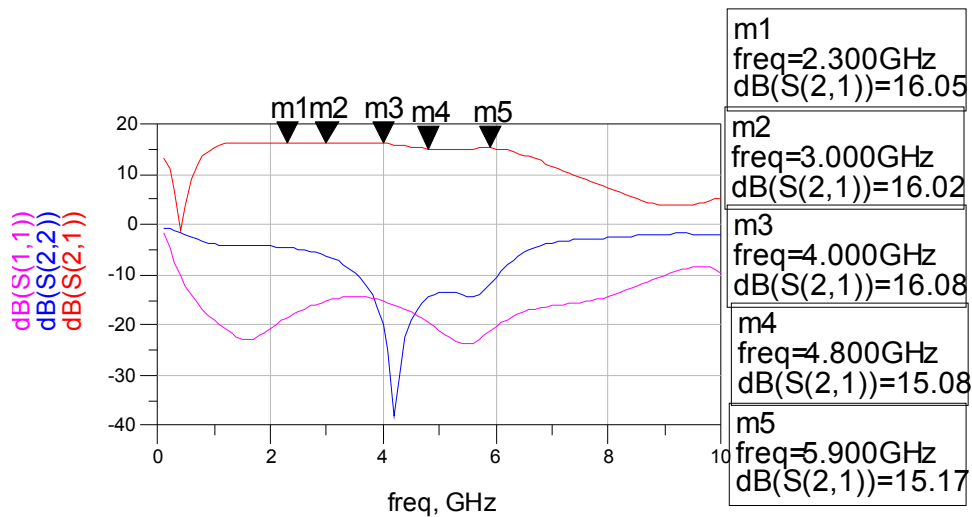


Figure 1 – Small signal gain plot. The Gain (S21), and input match (S11) and output match (S22) plotted verses frequency. The simulation was performed from 100 MHz to 10 GHz.

Figure 2 (page 5) contains plots of the noise figure (top left), input and output matches and stability (top right), VSWR (bottom left) and stability verses frequency. The simulation was performed from 100 MHz to 10 GHz. The noise figure at each band edge is approximately 3.5 dB. The minimum noise figure is found at 4 GHz to be approximately 1.6 dB. The VSWR between 4 and 5 GHz exceeds the design specifications. Both the input and output VSWR are less than 1.5. The VSWR performance below 4 GHz and above 5 GHz are both outside of the specified levels.

Each gradually increases to levels approaching 5 at the band edges. Both stability plots indicate that the circuit will be stable between 100 MHz and 10 GHz.

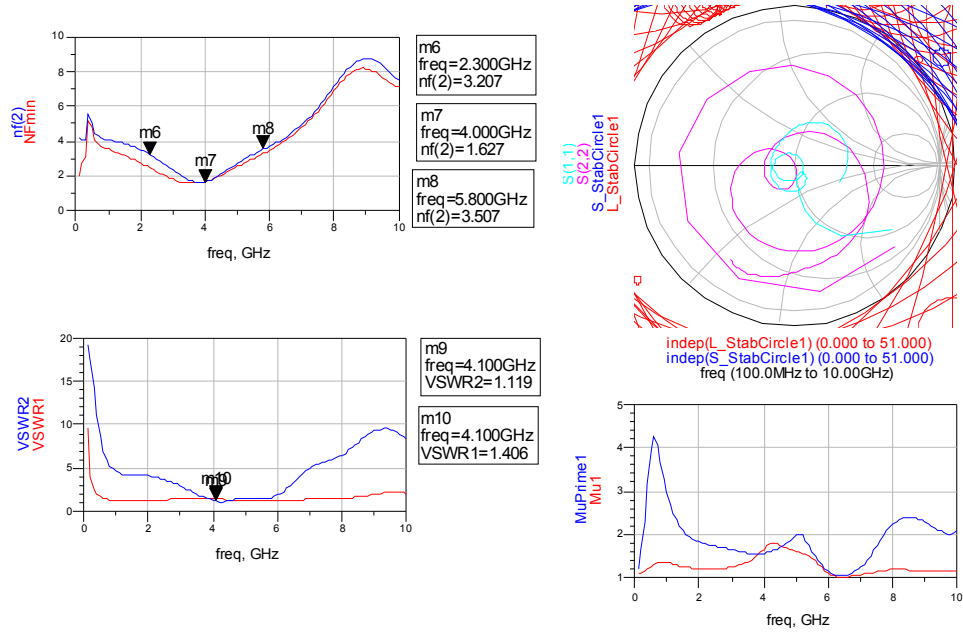


Figure 2 – Noise figure versus frequency (top left), input and output match and stability (top right), VSWR versus frequency (bottom left) and input and output stability versus frequency (bottom right). Each of these simulations were performed from 100 MHz to 10 GHz.

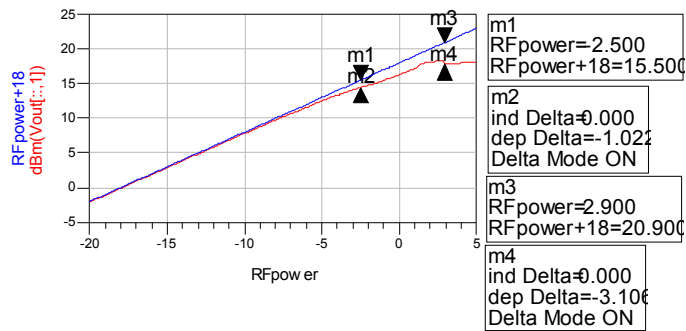


Figure 3 – Plot of input power (dBm) versus output power at 2305 MHz. The 1 dB compression point is at markers 1 and 2. The 3 dB compression points are at markers 3 and 4.

Figures 3-5 (pages 5, 6) are plots of the input output power verses input power at 2.305, 4.09 and 5.875 GHz. In each of the three plots the 1 dB and 3 dB compression points are marked. In figure 4 the 1 dB compression point is at -2.5 dBm of input power. The 3 dB compression point is at 2.9 dBm of input power. In figure 4 the 1 and 3 dB compression points are at 0.9 and 4.8 dBm of input power respectively. In figure 5 the 1 and 3 dB compression points are at -3.9 and 3.7 dBm of input power respectively. The data indicates that the greatest input power at the 1 and 3 dB compression point is achieved at the center frequency. In both figures 3 and 4 the simulations appears to break down at approximately 2 dB of input power. In figure 5 the simulation appears to behave as anticipated.

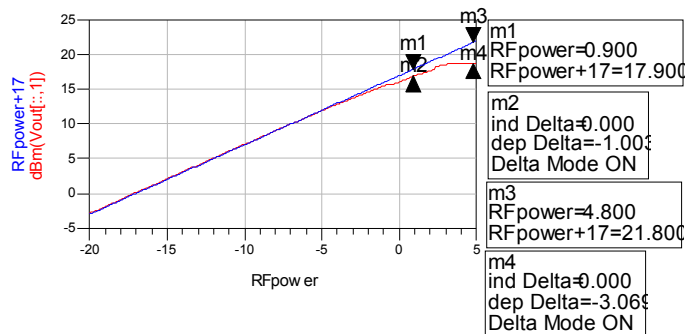


Figure 4 – Plot of input power (dBm) verses output power at 4090 MHz. The 1 dB compression point is at markers 1 and 2. The 3 dB compression points are at markers 3 and 4.

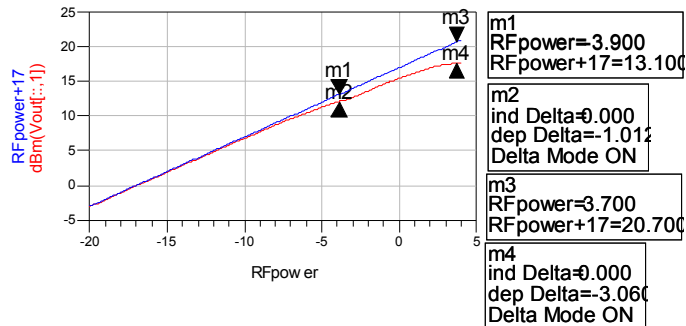


Figure 5 – Plot of input power (dBm) verses output power at 5875 MHz. The 1 dB compression point is at markers 1 and 2. The 3 dB compression points are at markers 3 and 4.

DC Analysis

The amplifier is supplied with a single 3.3 VDC external power supply. A voltage divider is used to reduce the input voltage to 0.6 VDC. This voltage is used to bias the gates of the enhanced devices. The first device has 3.27 VDC applied to the drain of the device. The voltage is reduced with each device. At the fifth device the drain voltage is 3.21 VDC. Bitmaps of the drain (left) and gate (right) voltages are in figure 6 (page 7).

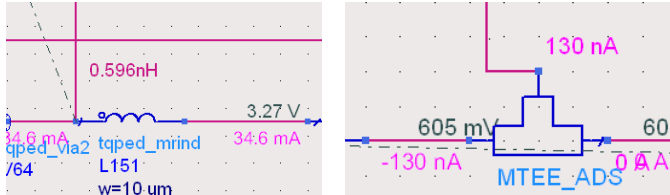


Figure 6 - Drain Input (left), Gate Input (right)

Figure 7 (page 7) displays the DC analysis of the five devices that are used in the amplifier. The devices are displayed in the order that they are used in the circuit. The device that is closest to the input is located on the left in the figure. The device that is closest to the output is on the right of the figure. The drain voltage and current for the five devices are tabulated in table 2 (page 7) along with the device power consumption. The total power consumption for the entire amplifier is 115.2 mW.

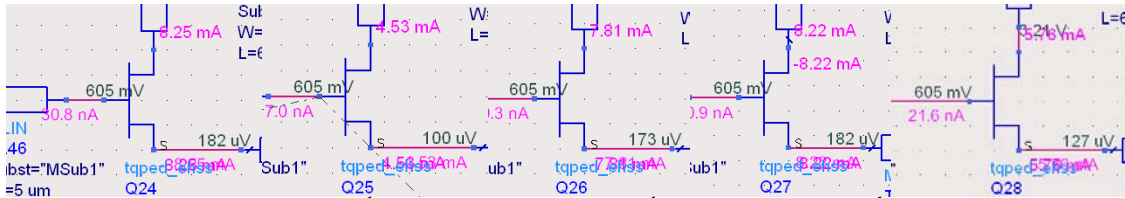


Figure 7 – 1st FET (left), 2nd FET (middle left), 3rd FET (middle), 4th FET (middle right) and 5th FET (right).

Device Number	Drain Voltage (VDC)	Drain Current (mA)	Device Power Consumption (mW)
1	3.27	8.25	27
2	3.24	4.53	14.7
3	3.22	7.81	25.1
4	3.21	8.22	26.4
5	3.21	5.76	18.5

Table 2 – Drain voltage (VDC), drain current (mA) and device power consumption (mW) for the five enhanced devices.

Schematic

This section contains schematic of the entire distributed amplifier (figure 8, page 8), RF input and voltage divider (figure 9, page 8), pHEMT devices (figures 10-12, pages 9-10) and RF output (figure 12, page 10). The DC bias voltages and current are supplied in the upper left corner of figure 8 (page 8). The RF input is supplied in the lower left corner and RF output is in the lower left corner of figure 8 (page 8).

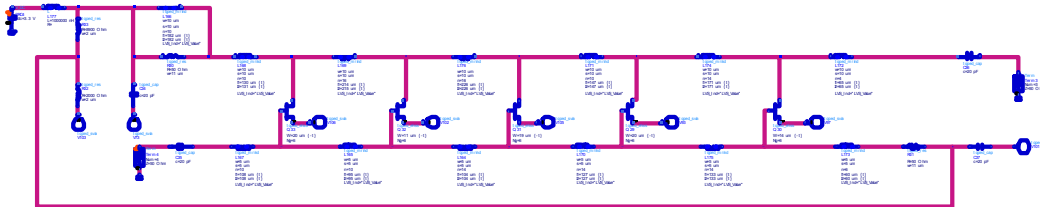


Figure 8 – Schematic for a five stage distributed amplifier. Included are voltage divider and RF input and output.

Figure 9 (page) is an expanded view of the DC distribution and RF input. The gate voltage is developed using a voltage divider. The drain voltage is supplied through the inductor L166 and terminating resistor R30.

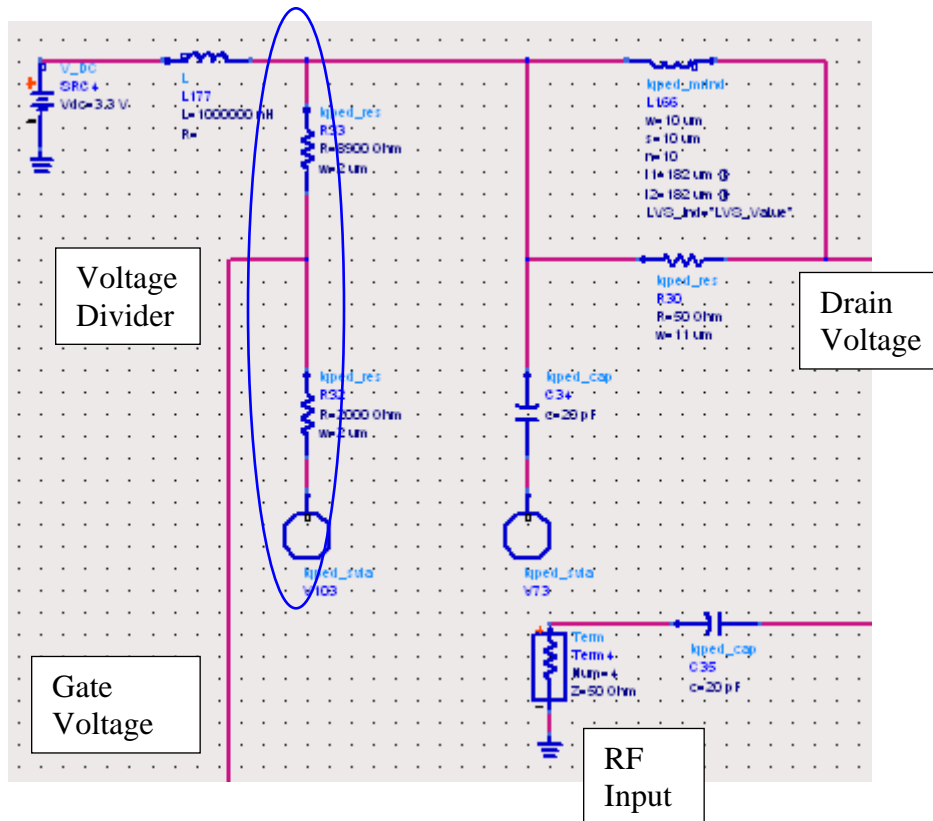


Figure 9 – DC supply and RF Input for the distributed amplifier. A voltage divider is utilized to enable single source operation.

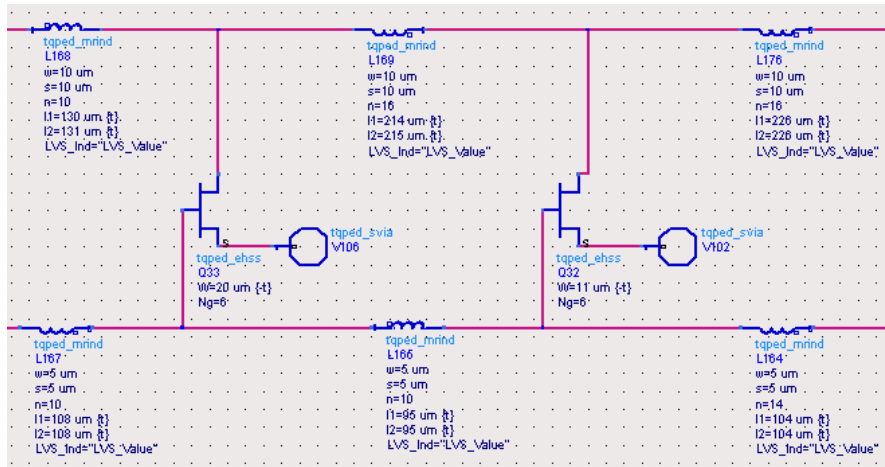


Figure 10 – First to pHEMT devices from the input.

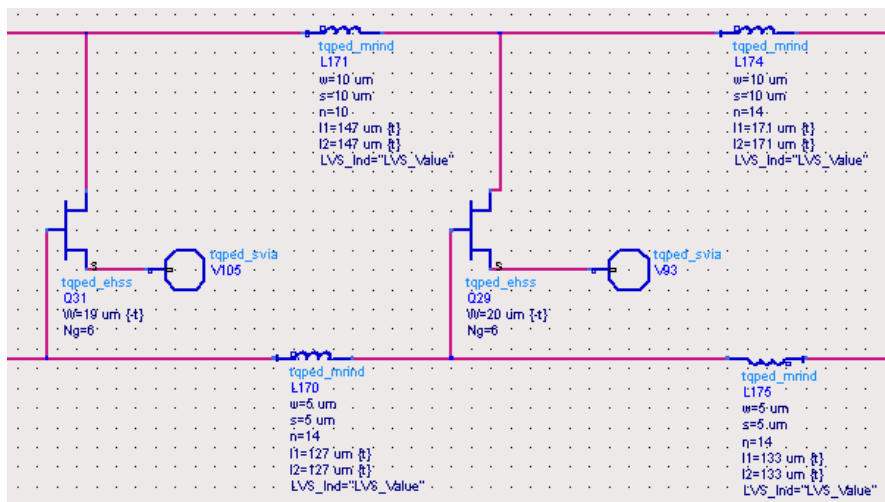


Figure 11 – 3rd and 4th pHEMT devices from the input.

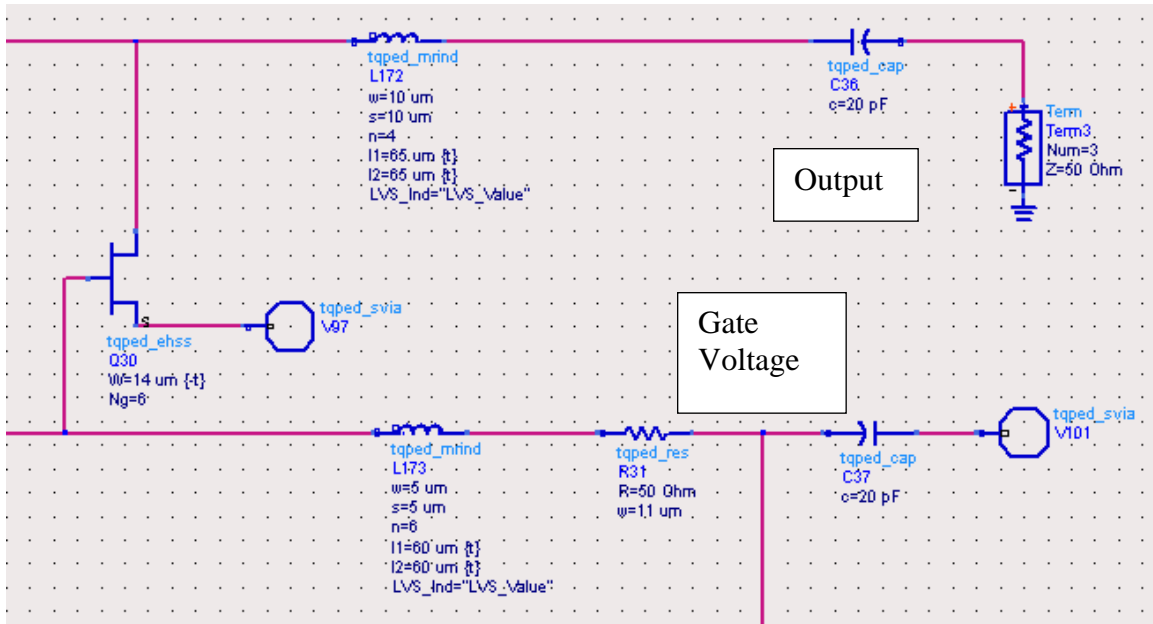


Figure 12 – Last pHEMT device with RF output and gate voltage input.

Layout

Figure 13 (page 11) is an illustration of the distributed amplifier layout. The layout occupies a 60 x 90 mil area. The RF input is located in the upper left corner of the circuit. The DC input is in the upper right corner and the RF output is in the lower right corner of the circuit. The pHEMT devices and associated inductors are placed in the layout in order from the input to the output. The voltage divider is placed across the top of the circuit.

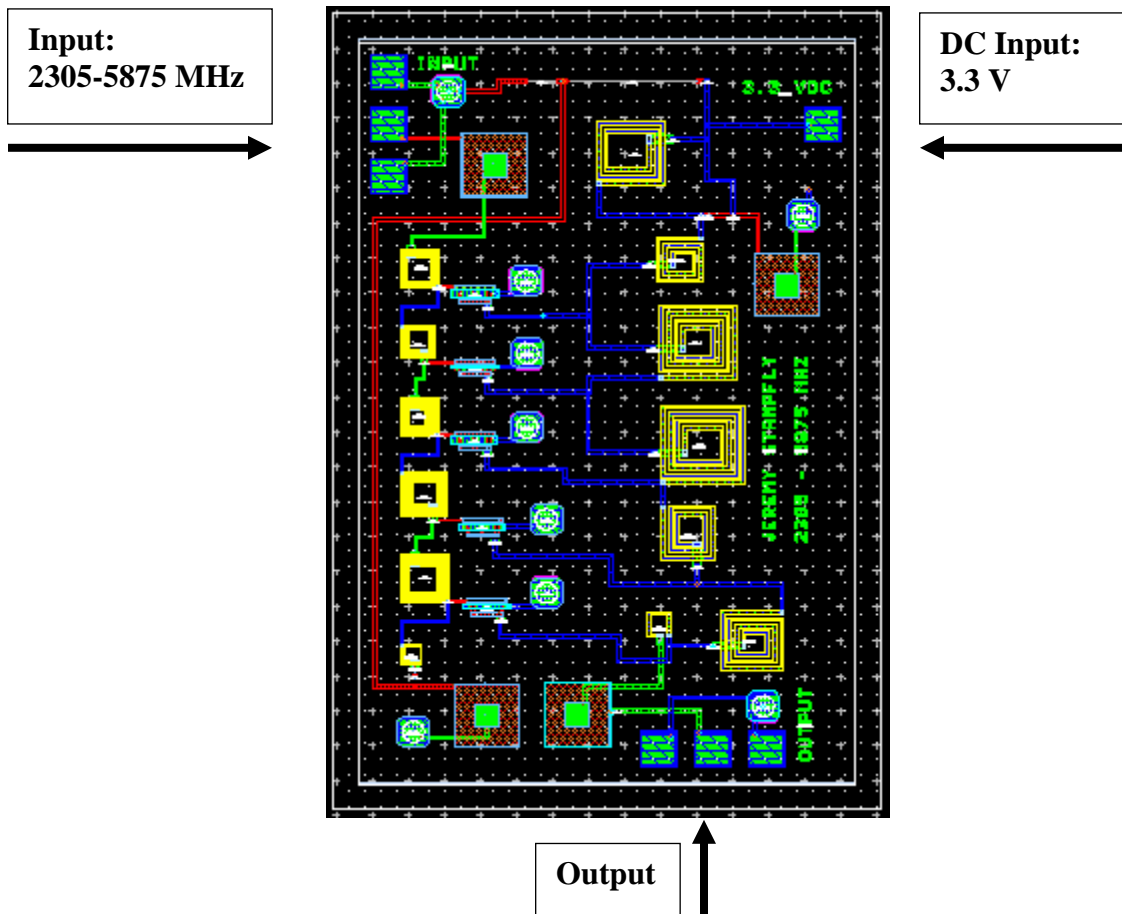


Figure 13 – Layout of the distributed amplifier. The RF input is in the upper left corner of the circuit. DC input is in the upper right corner of the circuit. RF output is lower right corner of the circuit. The circuit is designed to operate from 2.305 – 5.875 GHz.

Test Plan

1. Power up test equipment.
2. Calibrate network analyzer from 100 MHz to 10 GHz.
 - a. Calibrate using open, short, thru and load test fixtures.
 - b. Power levels are not anticipated to approach the measurement equipment limits.
3. Place circuit into the test fixture and connect RF input and output probes as shown in figure 13 (page 11).
4. Set DC supply to 3.3 V, 0 A.
5. Increase current until the circuit is drawing 34.6 mA.
6. Perform s-parameter measurements from 100 MHz to 10 GHz.
7. Connect frequency synthesizer to the input port.
8. Connect a spectrum analyzer to the output port.
9. Set frequency to 2.305 GHz and sweep the power from –20 to 5 dBm.
10. Repeat step 9 at 4.09 GHz.
11. Repeat step 9 at 5.875 GHz.

Conclusion

Distributed amplifiers have good gain-bandwidth performance. This type of amplifier is a good choice for applications where noise figure and power consumption are not critical. In this design a bandwidth of 4.5 GHz was achieved with the worst gain in that band being approximately 15.2 dB. Distributed amplifiers can be cascaded to improve the gain performance of the design. For battery operated system the distributed amplifier is not recommended.