

# **C-Band Power Amplifier MMIC**

By

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JHU MMIC Design, Fall 2007  
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## **Introduction:**

This report describes the design, simulation, and layout of a MMIC power amplifier submitted for the final class project of Johns Hopkins University's MMIC Design Course (525.787), Fall 2007. The amplifier was designed using Triquint's TQPED GaAs process. This is a C-band design operating from 5.150 GHz to 5.875 GHz. Portable wireless devices are the intended application for this design, and efficiency is of prime importance to extend device operating time. Enhancement mode devices were used facilitate the use of a single positive bias voltage. PAE is better than 20%, reaching 27% at 2 dB compression. Simulation and layout was carried out in Agilent's Advanced Design System (ADS) software. The design was laid out in a 60x60 mil area.

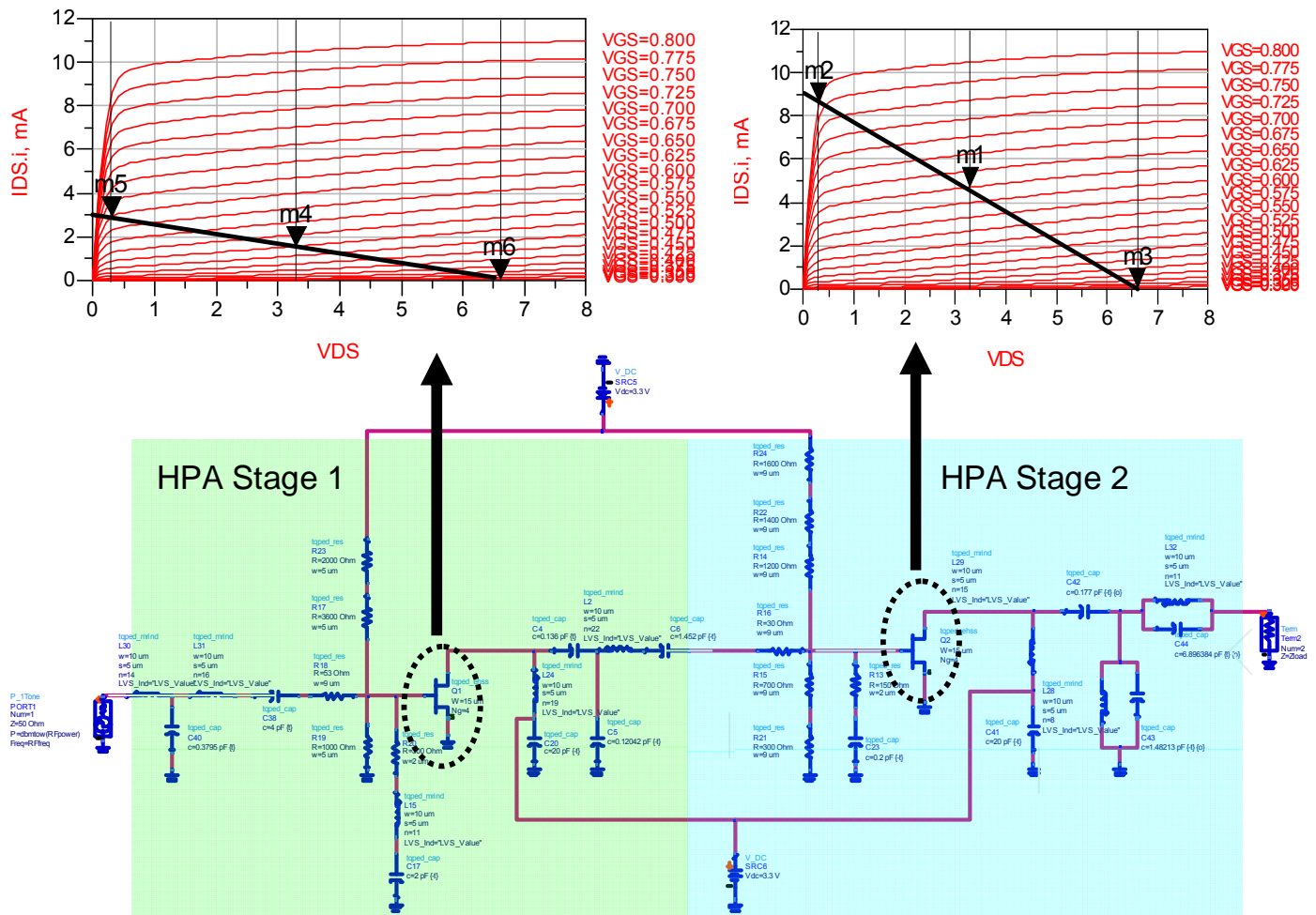
## **Design Approach:**

The requirements for this design are listed in the table below.

<b>Spec</b>	<b>Spec Value</b>	<b>Simulated</b>
Operating Band	5.150 – 5.875 GHz	N/A
Output Power	TBD	8.85 dBm
Gain	20 dB	~ 21.5 +/- 0.3 dB over band
Gain Ripple	+/- 1 dB	+/- 0.3 dB
PAE	> 20% - 25% @ 1dB compression	27% @ 2 dB compression
Input Match, 50ohms	< - 14dB, input and output	< -15 dB
Supply Voltage	+3.3 V	+3.3 V
Size	60 x 60 mil	60 x 60 mil

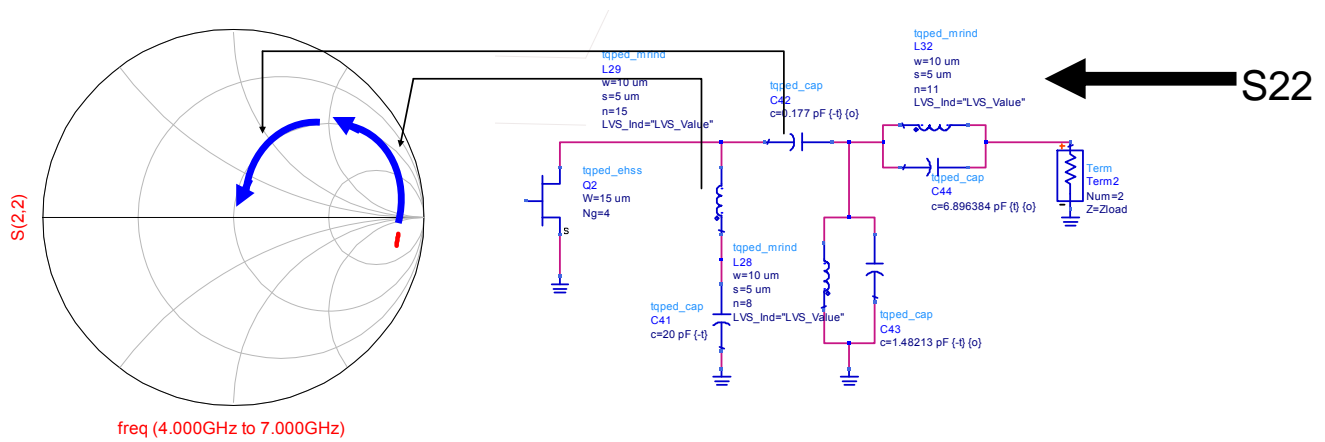
The highest priority requirement was PAE. A PAE of 20 to 25% is required at 1 dB compression. Large signal simulations predict a PAE of 23% at 1 dB compression. No lower limit was specified for output power. At 1 dB compression the design should produce XXX dBm of power. Layout of the design was restricted to a 60 by 60 mil die. Both drain and gate bias were designed to accept the same voltage, simplifying product integration by allowing the use of the same power regulation circuitry. Small signal simulation predicts 21.5 dB of gain, meeting the 20 dB requirement. Both input and output match are better than the -14 dB requirement.

It was decided to use the same periphery for the driver stage as the final stage. This was done because of concern over the accuracy of the fet model at the extreme edges physical size. To reduce power consumption of the first stage, it was biased at a lower gate voltage. The result was a device that had a peak drain current 1/3 of the 2nd stage, thereby reducing power consumption.

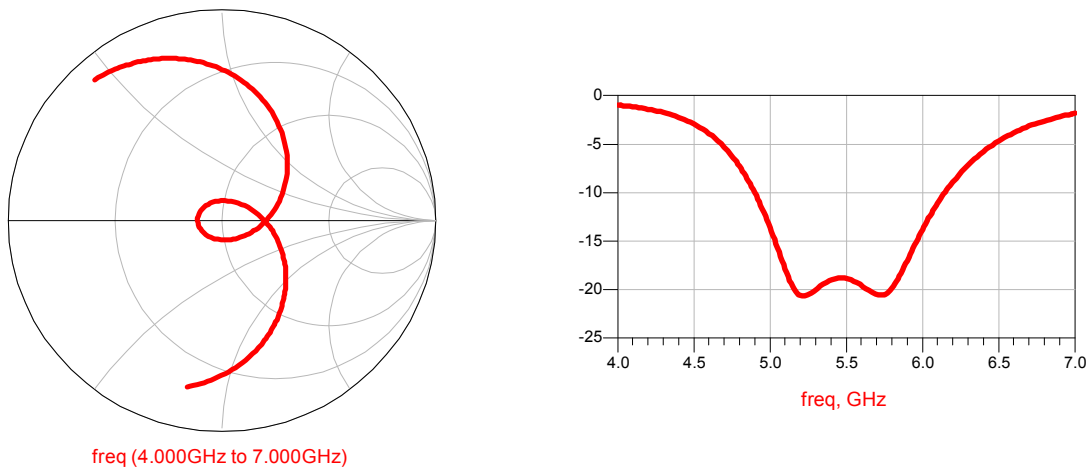


The first pass of the design employed 2 element matching networks for the output, input and interstage networks. Initial simulations showed that while the design met the requirements at the center of the band, performance quickly deteriorated toward band edges. Since the initial layout showed sufficient space to handle extra components, more elements were added to the different matching networks.

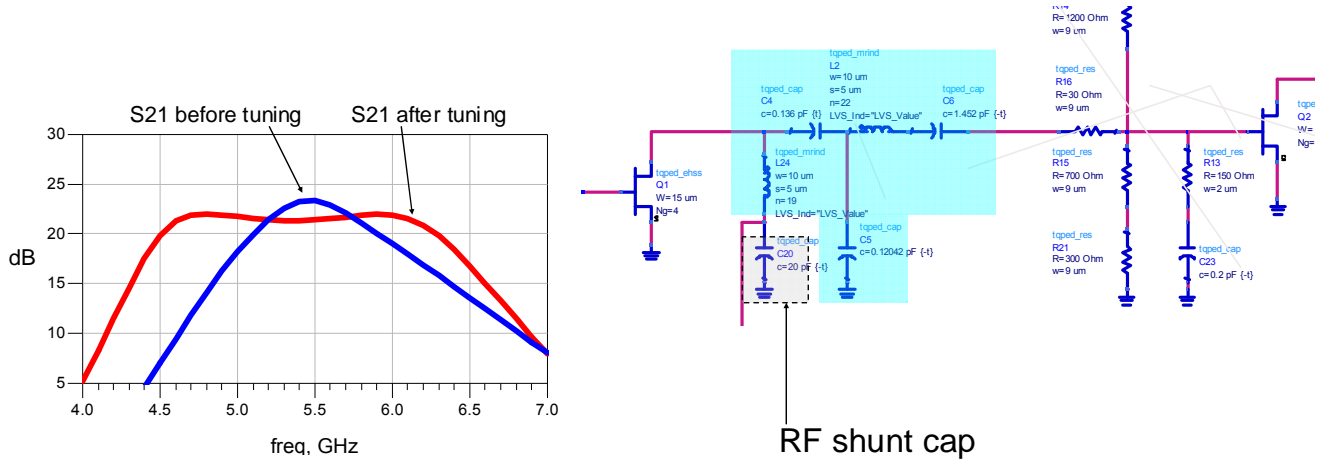
To improve PAE the output matching network (OMN) was modified. . As indicated in the figure below, a Parallel combination of inductor and capacitor was added in series and shunt. The addition of these elements created a looping of the impedance locus, thereby enhancing the bandwidth of the output Cripps match.



The figures below show the return loss looking of the OMN looking into the lumped element Cripps equivalent circuit of the fet's output.



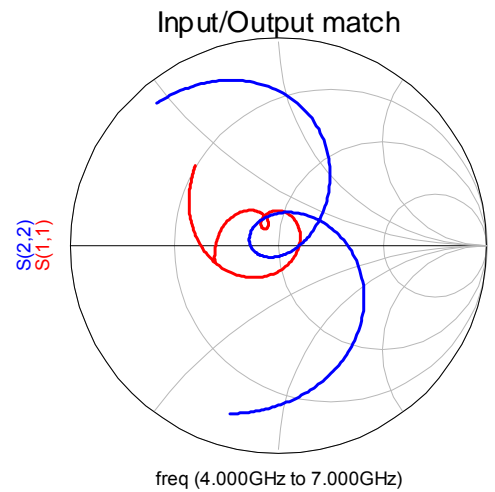
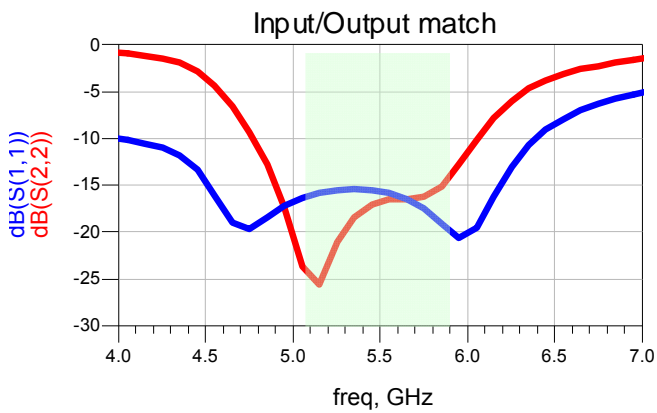
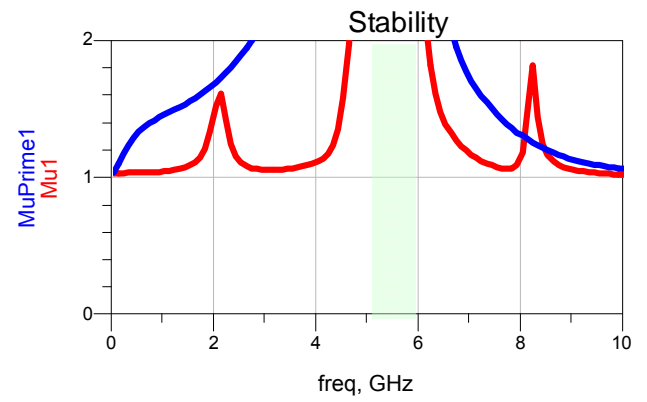
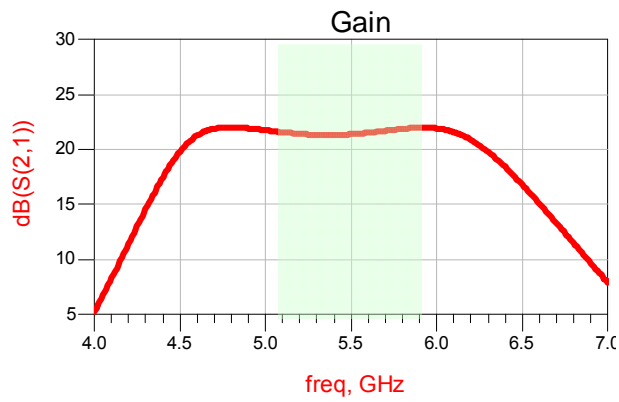
Although gain was better than 20 dB, the  $\pm 1$  dB gain ripple requirement was exceeded. ADS's filter synthesis tool was employed to create a more complicated interstage matching network. Additional tuning improved the gain ripple to less than  $\pm 0.3$  dB, as indicated in the graph below.



The filter synthesis tool was also used on the input matching network (IMN). Tuning of the IMN enabled the design to meet the input match requirement for the entire band.

# Simulation

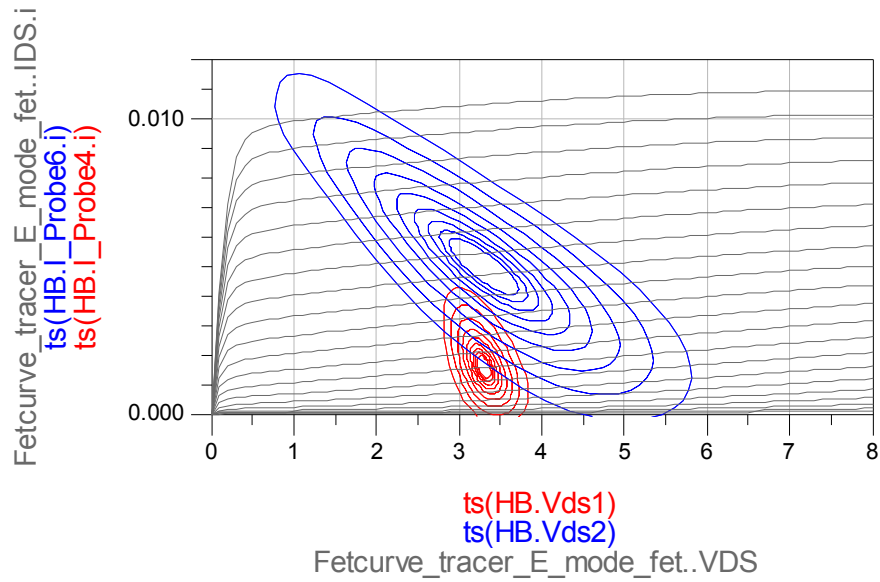
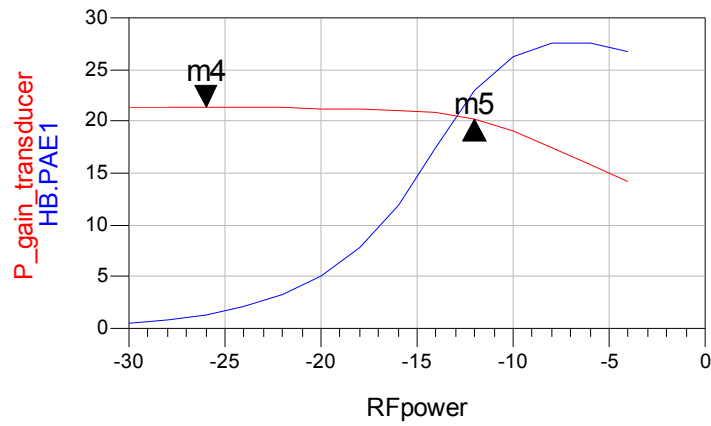
The following graphs depict small signal performance.



The following graphs depict large signal performance.

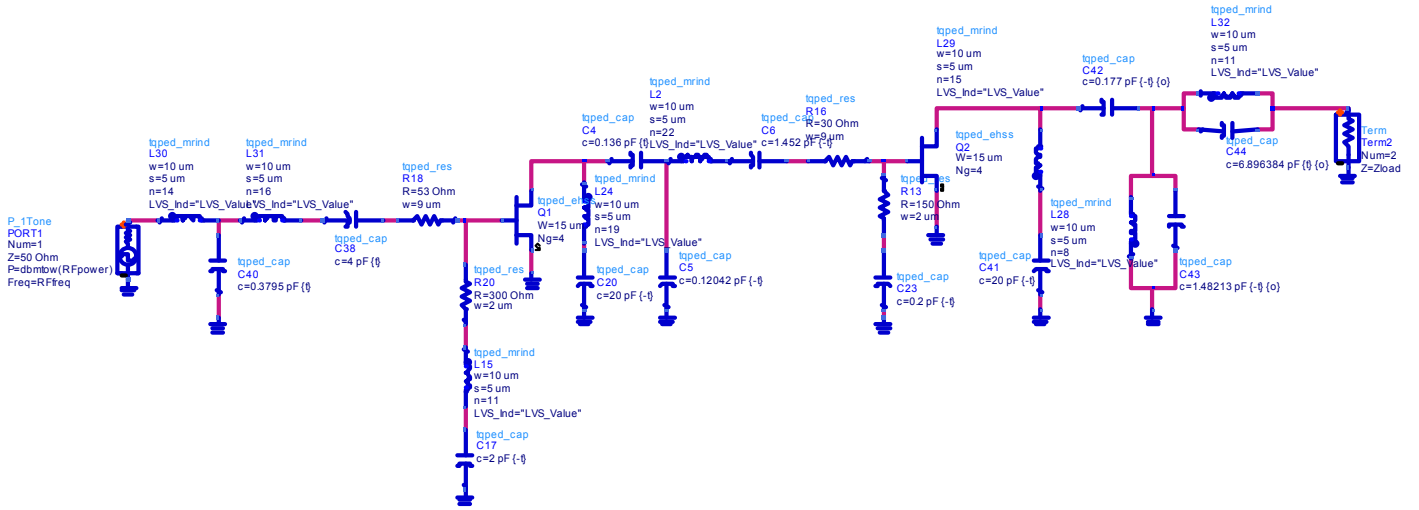
m4  
RFpower=-26.000  
P\_gain\_transducer=21.355

m5  
ind Delta=14.000  
dep Delta=-1.078  
delta mode ON

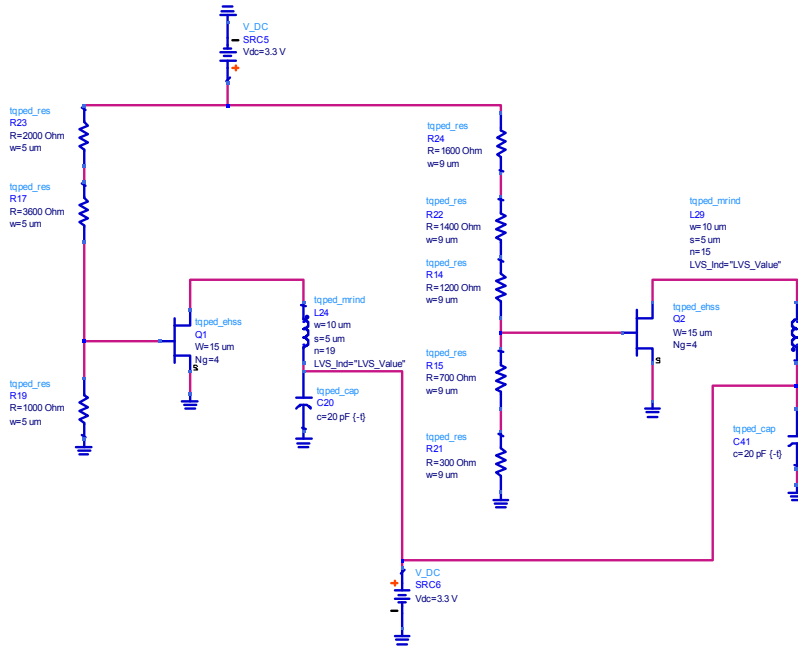


# Schematics

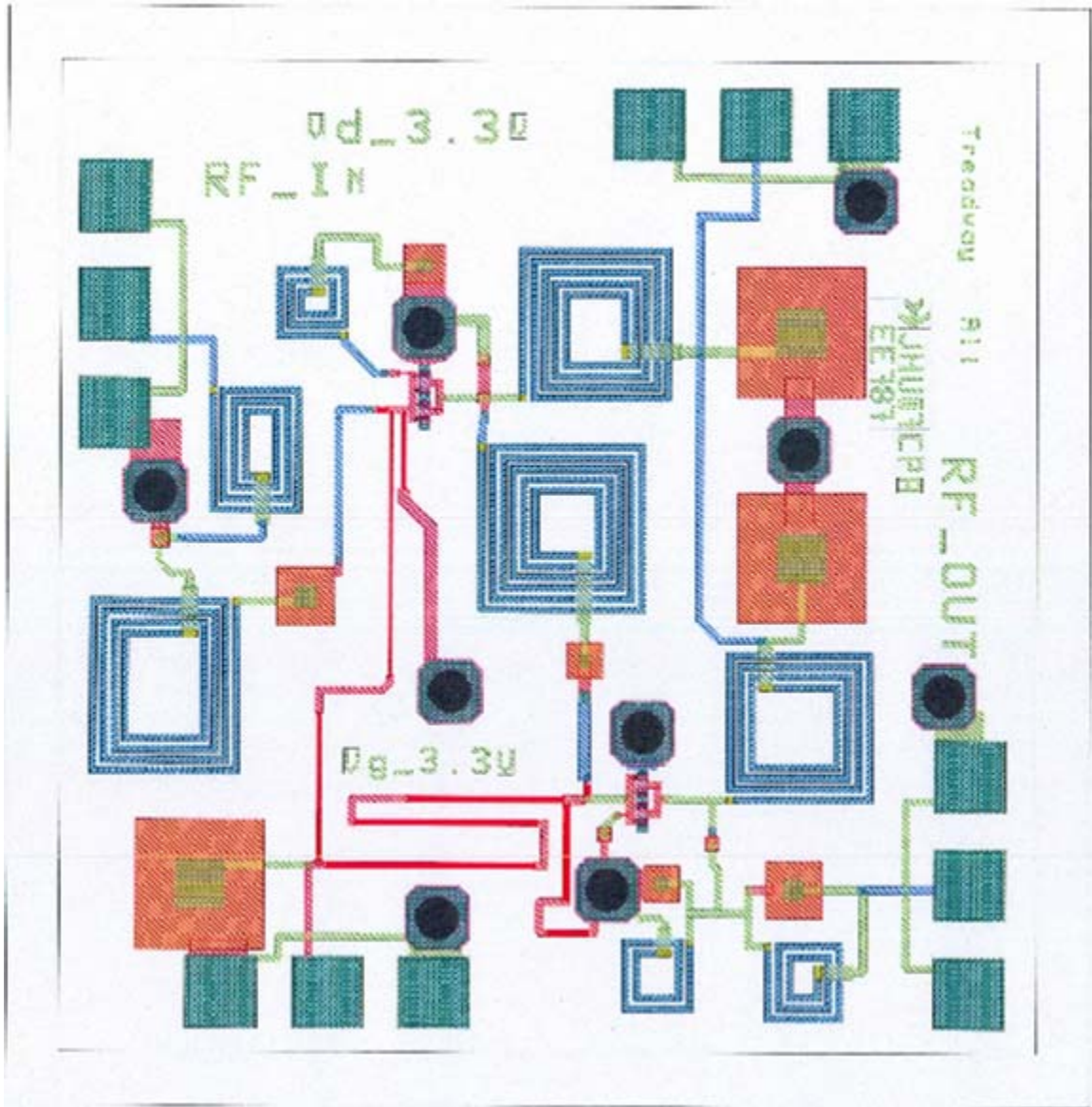
## RF schematic



## DC schematic



# Layout



## **Test Plan.**

### Small signal performance

1. Measure s-parameters on a VNA. Reduce VNA output power to -20dBm. Attach fixture to VNA. Adjust Vg bias supply to 0 V and slowly raise Vd bias to 3.3 V. Verify devices are pinched off. Slowly raise Vg supply to 3.3 V. Verify Vd bias current does not exceed 10 mA.
2. Measure s-parameters from 4 to 7 GHz

### Large signal performance.

1. Perform Pin/Pout test. Be sure to drive part into 1 dB compression.
2. Perform test at 5.15 GHz, 5.5 GHz, and 5.875 GHz.