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**Design and Layout of a S-band, High
Efficiency, Medium Power Amplifier
using Agilent's Advanced Design System
Software.**

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Table of Contents

1. Abstract.....	Page 2
2. Introduction.....	Page 2
3. Design Approach.....	Page 2
3.1. Power Amp	Page 3
3.1.1. Determine Bias Point, PAE, and RCripps	Page 3
3.1.2. Add Bias Circuitry and Stabilize	Page 4
3.1.3. Matching Network	Page 4
3.2. Driver Amp	Page 6
3.2.1. Determine Bias Point	Page 6
3.2.2. Matching interface network	Page 7
3.3 Specification versus goals	Page 10
3.4 Tradeoffs	Page 10
4. Additional Simulations.....	Page 10
5. Layout.....	Page 15
6. Test Plans.....	Page 16
6.1 Linear Parameters	Page 16
6.2 Power Measurements	Page 16
7. Conclusion and Recommendations.....	Page 16

Figures and Tables

Figure 3.1.1, Emode FET Bias Characteristics for a 60 μm (4x15) TriQuint FET	Page 3
Figure 3.1.2, Power Amp output stage with bias and stability circuit	Page 4
Figure 3.1.3a, Power Amp ideal output stage with matching	Page 5
Figure 3.1.3b, Gain, Power Out, and PAE for the ideal Power Amp output stage	Page 5
Figure 3.2.1a, Emode FET Bias Characteristics for a 60 μm (4x15) TriQuint FET	Page 6
Figure 3.2.1b, Power Amp ideal driver amp stage with matching circuits	Page 7
Figure 3.2.3, Two Stage High Efficiency, Medium Power Amplifier w/ single DC feed	Page 8
Figure 3.2.4, Linear simulation of 2 Stage High Efficiency, Medium Power Amplifier	Page 9
Table 3.3.1, Specification Compliance Matrix for a Two Stage, S-band Power Amp	Page 10
Figure 4.1, Non-Linear simulation of 2 Stage High Efficiency, Medium Power Amp	Page 11
Figure 4.2, Non-Linear simulation showing PAE, Gain, and Power Output at 1dB	Page 12
Figure 4.3, Linear Simulation showing Gain, Gain ripple, and VSWR (Final Circuit)	Page 13
Figure 4.4, Linear Simulation showing Stability and Noise (Final Circuit)	Page 14
Figure 5, S-band, High Efficiency, Medium Power Amplifier Layout generated in ADS	Page 15
Table 7, Specification Compliance Matrix for a Two Stage, S-band Power Amp	Page 16

1. Abstract

This paper describes the design, simulation and layout of a two-stage GaAs MMIC power amplifier operating at S-band frequency from 2.3 to 2.5 GHz. The power amplifier was designed using Agilent's Advanced Design System Software which included the TriQuint elements library. The critical design parameter for this High Efficiency Power Amplifier design is Power Added Efficiency (PAE). Simulations show that my design should achieve a PAE greater than 22% over a 100 MHz bandwidth centered at 2.4 GHz.

2. Introduction

Modern RF and microwave transmitter designs utilize integrated circuit power amplifiers that directly interface with the radiating element in order to maximize RF power output and efficiency. The primary goal for this design is to get the most RF output power for a given DC power consumption in order to extend battery life. My design will utilize a single supply voltage in the range of 3.0 to 3.6 VDC so that a small battery will be able to power the device. Additionally, I chose to build a two stage design that uses two 60 μm (4x15) Emode PHEMTs. The Emode FET was selected over the Dmode FET due to its higher gain for a given DC power consumption.

My S-band Power Amplifier design is based on the following criteria:

FREQUENCY:	2305 to 2497 MHz
BANDWIDTH:	> 193 MHz
GAIN, small signal:	> 24 dB with a goal of 26 dB
GAIN RIPPLE:	± 1 dB
OUTPUT POWER:	TBD @ 20-25% PAE
SUPPLY VOLTAGE:	+ 3.3 Volts only, goal (3 to 3.6V range)
VSWR, 50 Ohm:	< 1.5:1 input & output
SIZE:	Layout must fit on a 60 x 60 mil ANACHIP

3. Design Approach

My design strategy will be to use two stages in order to get sufficient gain and power output over the 200 MHz bandwidth. I found during some initial simulations that a single amplifier would not allow me to meet the gain ripple requirements and hence a two stage design is required. One of the goals for this design is to minimize power consumption to less than 40 mW. Also, keep in mind that the two stages will be self biased through a voltage divider network so there will be additional power consumed by biasing resistors. So, the first step will be to design the output stage using the Cripps method to determine the output

network with a bias goal of $I_{\max}/2 \approx 15$ mA. The next step will be to design the driver amplifier stage biased to approximately 15 to 20% of I_{dss} . Finally I will combine the two stages using a matching network and simplify the inter-stage topology while tuning the remaining elements to obtain the specifications listed in the introduction.

3.1. Power Amp

3.1.1. Determine Initial Bias Point, PAE, and RCripps

Setting V_{ds} to 3.5 VDC we see in Figure 3.1.1 that V_{gs} is equal to 0.679 VDC which is a reasonable bias point for an Emode FET. This bias value will allow for a simple design of the associated resistor bias network.

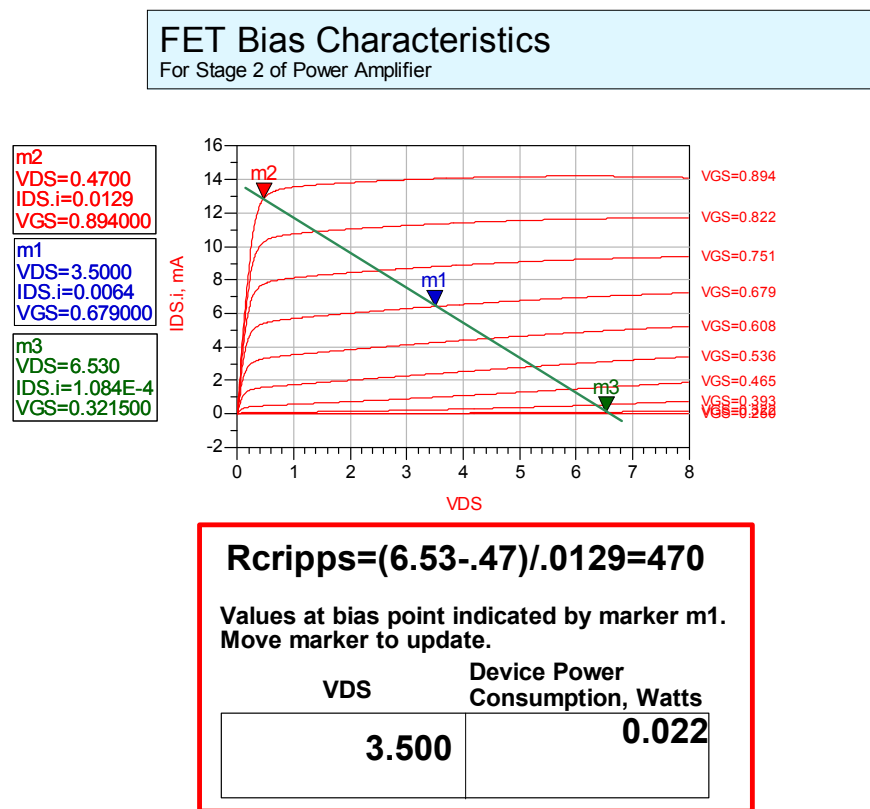


Figure 3.1.1, Emode FET Bias Characteristics for a 60 μm (4x15) TriQuint FET

Using the load line in Figure 3.1.1 I determine that ΔV_{DS} is equal to $2 \times (3.5 - 0.47) \text{V} = 6.06 \text{V}$ and that ΔI_{DS} is about 12.9 mA. Therefore, RF output power should be approximately equal to $(\Delta V_{\text{DS}} \times \Delta I_{\text{DS}}) / 8 \approx 9.8 \text{mW}$. With the device power consumption at 22 mW my Power Added Efficiency (PAE) should be approximately 44 %. However, I expect the actual PAE to be lower due to the additional power that will be consumed by biasing resistors. My R_{cripps} value can be calculated with the formula $\Delta V_{\text{DS}} / \Delta I_{\text{DS}}$ which equals 470 Ω .

3.1.2. Add Bias Circuitry and Stabilize

My main goal for the design of my bias circuit is to achieve a single DC feed for the Gate and Drain of my Emode FET's. I discover during simulations that the stability of the circuit is greatly affected by the value of the bias resistors. The higher the resistance the more unstable the circuit becomes. I utilized a series resistor "R5" to stabilize my circuit with higher value bias resistors. Higher value bias resistors are preferred in order to lower the power consumed by the bias circuit and improve the gain. My stabilized bias circuit is illustrated in Figure 3.1.2 below.

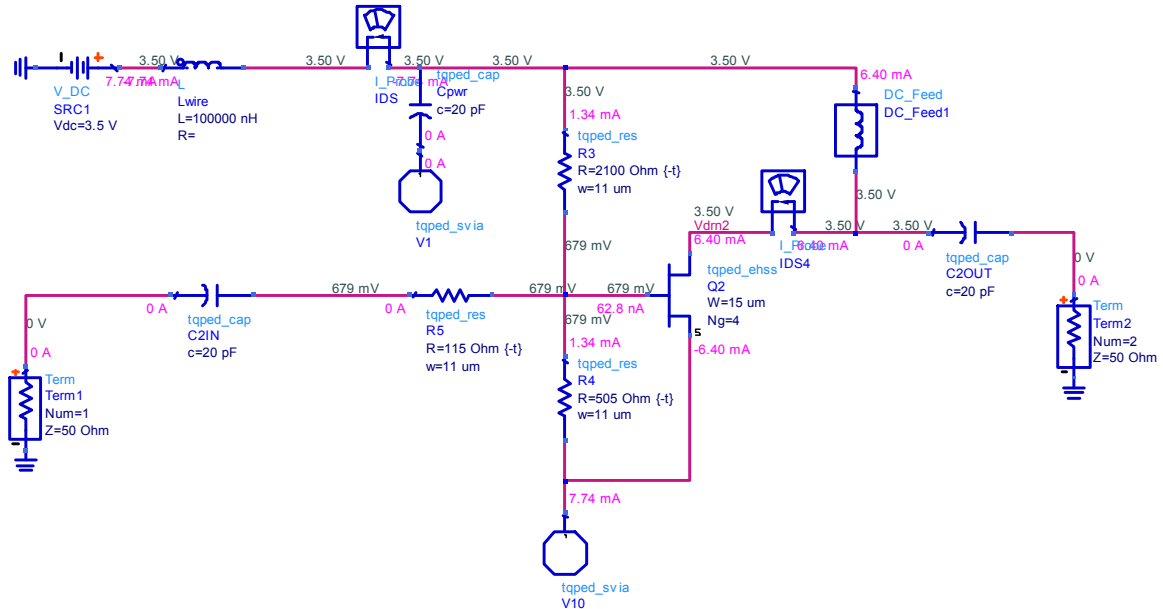


Figure 3.1.2, Power Amp output stage with bias and stability circuit.

3.1.3. Matching Network

Now using the "Cripps Method" I design the output matching circuit. The impedance looking into the output (S22) of the amplifier is equivalent to a 59.6 fF shunt capacitor in parallel with a 1457 Ω shunt resistor (Rds), which gives a S22 value of $536.7 - j703.4 \Omega$. I want to resonate out the reactance and replace Rds with the resistance of $R_{cripps} = 470 \Omega$. This results in a S22 value of $398.8 - j168.5 \Omega$. Now I take the conjugate value of S22 and use the Smith chart to determine the circuit element values that correspond to the path going from $398.8 + j168.5 \Omega$ to 50 Ω . This results in a 9.4 nH shunt inductor followed by a 0.46 pF series capacitor which provide a match to 50 Ω for the Cripps output matching circuit. I place the components in the ADS schematic and then determine the value of S11. To do this I take the conjugate value of S11 ($200.5 + j185.9 \Omega$) and design an input matching circuit to map S11 to 50 Ω . Doing this yields a 7.31 nH shunt inductor followed by a 0.524 pF series capacitor. Figure 3.1.3a illustrates the schematic for an ideal output stage of my power amplifier design.

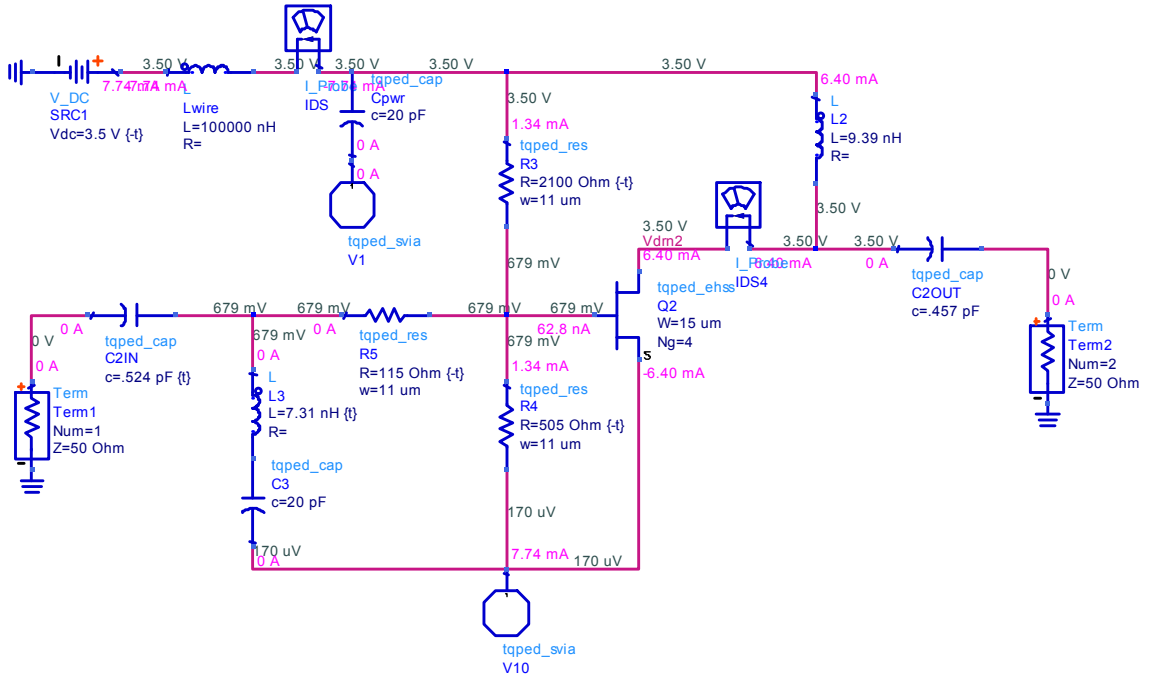


Figure 3.1.3a, Power Amp ideal output stage with matching circuit using R_{Cripps} method

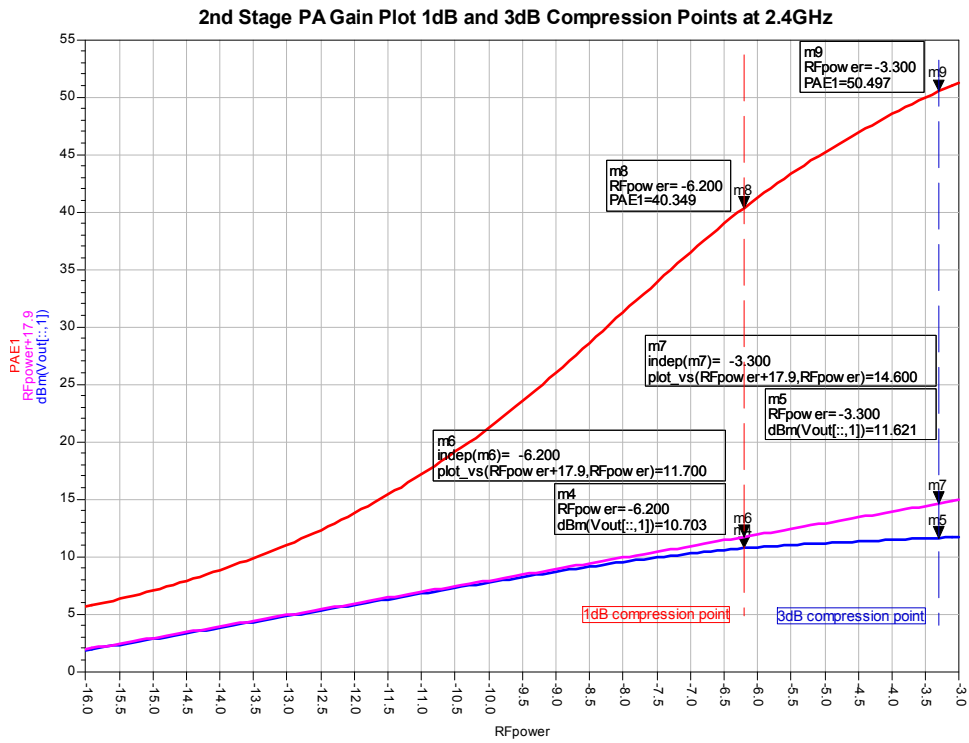


Figure 3.1.3b, Gain, Power Out, and PAE for the ideal Power Amp output stage.

Note from Figure 3.1.3b it can be seen that 1 dB of compression occurs at approximately -6.4 dBm of RF power in. This is a key piece of information required for the design of the Driver Amplifier stage. The driver amplifier will be designed to be linear past -6 dBm RF Power in to prevent compression before the output stage of the power amp.

3.2. Driver Amp

3.2.1. Determine Bias Point

For the driver amp design it is important to achieve gain with minimal DC power. This may be accomplished with the load line shown in Figure 3.2.1a below. The bias point is based on taking approximately 20% of IDSS of the output stage, refer to Figure 3.1.1.

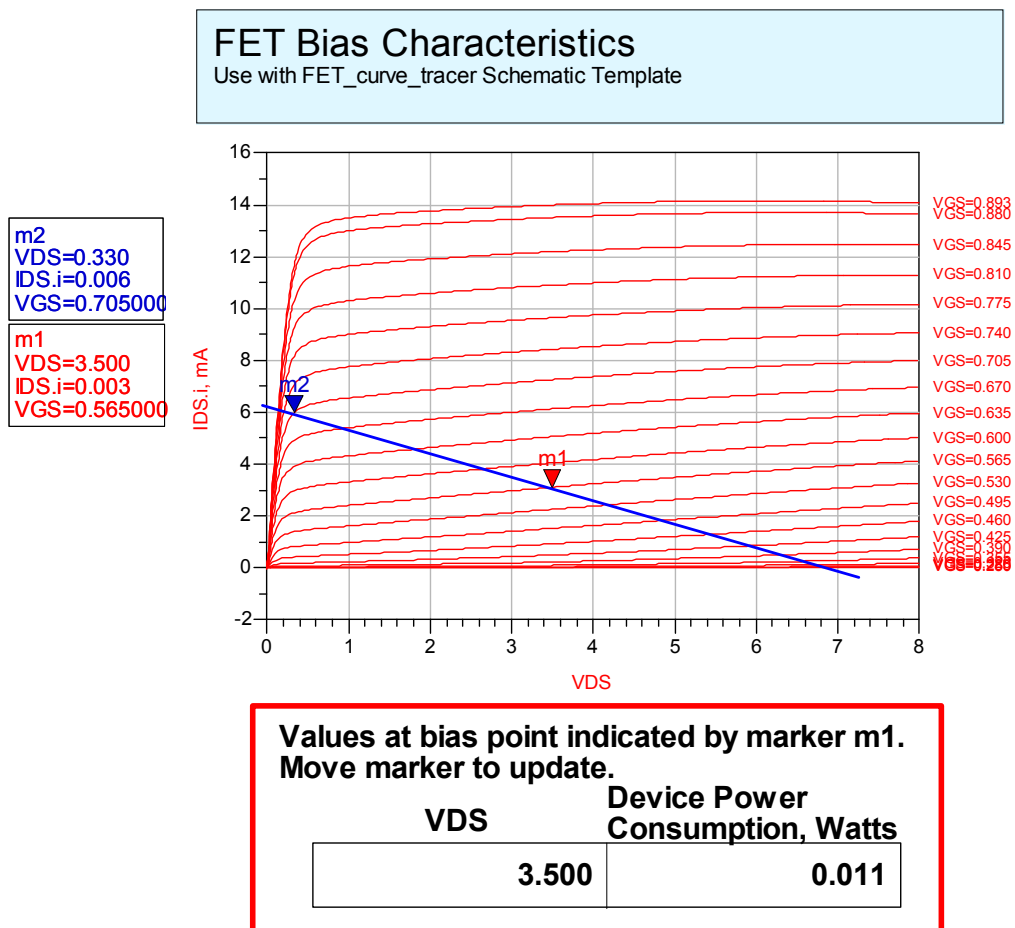


Figure 3.2.1a, Emode FET Bias Characteristics for a 60 μm (4x15) TriQuint FET

Using the load line in figure 3.2.1a I determine the RF output power for my driver stage should be approximately $(\Delta V_{DS} \times \Delta I_{DS})/8 \approx (2(3.5-.33)V_{DC} \times 6mA)/8 \approx 4.8 \text{ mW}$. With the device power consumption at 11 mW my Power Added Efficiency (PAE) should be

approximately 43 %. However, I expect the actual PAE to be lower due to the additional power that will be consumed by biasing resistors. Now I generate my circuit using the same steps and criteria used in section 3.1.2 through 3.1.3 to come up with my circuit shown in figure 3.2.1b below.

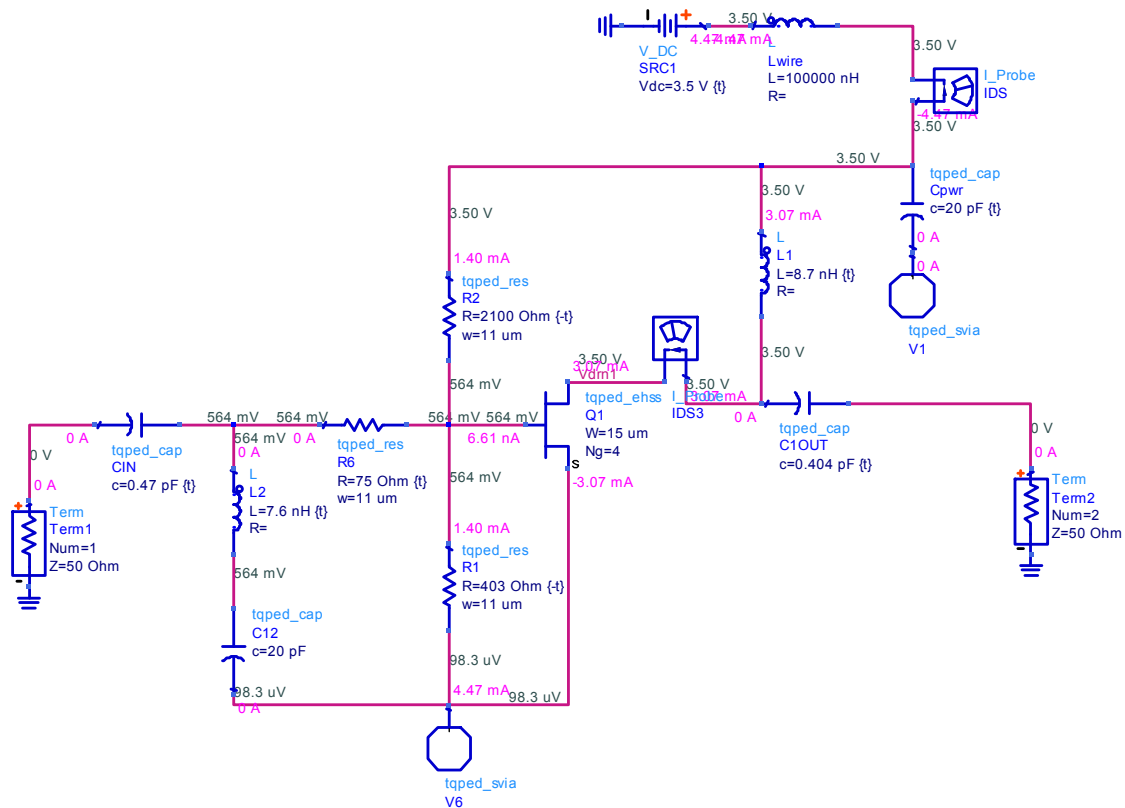


Figure 3.2.1b, Power Amp ideal driver amp stage with matching circuits.

3.2.2. Matching interface network

Now that I have my driver amp stage I need to match the output of the driver amp to the input of the power amp output stage. I use the smith chart to determine the component values of my intermediate matching circuit and connect the two circuits and tune. Figure 3.2.3 shows the entire two stage high efficiency power amp circuit. Note that I tune the two stages to obtain a flat gain response across the entire bandwidth as illustrated in Figure 3.2.4. Also, I met the specification for VSWR across the entire bandwidth for the input but I was only able to achieve the output VSWR specification for about 140 MHz of bandwidth. This would be one of the areas of concentration for future improvements of my circuit.

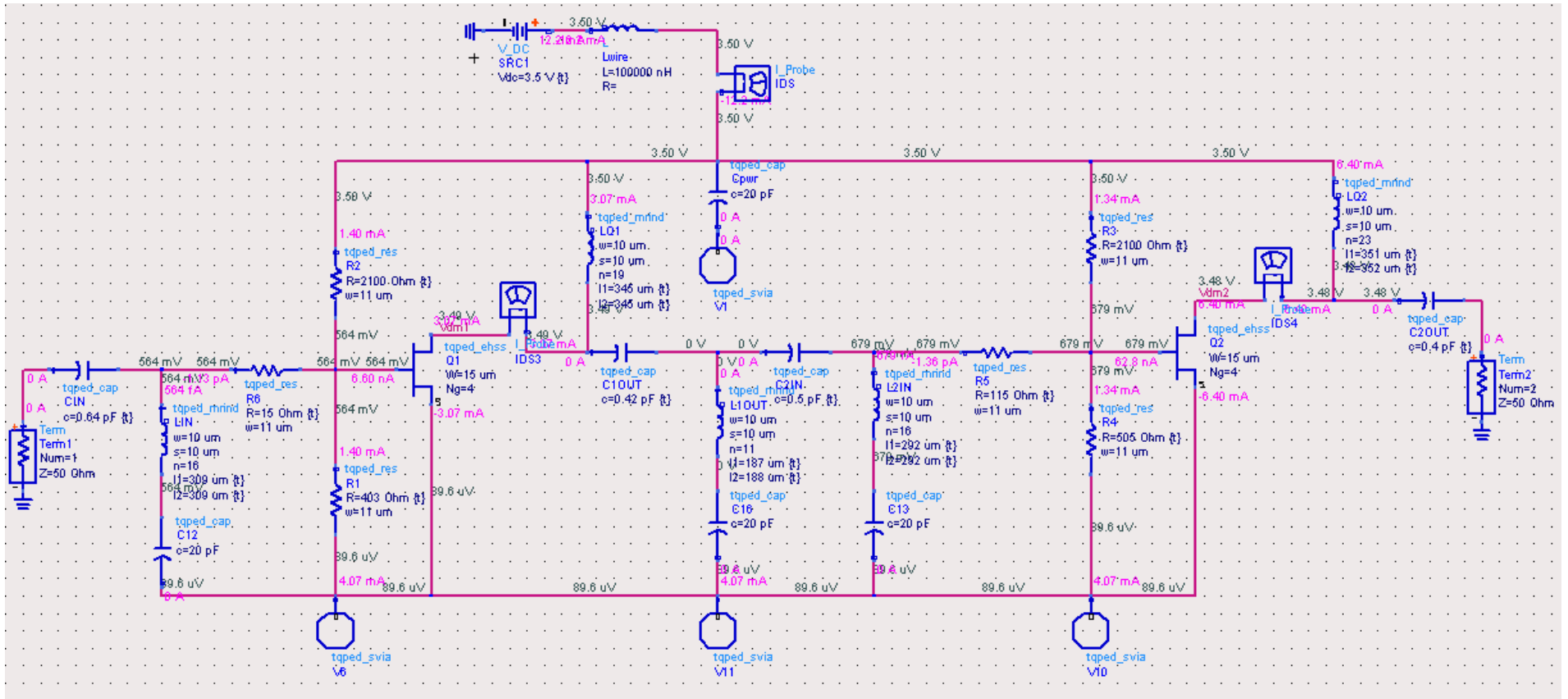


Figure 3.2.3, Two Stage, High Efficiency, Medium Power Amplifier with single DC power feed.

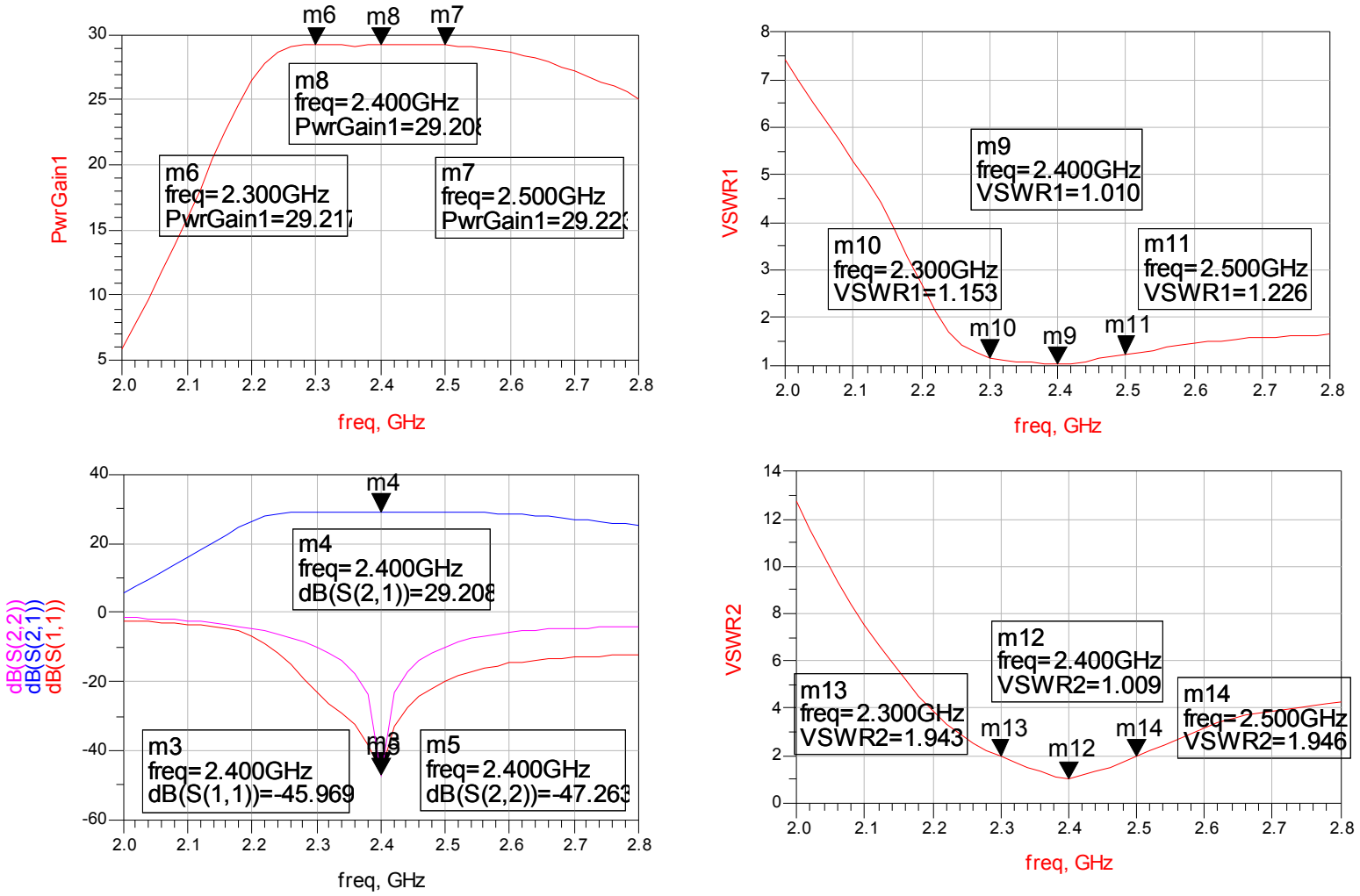


Figure 3.2.4, Linear Simulation results from my High Efficiency, Medium Power Amplifier.

3.3 Specification versus goals

Table 3.3.1 summarizes the design specification and the simulated results of both the simplified schematic and final layout schematic.

	Specification Goal	Simplified Schematic	Final Layout
Bandwidth	> 193 MHz	200 MHz	200 MHz
Gain	26 dB	29 dB	28 dB
Gain Ripple	± 1 dB	± 0.02 dB	± 0.2 dB
Output Power	TBD	10.1 dB	10.2 dB
Power Added Efficiency	20-25%	24%	23.3%
VSWR	< 1.5:1 input & output	1.01:1 input 1.01:1 output	1.01:1 input 1.01:1 output
DC Supply Voltage	3.0 – 3.6 VDC	3.5 VDC	3.5 VDC

Table 3.3.1, Specification Compliance Matrix for a Two Stage, S-band Power Amp.

3.4 Tradeoffs

The only major tradeoff I recognized in designing this circuit was Gain versus Stability. As I mentioned earlier there was a clear tradeoff when determining the size of the biasing resistors and the amount of power consumed by the bias circuit. Larger value biasing resistors meant lower power consumption by the bias circuit and higher power added efficiency. However, the tradeoff came in the form of instability to the circuit and therefore the need for larger series stabilizing resistors resulting in higher noise. However, noise was not a factor of consideration in the design of this circuit. Ultimately, an iterative process was used to determine the size of the biasing resistors and series stabilizing resistors.

4 Additional Simulations

Figure 4.1 illustrates the results of a nonlinear simulation detailing the dynamic load line response for my 1st and 2nd stages of the Power Amplifier. Figure 4.2 further illustrates the nonlinear simulation results showing Power Added Efficiency, Power Output, and Gain of my final circuit layout. Figure 4.3 and 4.4 show the linear simulation results of my final circuit.

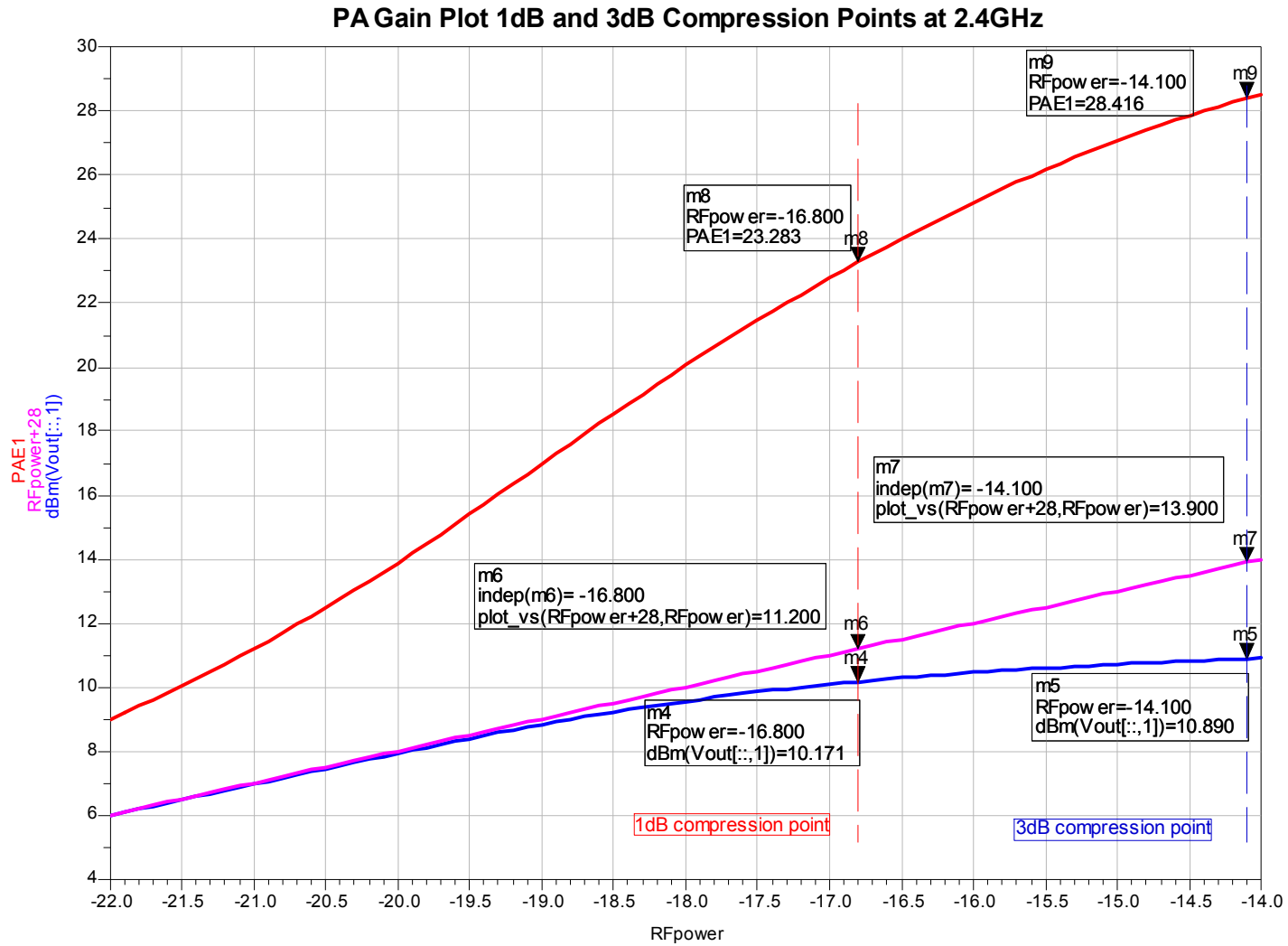


Figure 4.2, Non-Linear simulation showing PAE, Gain, and Power Output at 1dB and 3dB compression points.

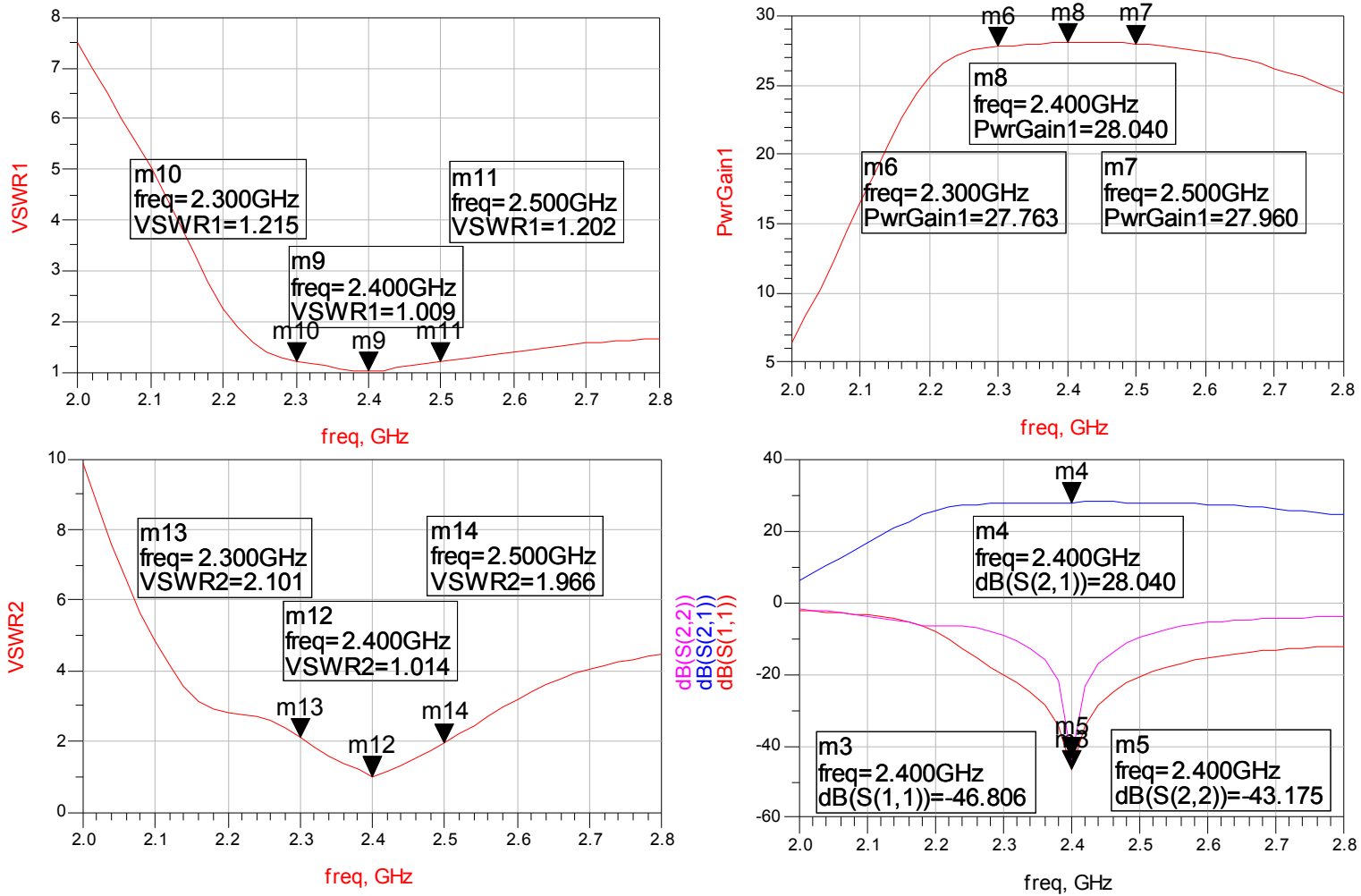


Figure 4.3, Linear Simulation showing Gain, Gain ripple, and VSWR (Final Circuit).

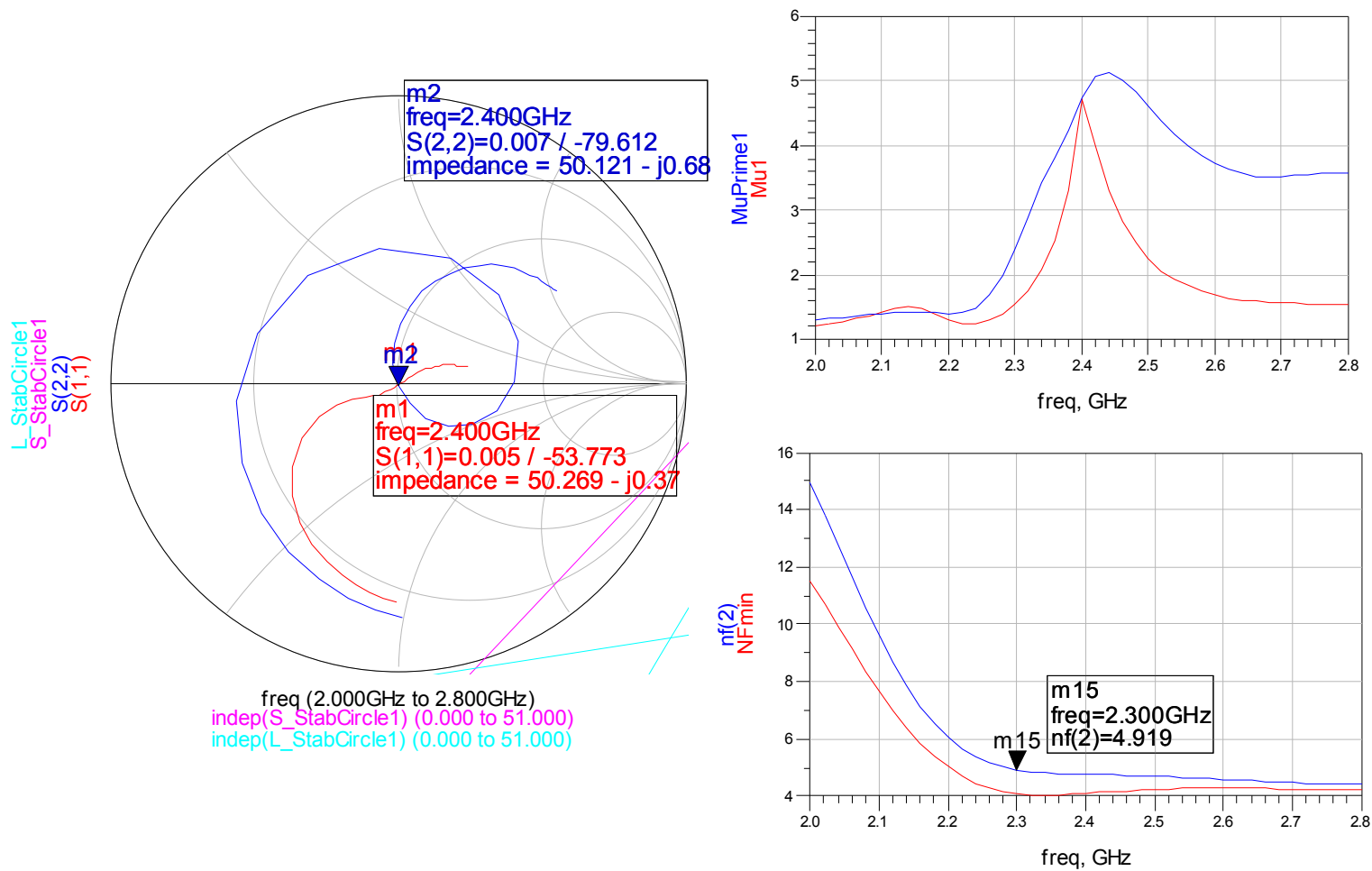


Figure 4.4, Linear Simulation showing Stability and Noise (Final Circuit).

5. Layout

The final circuit layout is illustrated in Figure 5 below.

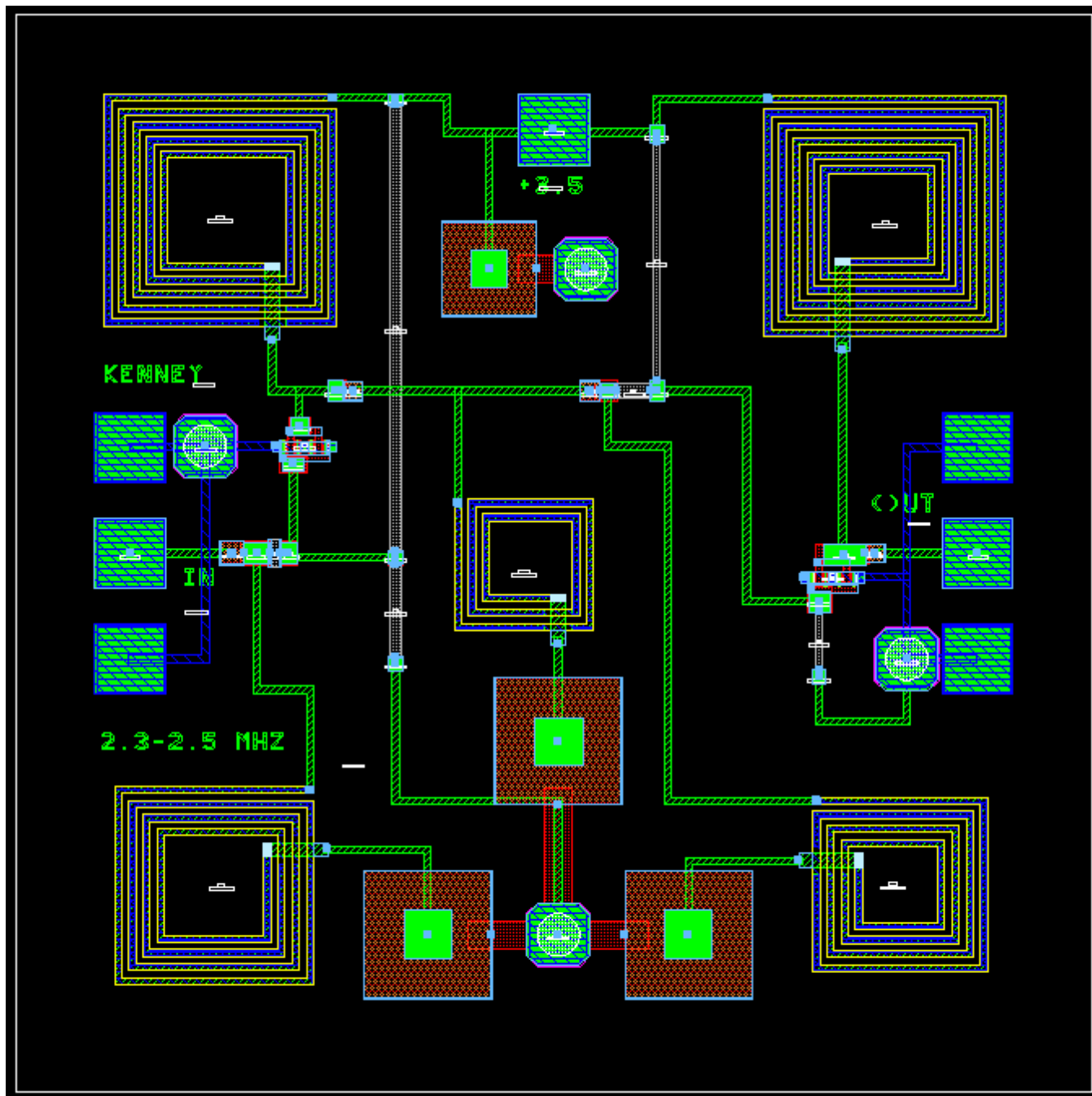


Figure 5, S-band, High Efficiency, Medium Power Amplifier Layout generated in ADS.

6. Test Plans

The following test procedures are recommended to test the 2 stage S band power amplifier.

6.1 Linear Parameters

Use an Agilent network analyzer to obtain the s parameters of the amplifier.

1. Calibrate the analyzer from 1GHz to 10GHz.
2. Place the DC bias power probe on the pad of the chip labeled “+3.5V”.
3. Place probe tips on the designated pads. The input port is labeled “IN” and the output port is labeled “OUT”.
4. Turn on the power supply and slowly adjust to +3.5V.
5. Record data.

6.2 Power measurements

For power measurements it is recommended that a signal generator and spectrum analyzer be used.

1. Connect the signal generator probe to the input pad of the amplifier chip, which is the port marked “IN”.
2. Connect the spectrum analyzer probe to the output pad of the amplifier chip, which is the port marked “OUT”.
3. Place the bias probe on the pad of the chip labeled “+3.5V”.
4. Turn on the power supply and slowly adjust to +3.5V.
5. For Pin vs. Pout set the generator to the frequency of interest and sweep the power up to, but not exceeding, 0 dBm and recording measurements from spectrum analyzer after each interval.
6. For Pout vs. Frequency set the Generator to -16.8 dBm. Sweep the frequency and record measurements from the spectrum analyzer after each interval.

7. Conclusion & Recommendations

The S band 2 stage, high efficiency medium power amplifier design was a success and met and exceeded all of the specification goals in it’s simulations. Future recommendations on this design would include improving the output match to achieve < 1.5 to 1 VSWR over the entire bandwidth. Table 7 illustrates the achieved results from the simulations performed using ADS.

	Specification Goal	Simplified Schematic	Final Layout
Bandwidth	> 193 MHz	200 MHz	200 MHz
Gain	26 dB	29 dB	28 dB
Gain Ripple	± 1 dB	± 0.02 dB	± 0.2 dB
Output Power	TBD	10.1 dB	10.2 dB
Power Added Efficiency	20-25%	24%	23.3%
VSWR	< 1.5:1 input & output	1.01:1 input 1.01:1 output	1.01:1 input 1.01:1 output
DC Supply Voltage	3.0 – 3.6 VDC	3.5 VDC	3.5 VDC

Table 7, Specification Compliance Matrix for a Two Stage, S-band Power Amp.