# MMIC DESIGN PROJECT
# C BAND DRIVER AMPLIFIER

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**EE525.787**

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## Abstract

This report documents the design of a C band driver amplifier using the TriQuint TQS TRx process. The design was completed as part of the MMIC Design course offered by Johns Hopkins University. The amplifier was designed using the Advanced Design System (ADS) software which included the TriQuint elements library, and was laid out in a 60 x 60 mil Anachip. The driver amplifier is intended to be used in a simplex transceiver for the C band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies, and will be used in conjunction with other projects designed in the class.

# Introduction

## Circuit Description

The driver amplifier is basically comprised of two cascaded GFET transistors biased class AB. Input and output matching circuitry was used to achieve the desired performance as stated in the circuit specifications. Where possible, components were used in both the matching circuitry and bias networks to reduce the total number of components used in the design.

## Design Philosophy

In designing the driver amplifier the main focus was concentrated on output power and gain. These are critical parameters because the small amount of power exiting the variable amp must be amplified enough to drive the next stage which is the power amplifier. Also, it is desired in the specs to use only one 5v power supply, which calls for self-biased circuitry. For these reasons I chose the TriQuint 300um GFET for both stages.

The first step in the design was to determine the bias point for both stages. For the first stage I chose Iq to be about 1/3 IDSS primarily to increase efficiency and lower the power to drive the second stage.

Stage 1: Vds=3.8v ; Vgs=-1.2v; Id=29mA

This was done in ADS by connecting voltage sources to the gate and drain of the GFET and sweeping the voltages to obtain the parts IV curves.
Next, the bias for stage 2 was chosen to be about ½ IDSS because this is where the main power amplification is taking place.

Stage 2: Vds=4.2v; Vgs=-0.8v; Id=46mA

The next step in the design was to determine the input and output matching circuitry for the first and second stages, individually. This was done using the Cripps method, where the output impedance of the GFET is determined using the linear s parameter file. Using this technique an output matching circuit can be developed. Next, by cascading the s2p file with the output matching network, a matching network can now be developed for the input of the transistor. Note that ideal elements were used for this iteration of the design process and each stage was modeled separately.

After the matching circuitry is designed for both stages and each stage is optimized for best output power, return loss, and gain, (this includes both linear and nonlinear modeling) the two stages are now combined and the overall performance of the amplifier is optimized. Upon determining that the overall performance of the ideal element model is satisfactory, it is now time to substitute in the TriQuint elements. I modeled TriQuint capacitors and inductors against their ideal counterparts to obtain comparable values. Since inductors contained high series resistance, I added them one at a time and tweaked the circuit at each iteration.

The final step was to add interconnects to the circuit and take the overall layout into consideration. Once the circuit was laid out in the 60 x 60 mil anachip using microstrip lines, the performance must again be evaluated. I found that the greatest impact came in adjusting the various inductances in the circuit because the interconnections coming from each inductor added increased the inductance.

### Trade-offs

While a self-bias approach uses only one voltage supply and is relatively simple, the bias is not easily adjustable. A resistor ladder could have been added to compensate for variations in Vp but this would require more space.

# Modeled Performance

### Specification Compliance Matrix

The following table summarizes the design specification and the simulated results of both the simplified schematic and final layout schematic.

| | **Specification Goal** | **Simplified Schematic** | **Final Layout Schematic** |
|---|---|---|---|
| **Bandwidth** | >725 MHz | 1000 MHz | 1000MHz |
| **Gain** | >12 dB | 18.7dB | 13.6dB |
| **Gain Ripple** | ±0.5 dB | 0.37dB | 0.49dB |
| **Output Power** | >+13dBm | 14.77dBm | 14.1dBm |
| **VSWR** | <1.5:1 input & output | 1.24:1 input<br>2.44:1 output | 1.32:1 input<br>2.32:1 output |
| **Supply Voltage** | ±5v | +5v only | +5v only |

## Predicted Performance

The following plots show the modeled performance of the simplified schematic and the final layout schematic.

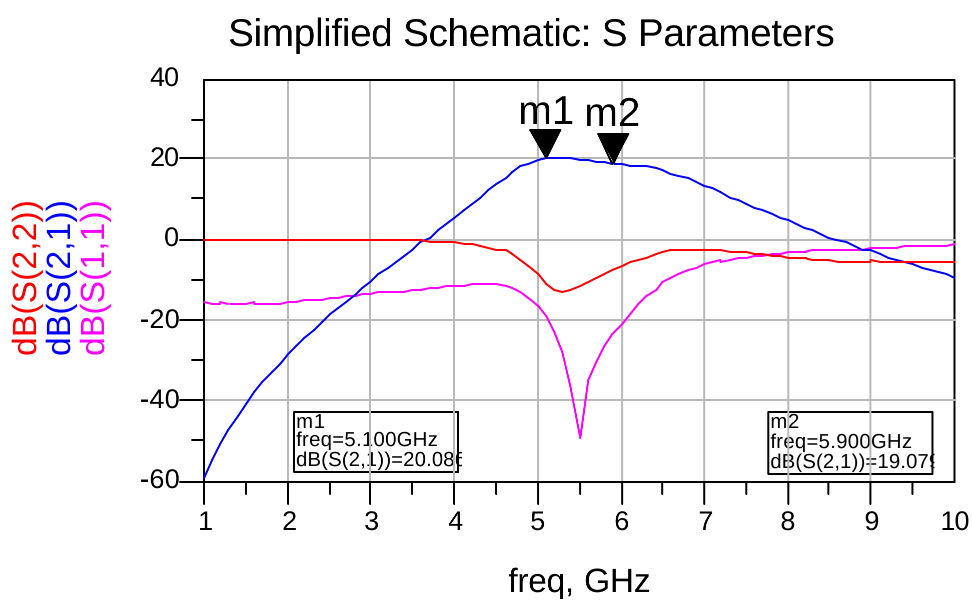


Figure 1: Simplified Schematic S Parameters

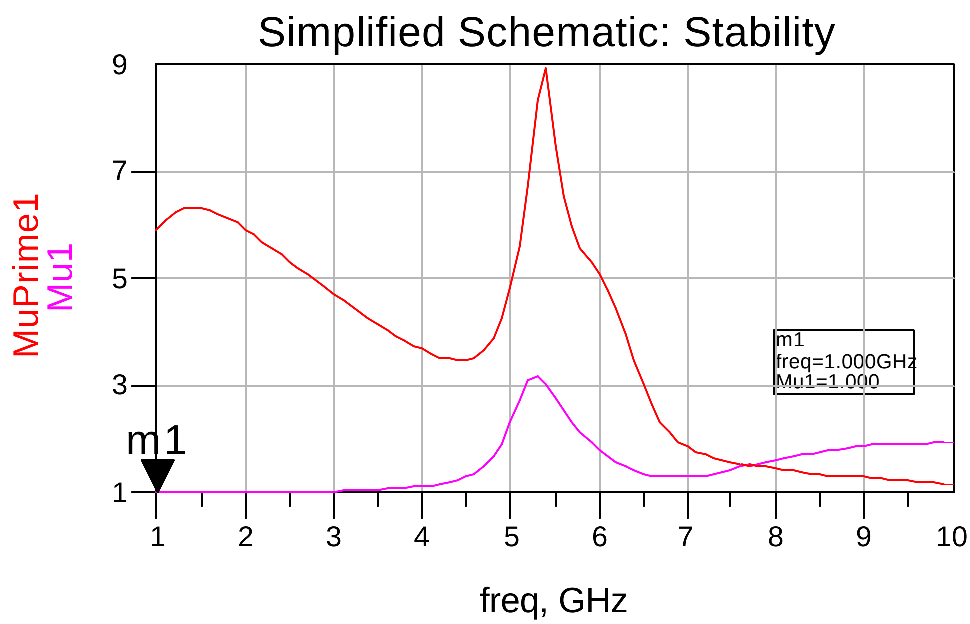


Figure 2: Simplified Schematic Stability

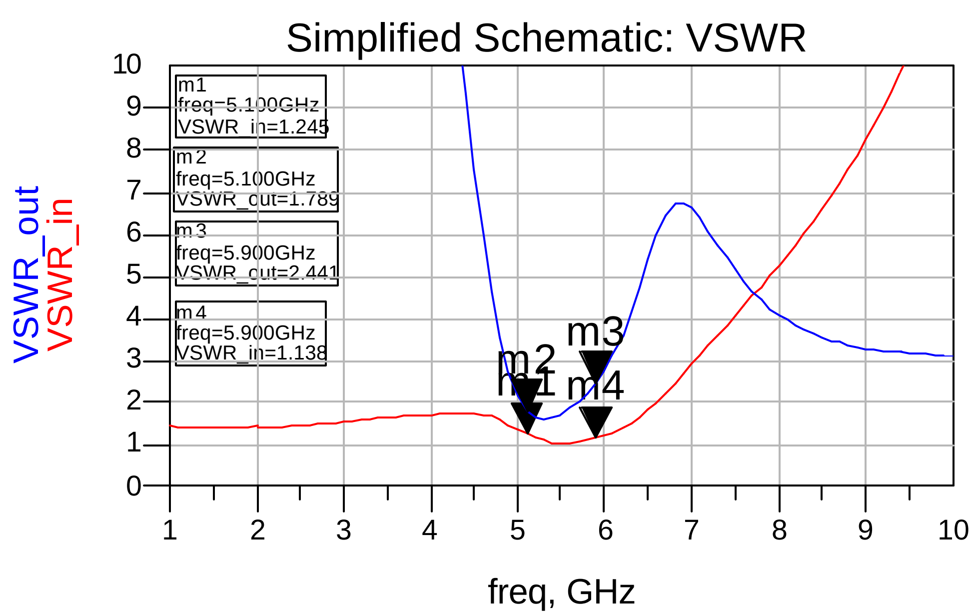


Figure 3: Simplified Schematic VSWR

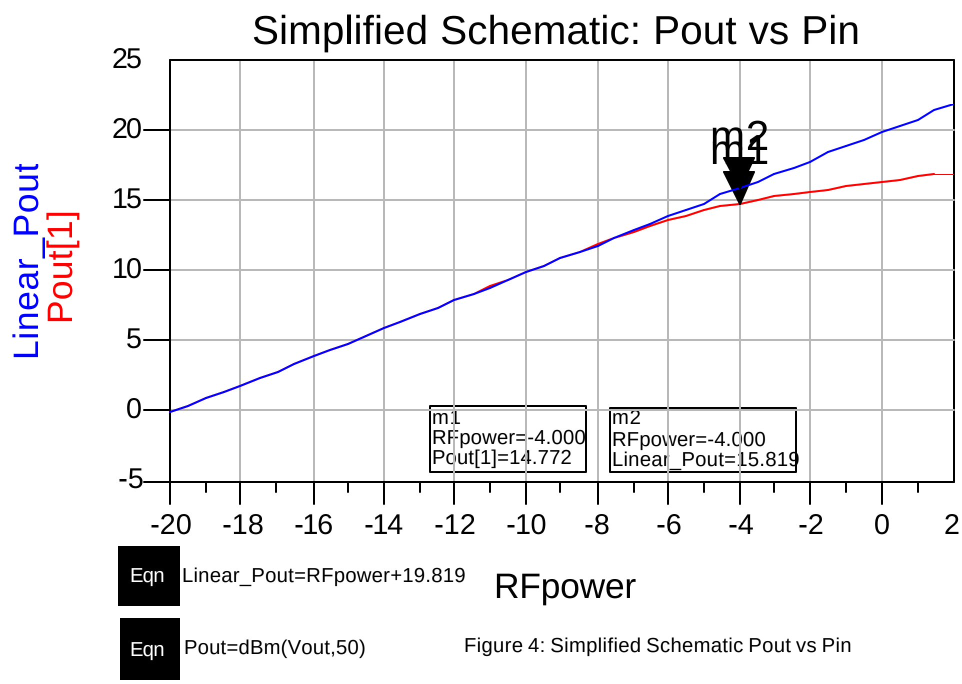


Figure 4: Simplified Schematic Pout vs Pin

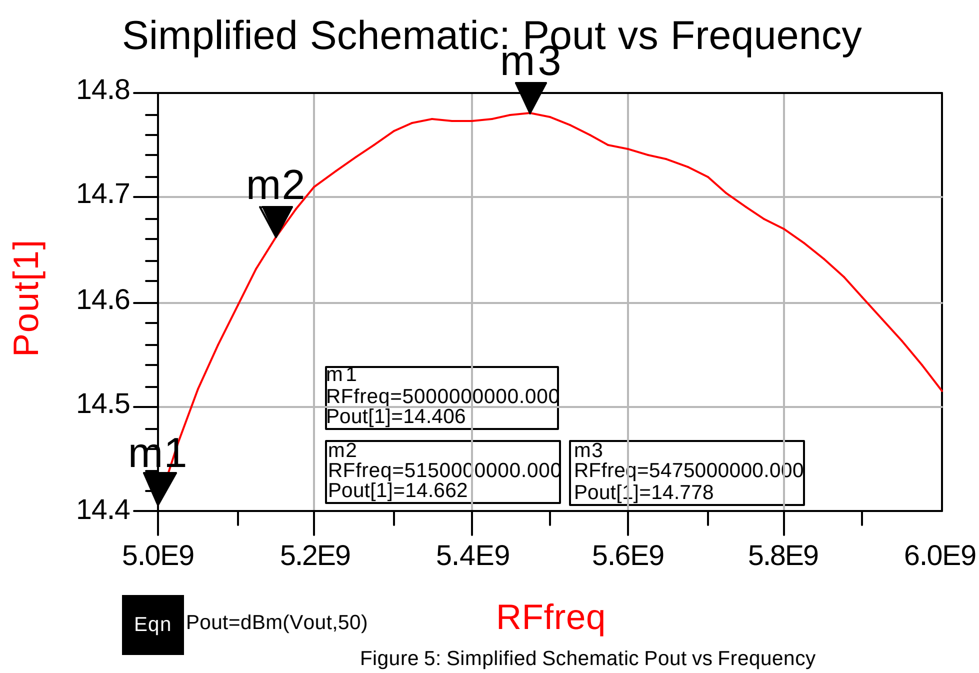


Figure 5: Simplified Schematic Pout vs Frequency

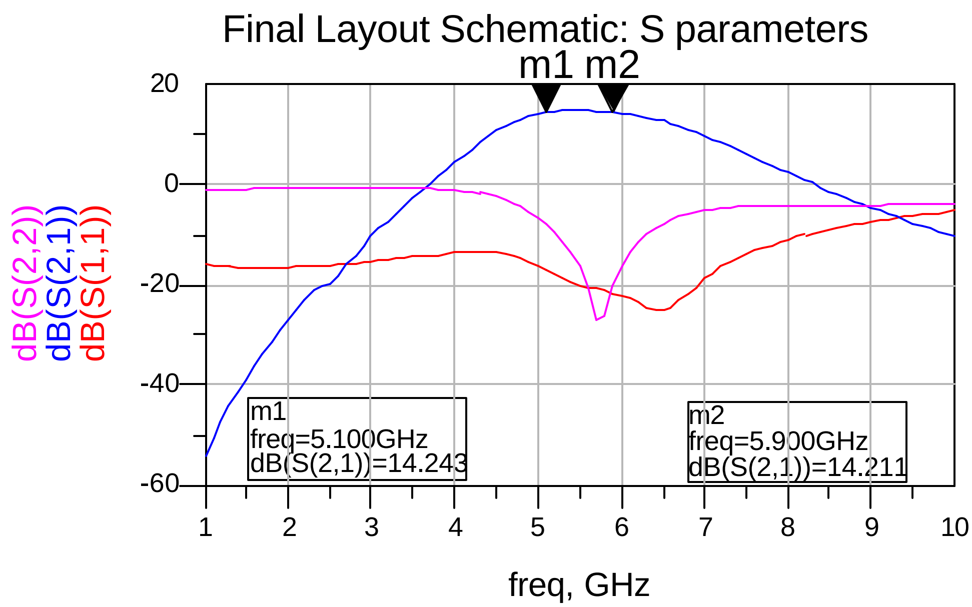


Figure 6: Final Layout Schematic S Parameters

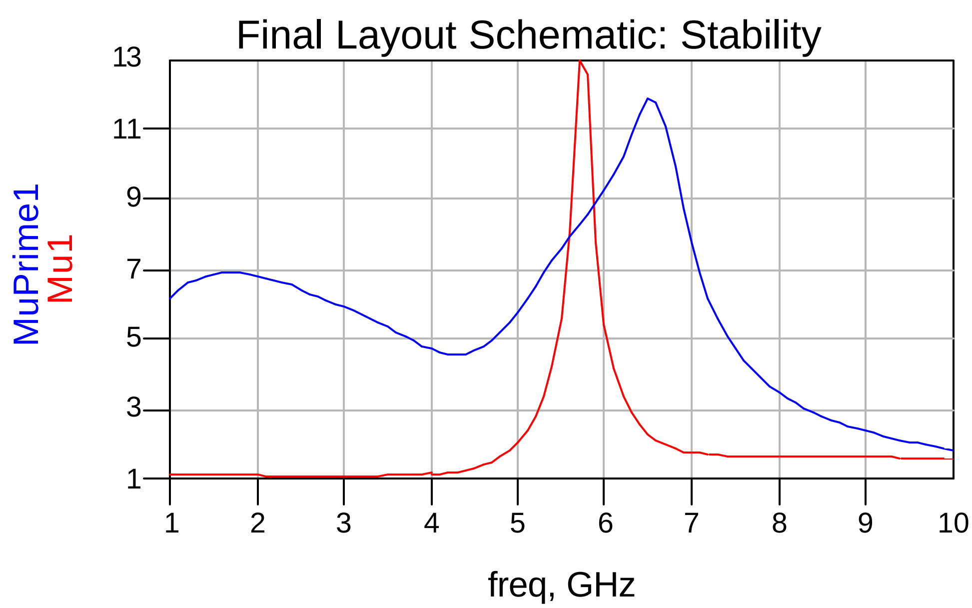


Figure 7: Final Layout Schematic Stability

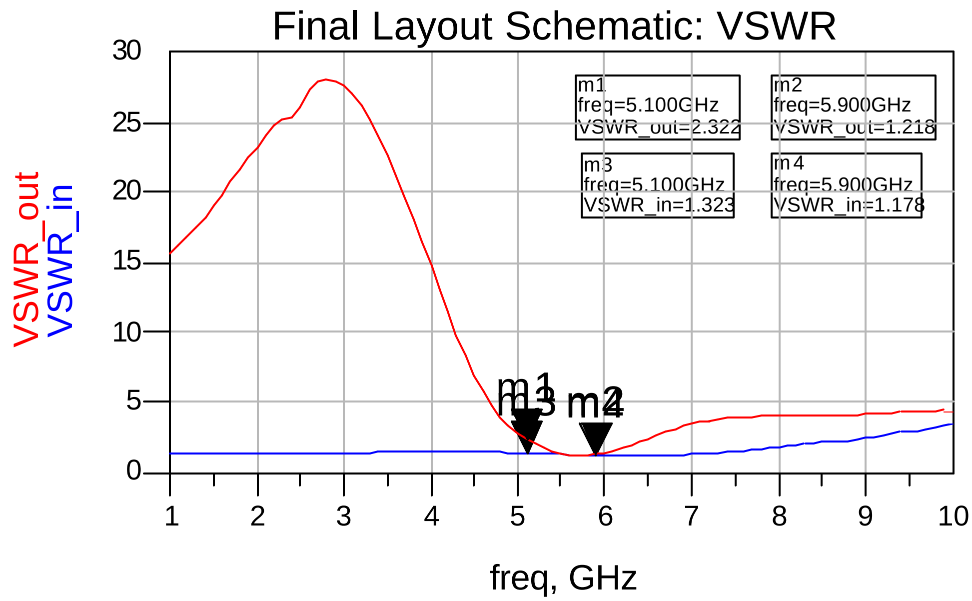


Figure 8: Final Layout Schematic VSWR

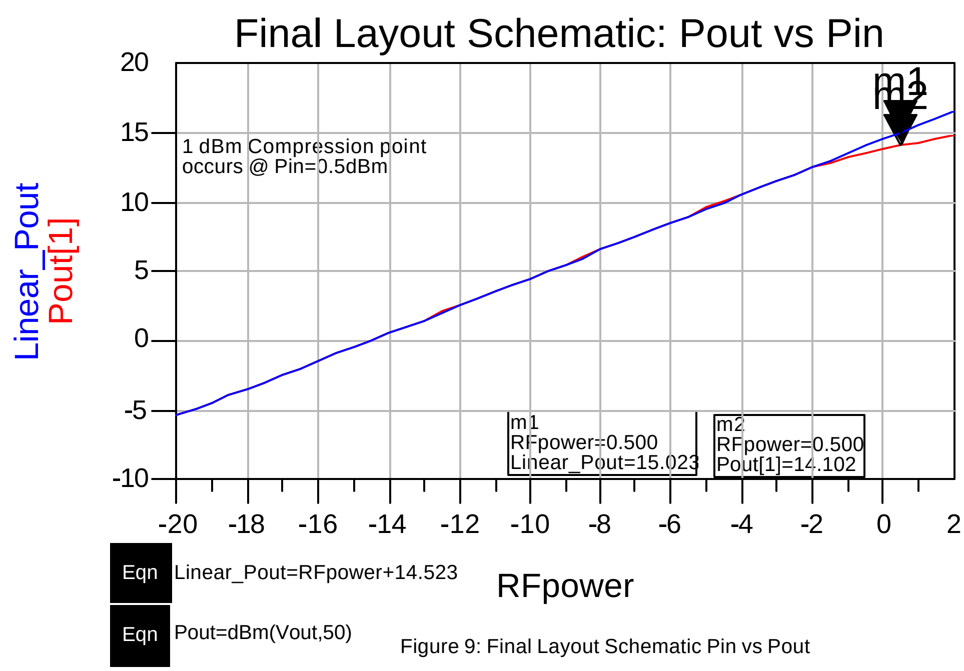


Figure 9: Final Layout Schematic Pin vs Pout

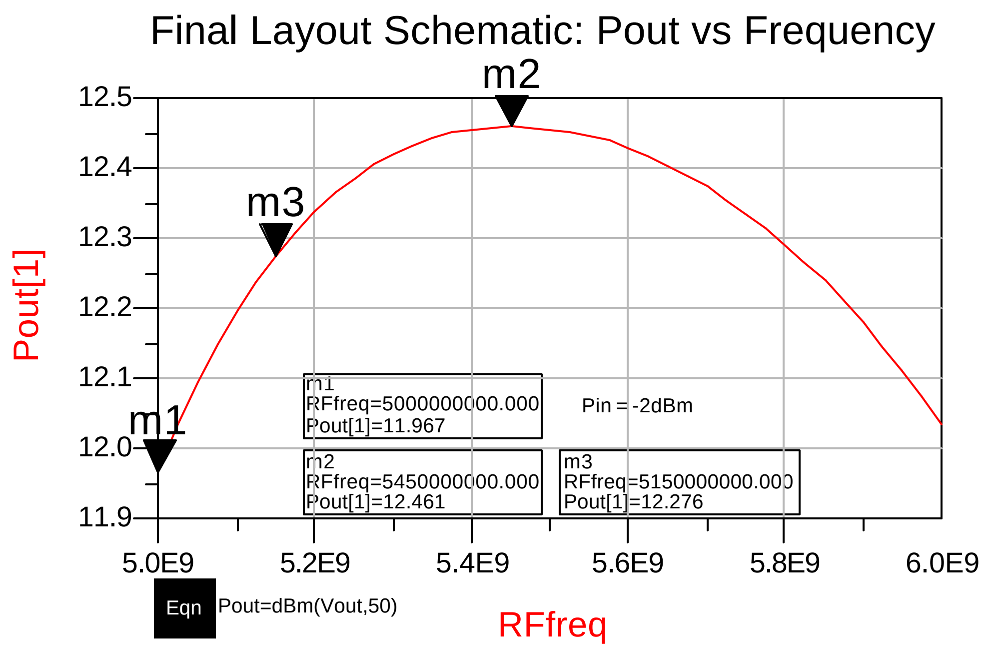


Figure 10: Final Layout Schematic Pin vs Frequency

## Schematic Diagrams

The following diagrams are the schematics used for the simplified and final layout.

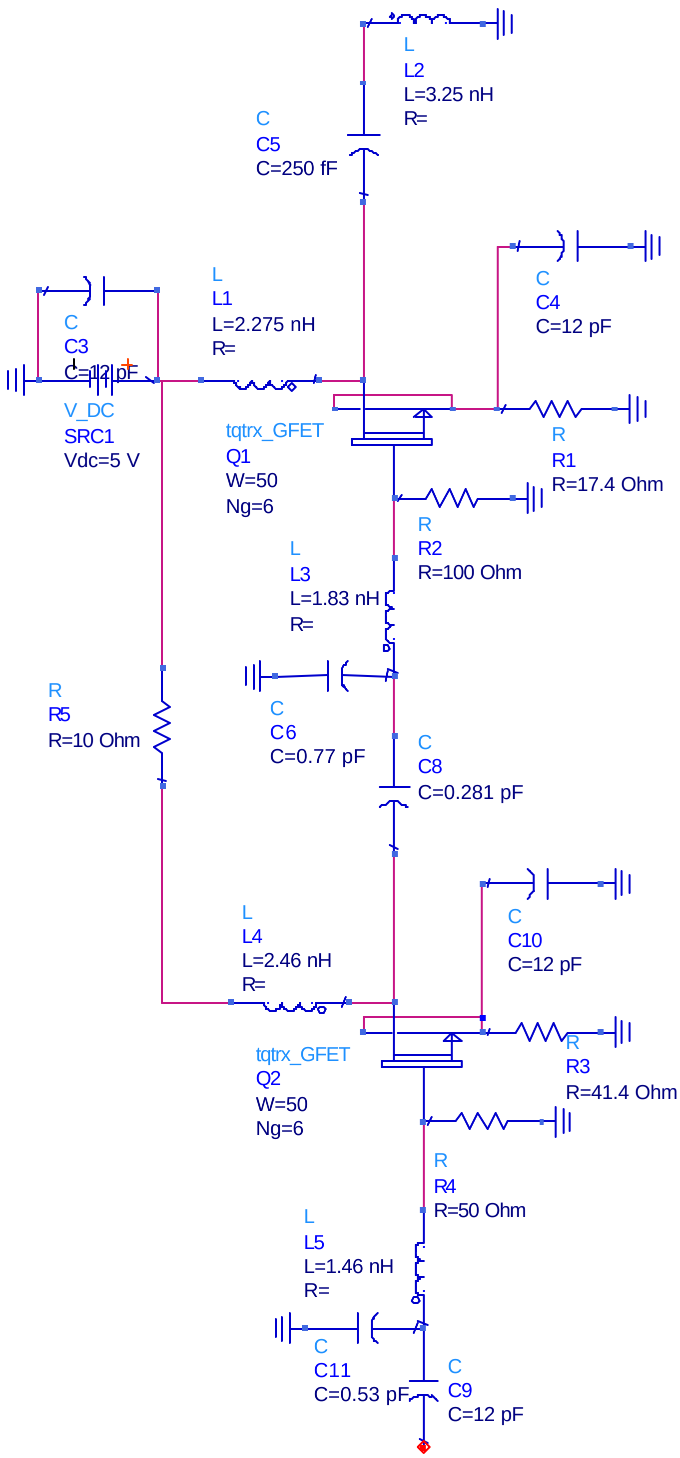


Figure 11: Simplified Schematic:

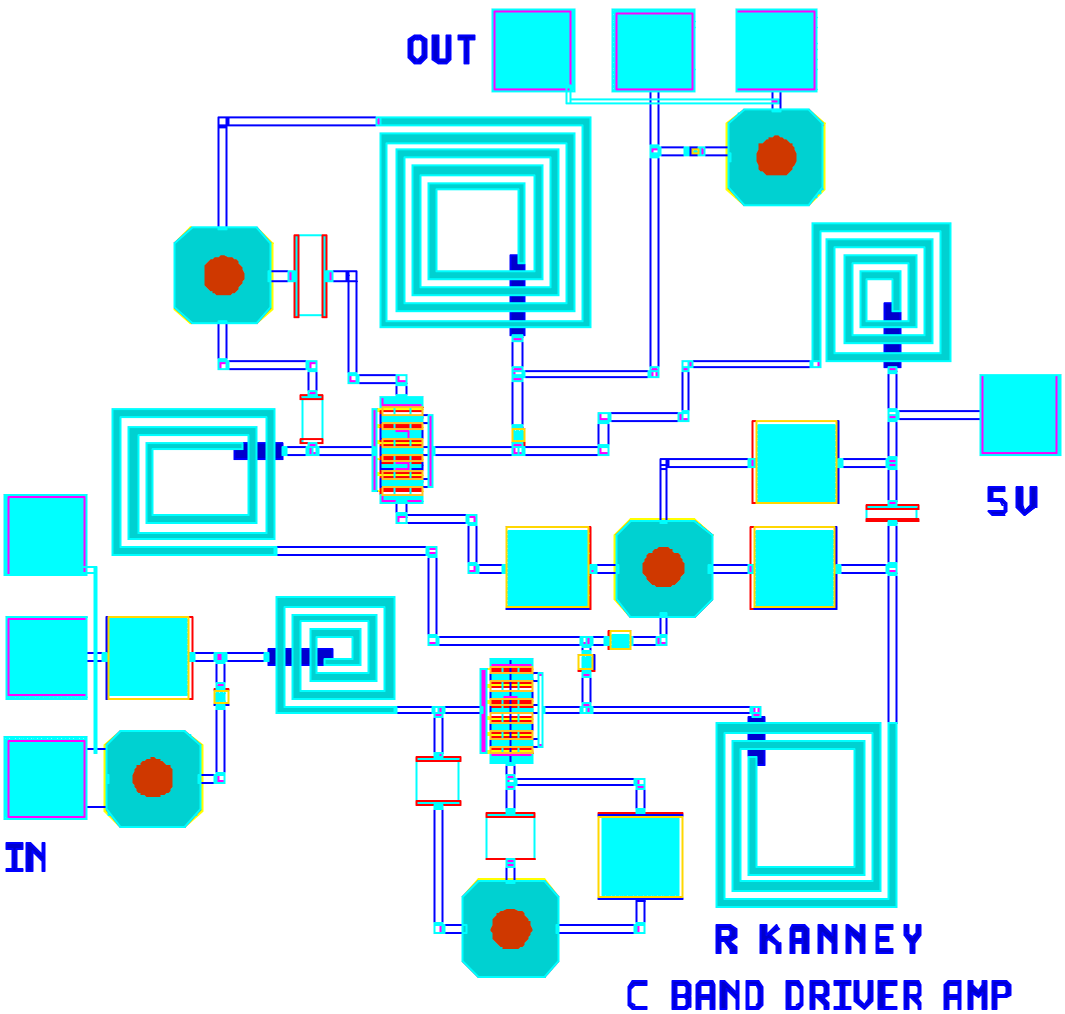


Figure 12: Final Layout Schematic

# DC Analysis

The following is the simplified DC schematic without inductors and microstrip. Also listed in the table below is the bias check.

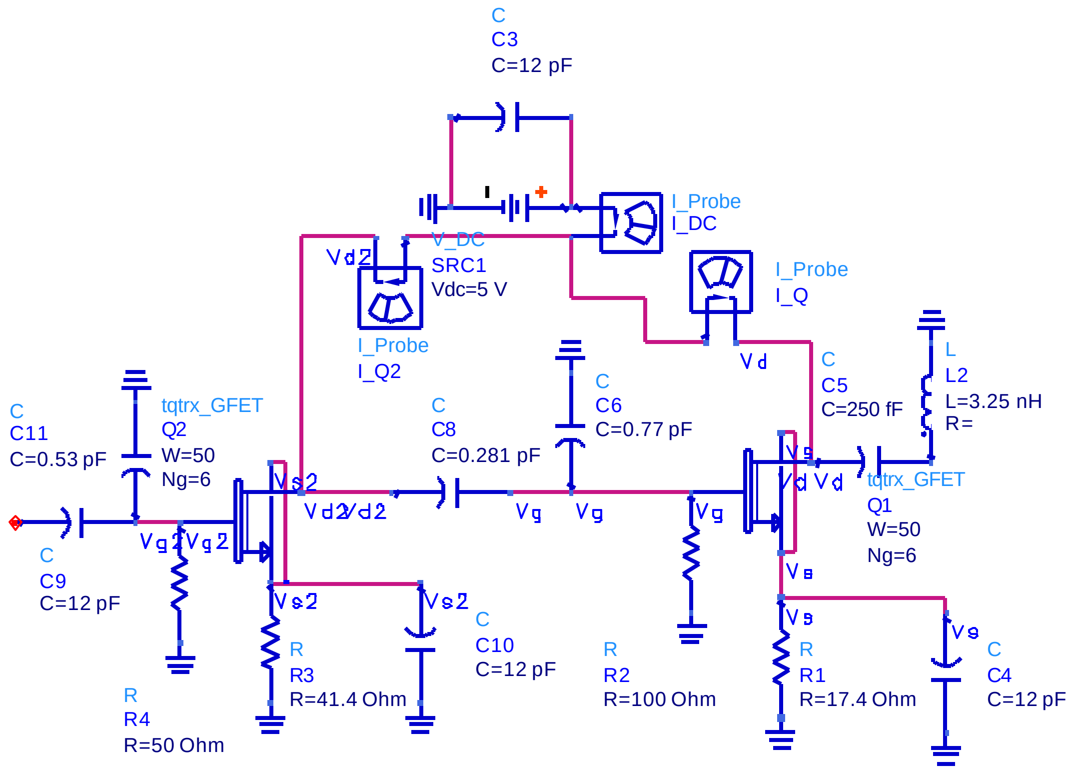


Figure 12: Simplified DC Schematic

### DC Bias Check

| | Stage 1 | Stage 2 |
|---|---|---|
| **Id** | 28.91mA | 45.85mA |
| **Vds** | 3.8V | 4.2V |
| **Vgs** | -1.2V | -0.8V |

All components in the circuit are capable of handling the currents presented to them.

# Test Plan

The following test procedures are recommended to test the C band driver amplifier.

## Linear Parameters

An Agilent 8510 network analyzer is needed to measure the s parameters of the amplifier. It is also recommended that a 20dB attenuator pad be placed on the 2$^{nd}$ port of the analyzer to protect it.

1. Connect a 20dB attenuator to port 2 of the network analyzer.
2. Calibrate the analyzer from 1GHz to 10GHz.
3. Place the bias probe on the pad of the chip labeled "5V".
4. Place probe tips on the designated pads. The input port is labeled "IN" and the output port is labeled "OUT".
5. Turn on the 5V power supply.
6. Record data.

## Power measurements

For power measurements it is recommended that a signal generator and spectrum analyzer be used.

1. Connect a 20dB attenuator to the input of the spectrum analyzer.
2. Connect the signal generator probe to the input pad of the amplifier chip, which is the port marked "IN".
3. Connect the spectrum analyzer probe to the output pad of the amplifier chip, which is the port marked "OUT".
4. Place the bias probe on the pad of the chip labeled "5V".
5. Turn on the 5V power supply.
6. For Pin vs Pout set the generator to the frequency of interest and sweep the power up to, but not exceeding, 4dBm. Record measurements from spectrum analyzer after each interval.
7. For Pout vs Frequency set the Generator to 0.5dBm. Sweep the frequency and record measurements from the spectrum analyzer after each interval.

## Conclusion & Recommendations

The C band amplifier design was a success and met and exceeded all of the specification goals except for output VSWR. Future recommendations on this design would include improving the output match to improve output VSWR and to take the power added efficiency more into account. Also, a resistor ladder should be added to the design to compensate for changes in device characteristics.