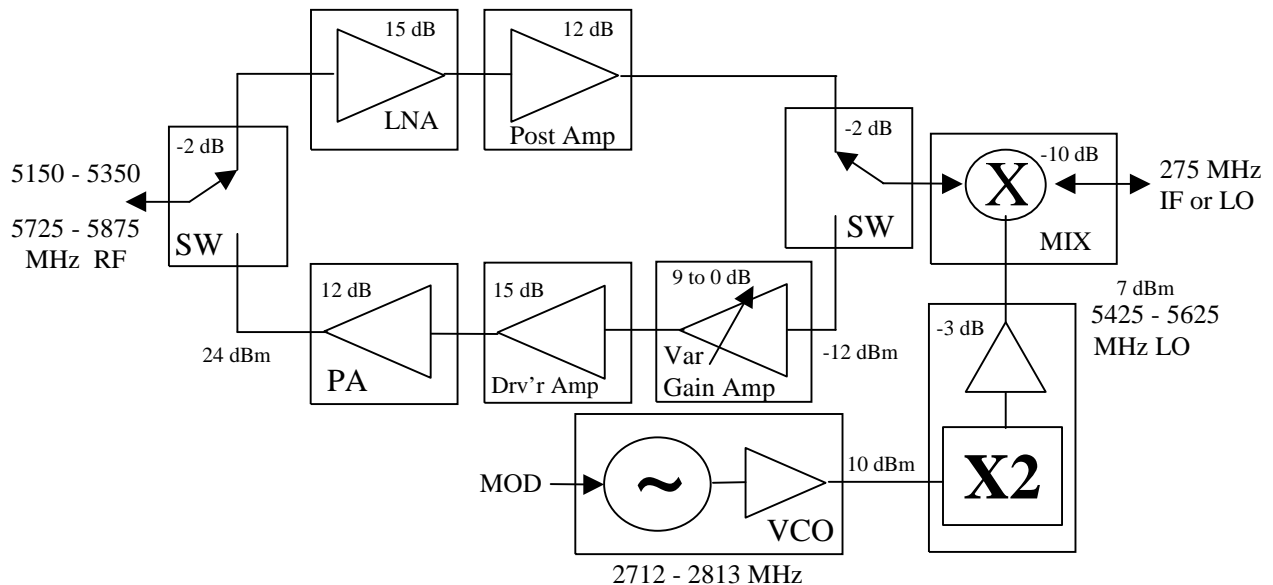


MMIC DESIGN EE 525.787 FALL 2001

STUDENT PROJECTS

This year's project for the MMIC Design class at The Johns Hopkins University is a simplex transceiver for the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies. The up-down conversion scheme uses a C-band frequency converter, which produces a 275 MHz IF signal that can be down converted to baseband with a 275 MHz second LO. The second LO is upconverted to C-band in the transmit mode. Modulation can be introduced onto the second LO or by direct frequency modulation of the VCO in the transceiver. The up-down converter consists of a mixer, VCO, and frequency doubler. The VCO operates from 2712 to 2813 MHz, which when doubled is between the WLAN and ISM frequencies. Thus, the VCO has dual band usage with high side or low side LO injection to the mixer. C-band SPDT switches are employed to route receive and transmit signals appropriately. The receive chain consists of an LNA and a post amplifier in cascade. The transmit path employs a variable gain amplifier for level control and a driver amplifier feeding a ¼ watt power amplifier. Nine unique MMIC designs make up the ten chip C-band transceiver. Each design is to be contained on a 60 mil square die in the TQS TRx process. The proposed block diagram is shown below.



Chip Set for the 5150 - 5350 MHz WLAN and
5725 - 5875 MHz ISM Bands

SPECIFICATIONS FOR C BAND LOW NOISE AMPLIFIER

*On chip high Q matching networks, source inductance
and FET size tuned for low noise with good input VSWR*

FREQUENCY:	5150 to 5875 MHz
BANDWIDTH:	> 725 MHz
GAIN:	> 15 dB
GAIN RIPPLE:	± 0.5 dB max.
NOISE FIGURE:	< 5 dB; 3 dB, goal
INPUT IP3:	> +5 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	± 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND POST AMPLIFIER

Two stage amplifier with on chip bias network and FET size tuned for efficient Class A power operation with good input & output VSWR

FREQUENCY:	5150 to 5875MHz
BANDWIDTH:	> 725 MHz
GAIN small signal:	> 12 dB; 15 dB, goal
GAIN RIPPLE:	± 0.5 dB goal
OUTPUT IP3:	> +20 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	± 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND POWER AMPLIFIER

*On chip drain and gate bias network, output matching network,
and FET size tuned for efficient Class F power operation with
good input & output VSWR*

FREQUENCY:	5150 to 5875 MHz
BANDWIDTH:	> 725 MHz
GAIN, small signal:	> 12 dB; 15 dB, goal
GAIN RIPPLE:	± 0.5 dB max.
OUTPUT POWER:	> +24 dBm @ 1 dB compression
EFFICIENCY:	> 20 % @ 1dB compression; 25 %, goal
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE:	+ 7 and -5 Volts
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND DRIVER AMPLIFIER

Two stage amplifier with on chip bias network and FET size tuned for efficient Class A power operation with good input & output VSWR

FREQUENCY:	5150 to 5875MHz
BANDWIDTH:	> 725 MHz
GAIN small signal:	> 12 dB; 15 dB, goal
GAIN RIPPLE:	\pm 0.5 dB goal
OUTPUT POWER:	> +13 dBm @ 1 dB compression
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	\pm 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND VARIABLE GAIN AMPLIFIER

One or two stage amplifier with on chip bias and gain control networks with good input & output VSWR

FREQUENCY:	5150 to 5875MHz
BANDWIDTH:	> 725 MHz
GAIN small signal:	9 dB to 0 dB, voltage variable
GAIN RIPPLE:	± 0.5 dB goal
OUTPUT POWER:	> +10 dBm @ 1 dB compression
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	± 5 Volts; + 5 Volts only, goal
CONTROL VOLTAGE:	0 to -5 Volts
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND UP / DOWN CONVERTER

*Lumped element hybrid for RF and LO,
external bias for starved LO operation.*

FREQUENCY: RF = 5150 to 5875 MHz; LO = 5425 to 5625 MHz;
IF=275 MHz

ISOLATION: LO/RF 10 dB min.; 16 dB goal

CONVERSION LOSS: 10 dB max.; 7 dB goal

LO POWER: +7dBm max 0 dBm goal

VSWR, 50 Ohm: 2.5:1 max.; 1.5:1 goal

SUPPLY VOLTAGE: Variable, 0 to 5 Volts

SIZE: 60 x 60 mil ANACHIP

SPECIFICATIONS FOR S BAND VOLTAGE CONTROLLED OSCILLATOR

On chip high Q resonator and tuning varactor.

FREQUENCY: 2712 to 2813 MHz

OUTPUT POWER: > +5 dBm; +10 dBm goal

CONTROL VOLTAGE: 0 TO -5 Volts

SUPPLY VOLTAGE: ± 5 Volts; +5 Volts only goal

OUTPUT IMPEDANCE: 50 Ohm, nominal

SIZE: 60 x 60 mil ANACHIP

SPECIFICATIONS FOR S/C BAND FREQUENCY DOUBLER

FET doubler with on chip matching for fundamental and third harmonic rejection.

FREQUENCY: OUTPUT = 5425 to 5625 MHz;
 INPUT=2712.5 TO 2812.5 MHz

CONVERSION LOSS: 3 dB max.; 0 dB goal

INPUT POWER: +10 dBm typ.

SPURIOUS: FUNDAMENTAL = 16 dBc min.; 25 dBc goal
 THIRD = 20 dBc min.; 30 dBc goal

VSWR, 50 Ohm: 2.5:1 max.; 1.5:1 goal

SUPPLY VOLTAGE: ± 5 Volts; + 5 Volts only, goal

SIZE: 60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND SPDT SWITCH

FET switch with on chip TTL driver and FET size tuned for 1/4 watt power operation with good input & output VSWR

FREQUENCY: 5150 to 5875MHz

BANDWIDTH: > 725 MHz

INSERTION LOSS: < 2 dB; 1.5 dB, goal

ISOLATION: > 20 dB

POWER HANDLING: > +24 dBm @ 1 dB compression

VSWR, 50 Ohm: < 1.5:1 input & output

SUPPLY VOLTAGE : \pm 5 Volts

CONTROL: TTL

SIZE: 60 x 60 mil ANACHIP

PROJECTS

Low Noise Amplifier - 15 dB gain, 3 dB NF

Post Amplifier – 12 dB Gain, +20 dBm IP3

Power Amplifier - 1/4 watt, 15 dB gain, class F

Driver Amplifier - 15 dB gain, +13 dBm output @ P1dB

Variable Gain Amplifier – 9 to 0 dB gain

Up/Down Converter – 275 MHz IF, 0 dBm LO power

Voltage Control'd Osc. - 2712 to 2813 MHz tuning range

Frequency Doubler – 3 dB Conversion Loss

SPDT Switch – 2 dB insertion loss, 20 dB isolation

GENERAL CONDITIONS

TriQuint:

TQTRx Process, with vias
4 mil (100 micron) thick wafer
60 x 60 mil die (ANACHIP)
TOM3 FET model in ADS

Testing:

Agilent 8510 VNA (45 MHz to 26 GHz)
Cascade Model 43 wafer probe station with
up to 4 RF probes & 4 DC needle probes
Synthesized signal generators to 26 GHz
Spectrum analyzer to 18 GHz