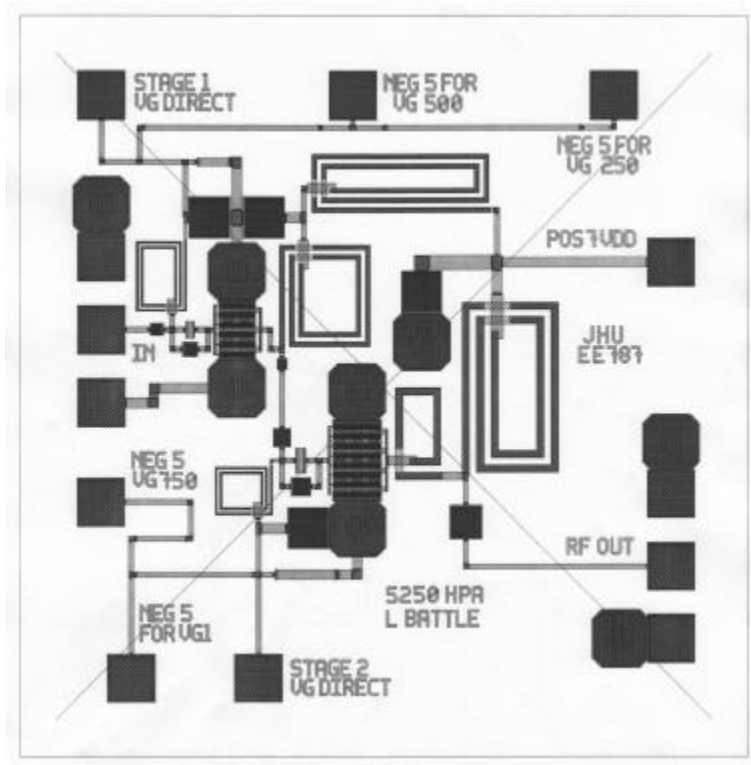


C Band Power Amplifier Design and Layout Using Agilent ADS and Triquint Element Library



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Abstract

The purpose of this exercise was to design a ¼ Watt C Band MMIC HPA utilizing Agilent/HP ADS software for eventual circuit fabrication by Triquint. Performance requirements were given for the design which included frequency range, gain, ripple, output power, and VSWR. Circuit layout was restricted to a standard 60x60 mil package. Class F operation was targeted for improved efficiency but was not realizable using standard Triquint elements within the allotted time. All other performance requirements were achieved using a two-stage design with Triquint GFET transistors. The complete design process included device selection, circuit design, circuit modeling and simulation, and physical layout. A test plan is included for testing of first unit to verify actual performance versus modeled performance.

Introduction

Performance requirements for the design are listed in Table 1.

Table 1 -- Design Requirements

Parameter	Design Requirement/Goal
Operating Frequency Range:	5150 to 5350 MHz
Bandwidth:	> 200 MHz
Gain:	> 12 dB (15 dB Goal)
Gain Ripple over Frequency:	± 0.5 dB
Output Power (P1dB):	> +24 dBm
Efficiency (Power Added Efficiency):	> 20% @ P1dB (25% Goal)
Input and Output VSWR:	< 1.5:1
Supply Voltage:	+7 V and -5 V
Physical Layout:	60 x 60 mil ANACHIP package with standard Triquint elements

The most restrictive parameters in the design were the overall 60x60 mil size restriction and the limitation of devices to standard Triquint elements. This restricted the design to Triquint EFET, DFET, or GFET transistors and restricted other passive elements and interconnects to a size that would fit within the chip outline when physically laid out. Initially, the second stage output matching network to achieve the design goal of Class F operation was to be implemented towards the end of the design process. However, the component and size restrictions hindered achieving this goal.

The design assumed two stages of cascaded gain were required to achieve the required gain of 12dB (15 dB goal). The second (output) stage was designed to provide maximum power output while the first (input) stage was designed for maximum gain. The design of the second (output) stage was selected as the starting point due to its influence on the critical output power performance requirement.

The second (output) stage was designed using a Cripps output match approach to maximize output power. The Triquint GFET type power transistor was selected and a range of device sizes were DC simulated to create series of DC Characteristic Curves. A 800 μm GFET (8 gate fingers x 100 μm per gate finger) size was selected to give voltage swing of 12 volts p-p (based on drain bias supply of +7 V) and peak current of 300 mA to achieve device limited output power of 450 mW (+26.5 dBm). Setting the bias to $I_{DS}=100$ mA was expected to yield an output power of 300 mW (+24.8 dBm). This operating point also had the advantage of requiring a $Z_I=62 \Omega$ for a Cripps match output. This would allow for a good compromise between achieving a maximum output power match (62 Ω) and a near ideal Z_o match (50 Ω). The nonlinear model was biased and an S-parameter simulation was performed to model the R_{ds} and C_{ds} of the device. Input series resistance was used to achieve unconditional stability from 0.5 GHz to 10.5 GHz (approximately twice normal operating frequency). Parallel capacitance was added to the input resistance to recover gain at higher frequencies while still maintaining a μ factor greater than one. Using the R_{ds} and C_{ds} model of the transistor and the required Cripps Z_I an output matching network (OMN) was designed with an integrated shunt inductance component for adding drain bias to the circuit. A new S-parameter simulation for the FET with OMN was used to generate a conjugate match input matching network (IMN) to maximize gain. A shunt inductor was also incorporated in the IMN for adding gate bias to the circuit. Simulation of the second (output) stage with ideal elements yielded 10.2 dB of gain and an output power (P1dB) of +26 dBm. Tuning of the circuit for improved performance was held until modeled Triquint elements were substituted for ideal elements for expediency in design.

Given the gain for the second stage of approximately 10 dB with a final target output power of +24 dBm for the cascaded circuit, a target minimum output power (P1dB) for the first (input) stage was determined

to be +14 dBm. In order to ensure that the first (input) stage would not compress before the second (output) stage and limit the overall amplifier, extra margin was added to the requirement for the device selection. A 450 μm GFET (6 gate fingers x 75 μm per gate finger) size was selected which had a device limited maximum output power of 250 mW or 24 dBm. Using the device with reduced bias (V_{gs}) and conjugate match for maximum gain, a more reasonable output power (P1dB) of approximately 18-20 dBm was assumed. This would operate the first (input) stage at a reasonable 4 dB back-off point even if the second (output) stage gain was reduced once Triquint modeled elements were substituted for ideal. This over sizing of the first stage would be at the expense of overall efficiency with the intention that future iterations of the design could reduce the device size to recover efficiency once other parts of the design are tested and proven. Input and output matching networks were designed using S-parameter simulation and the nonlinear model biased at the appropriate operating point. Shunt inductance components were integrated into both matching networks to allow for drain and gate bias to be added to the circuit. Simulation of the first (input) stage with ideal elements yielded 11.1 dB of gain and an output power (P1dB) of +22 dBm. Once again tuning of the circuit was deferred until Triquint modeled elements replaced ideal elements in order to reduce the number of tuning iterations.

Since the output of the first (input) stage as well as the input of the second (output) stage were both matched to 50 Ω , the two stages could be cascaded with no changes to the matching networks. Initial simulation of the complete cascaded circuit with ideal elements yielded gain of 21.5 dB at center band (5250 MHz) and output power (P1dB) of +26.1 dBm. Wide band simulation from 0.5 to 10.5 GHz verified stability remained unconditional for the new cascaded circuit.

With a complete cascaded circuit designed and simulated with ideal elements, the next step in the design was to verify physical layout within the package constraints was achievable. Triquint modeled inductors, capacitors, and resistors were generated in the layout mode along with the two GFET transistors and ground vias. Individual L and C Triquint components were sized based on comparison simulations with ideal elements as a starting point. Working without interconnecting traces the components were arranged to form an "paper doll" layout that approximated desired final layout. This activity confirmed that physical layout within package restrictions would be possible. Subsequent steps added transmission line interconnects and refined component placement trying to minimize the overall footprint while not violating design rules or placing components in such proximity as to create potential for undesired interactions. From this physical layout ADS generated a schematic for simulation. Going from layout to schematic presented some minor but relatively surmountable problems. Such an approach worked for this circuit but would not be advisable for more complicated circuit designs.

An initial simulation of the new cascaded circuit with Triquint modeled elements and interconnects revealed a noticeable reduction in gain and a larger than expected rise in the stability factor μ . Leaving the initial separate matching networks intact allowed for easy independent simulation of the first and second stages. After confirming high stability factors for each stage, the input stability resistance and capacitance values were adjusted to recover gain while still maintaining unconditional stability from 0.5 to 10.5 GHz. Further simulations adjusted matching network component values to optimize gain, output power, ripple, and VSWR performance. With acceptable performance, the bias networks were added and the final circuit was re-simulated to verify no bias circuit induced interactions.

At this point in the design the Class F matching network was attempted. The approach undertaken would create a short condition for the 2nd harmonic and an open condition for the third harmonic at the circuit output by the addition of a shunt L-C circuit. This would create the desired waveform shape of achieving maximum voltage and current swing while transitioning through a lower powered bias point (high voltage matched with low current, high current matched with low voltage). Initial simulations used ideal elements and yielded improved output power (P1dB) and efficiency (PAE) performance by 2-3 dB and 7-8% respectively. Unfortunately, attempts to realize the circuit with Triquint modeled elements failed since the required inductance at the 3rd harmonic (15.75 GHz) to generate the open condition appeared as capacitance due to self resonance of the spiral inductors. The only element architecture found to come close to the desired inductance (approximately 17 nH) at the required frequency was a spiral inductor of 1.25 or fewer turns that would encircle most if not all of the chip. Any simulations with Triquint modeled elements

continuously generated noticeably worse gain and efficiency at which time the Class F goal was abandoned. More on this issue is discussed in the conclusions section of this paper.

Modeled Performance

A summary of cascaded circuit performance including Triquint modeled elements and all interconnects is listed in Table 2. The performance data listed was generated using DC, S-Parameter, and Single Tone Harmonic Balance simulations using Agilent ADS software. Design requirements are also listed in the table and compliance with each requirement is indicated.

Table 2 -- Performance Summary and Compliance Matrix

Parameter	Design Requirement/ Goal	Simulated Performance (including Triquint elements and interconnects)	Performance Compliance
Operating Frequency Range	5150 to 5350 MHz	5150 to 5350 MHz	Compliant
Bandwidth	> 200 MHz	> 200 MHz	Compliant
Gain	> 12 dB (15 dB Goal)	21.5 dB at 5250 MHz center frequency	Compliant
Gain Ripple over Frequency	± 0.5 dB	± 0.25 dB	Compliant
Output Power (P1dB)	> +24 dBm	+25 dBm	Compliant
Efficiency (Power Added Efficiency)	> 20% @ P1dB (25% Goal)	19.6%	Not-Compliant*
Input and Output VSWR	< 1.5:1	1.4:1 (Input) 1.5:1 (Output)	Compliant
Supply Voltage	+7 V and -5 V	+7 V and -5 V	Compliant
Size	60 x 60 mil ANACHIP	60 x 60 mil	Compliant
Mode of Operation	Class F	Class A	Non-Compliant*

* **Non-Compliance for Efficiency and Mode of Operation** - Class F Operation was not achievable due to component restrictions at high frequencies (for reasons previously discussed in Introduction section of this paper). The mode of operation is the primary reason for efficiency non-compliance. A secondary reason for low efficiency is the over-sizing of transistors for the initial iteration of the design to ensure high output power performance.

Complete plots of simulation results are included on the following pages. Listed results include:

Figure 1 -- Simulation Results – Circuit With Ideal Elements (page 5)

- Power Added Efficiency
- Gain
- Dynamic Load Line
- Stability
- Input and Output Impedance (VSWR and Return Loss)
- Gain Compression

Figure 2 -- Narrowband Simulation Results - Triquint Elements and Interconnects (page 6)

- Gain
- Stability
- Gain Compression
- Input and Output Impedance (VSWR and Return Loss)
- Dynamic Load Line
- Power Added Efficiency

Figure 3 -- Wideband Simulation Results - Triquint Elements With Interconnects (page 7)

- Gain

- Stability
- Input and Output Impedance (VSWR and Return Loss)

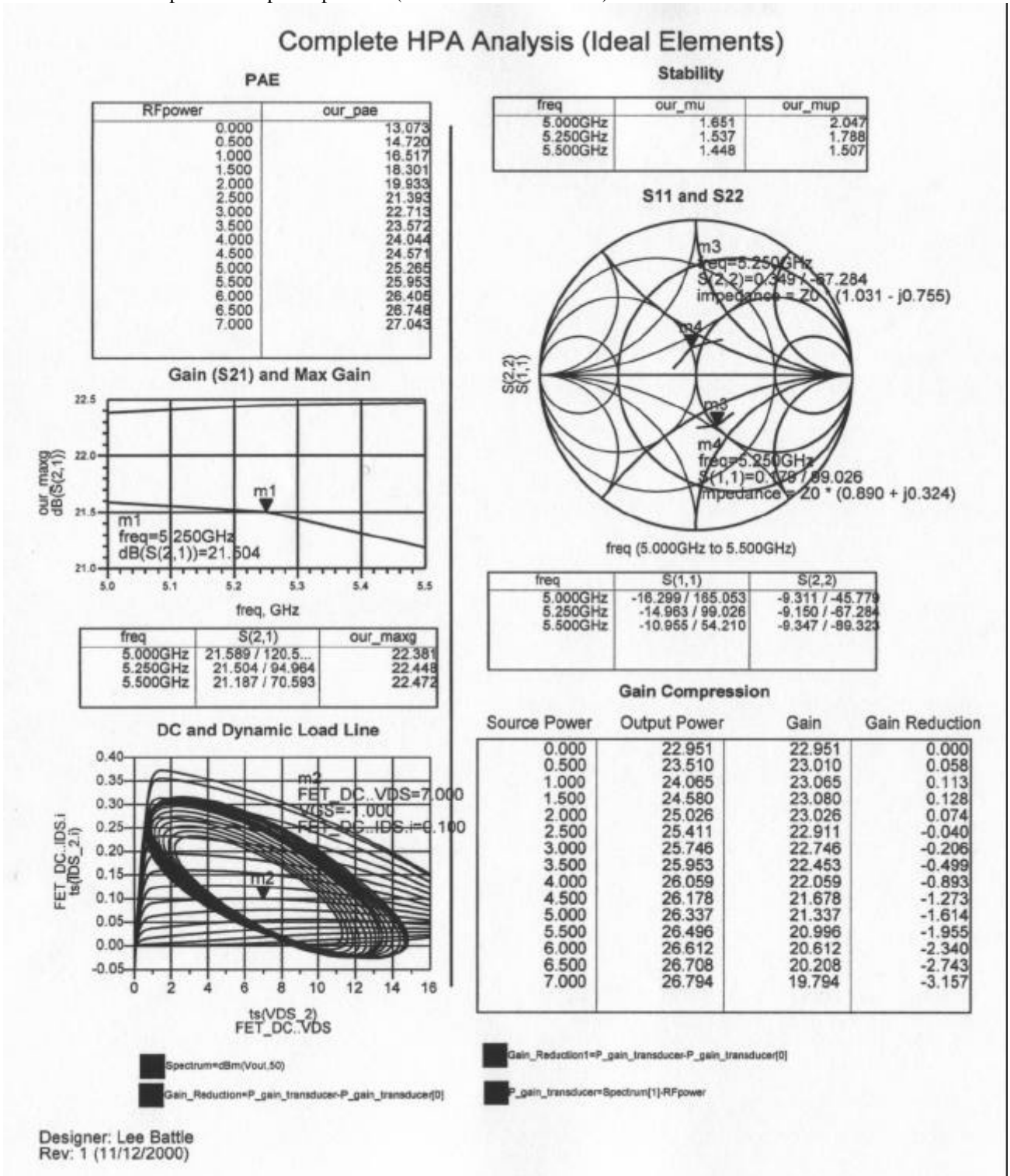
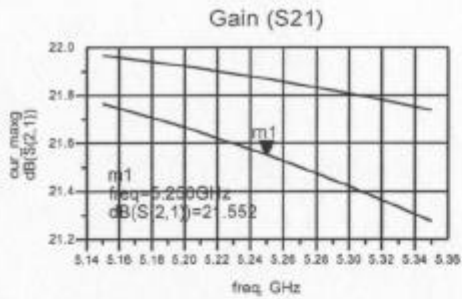


Figure 1 -- Simulation Results – Circuit With Ideal Elements

Complete HPA - Narrowband Analysis
(Triquint Elements and Interconnects)



freq	S(2,1)	our_maxg
5.150GHz	21.766 / 67.497	21.967
5.200GHz	21.668 / 61.345	21.922
5.250GHz	21.552 / 55.369	21.869
5.300GHz	21.421 / 49.567	21.808
5.350GHz	21.277 / 43.941	21.739

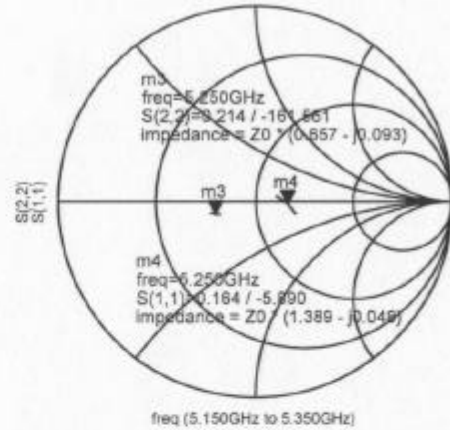
Stability

freq	our_mu	our_mup
5.150GHz	2.960	3.835
5.200GHz	2.639	3.447
5.250GHz	2.725	3.126
5.300GHz	2.621	2.870
5.350GHz	2.528	2.667

Output Power Compression (P1dB)

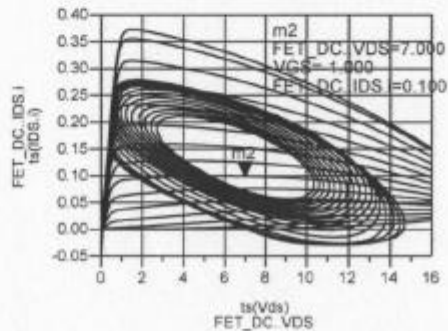
Source Power	Output Power	Gain	Gain Reduction
-3.000	19.752	22.752	0.000
-2.500	20.292	22.792	0.040
-2.000	20.836	22.836	0.084
-1.500	21.379	22.879	0.127
-1.000	21.918	22.918	0.166
-0.500	22.441	22.941	0.189
0.000	22.934	22.934	0.162
0.500	23.384	22.884	0.132
1.000	23.797	22.797	0.045
1.500	24.175	22.675	-0.078
2.000	24.489	22.489	-0.263
2.500	24.738	22.238	-0.515
3.000	24.984	21.984	-0.768
3.500	25.242	21.742	-1.011
4.000	25.379	21.379	-1.373
4.500	25.434	20.934	-1.818
5.000	25.476	20.476	-2.277

Input and Output Match - Return Loss



freq	S(1,1)	S(2,2)
5.15GHz	-19.45 / 14.51	-14.56 / -1.58E2
5.20GHz	-17.35 / 2.68	-13.95 / -1.60E2
5.25GHz	-15.69 / -5.89	-13.39 / -1.62E2
5.30GHz	-14.37 / -12.88	-12.88 / -1.63E2
5.35GHz	-13.29 / -18.39	-12.43 / -1.65E2

Dynamic Load Line Output Stage



Efficiency

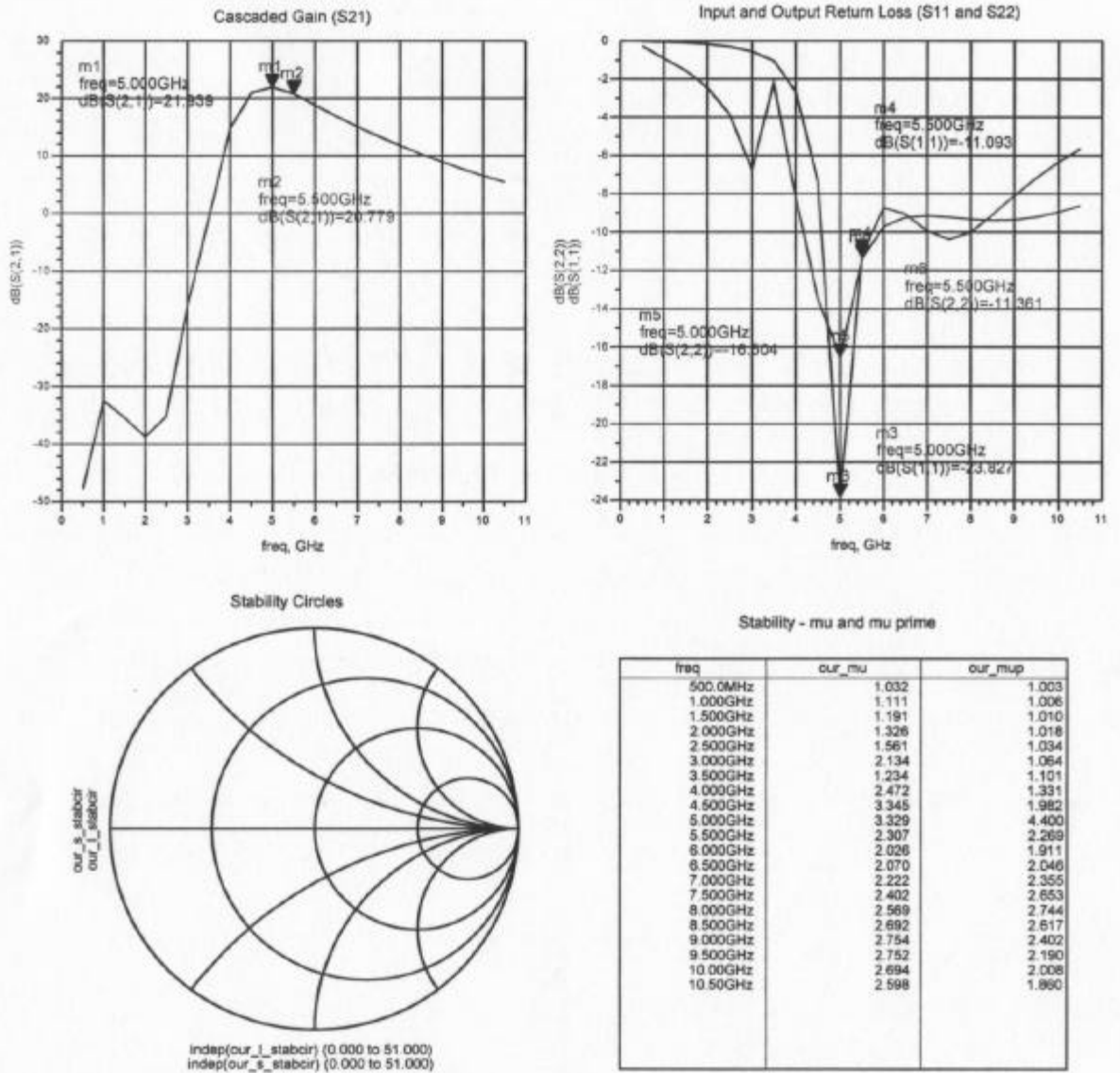
RFpower	our_pae
-3.000	5.740
-2.500	6.484
-2.000	7.325
-1.500	8.273
-1.000	9.328
-0.500	10.477
0.000	11.685
0.500	12.914
1.000	14.158
1.500	15.412
2.000	16.653
2.500	17.961
3.000	19.575
3.500	21.200
4.000	22.127
4.500	22.615
5.000	22.985

Spectrum=dBm(Vout,50) Gain_Reduction=P_gain_transducer-P_gain_transducer Gain_Reduction=P_gain_transducer-P_gain_transducer P_gain_transducer=Spectrum(1)-RFpower

Designer: Lee Battle Filename: Final Narrow 12/4/2000

Figure 2 -- Narrowband Simulation Results - Triquint Elements and Interconnects

Complete HPA - Wideband Analysis
(Triquint Elements and Interconnects)



Designer: Lee Battle Filename: Final Wide 12/4/2000

Figure 3 -- Wideband Simulation Results - Triquint Elements With Interconnects

Schematics and Layout Diagrams

Schematics and a layout diagrams for the complete circuit are included on the following pages. Diagrams and details for each are as follows:

Figure 4 -- Simple Schematic (no interconnects) (page 9)

This schematic includes all circuit elements using Triquint equivalent models. Microstrip interconnects have been omitted to simplify schematic viewing. The schematic illustrates the RF signal input at the left and RF signal output at the right. Circuit bias is provided using a common +7 V drain bias connection and individual gate bias connections. Connections are provided for fixed value gate bias (V_{gs}) using resistor divider networks and a fixed -5 V DC supply or a direct connection can be used to provide variable gate bias (V_{gs}) using an adjustable DC supply.

Figure 5 -- DC Schematic (no interconnects and inductors) (page 10)

This schematic illustrates a DC equivalent of the circuit including bias supply voltages and replacing inductors with equivalent DC shorts. Node voltages and currents are indicated from ADS simulation. Actual gate and drain voltage and drain-source currents have been highlighted (Note that an error exists in second stage gate bias schematic labels - connection port for $V_{gs}=-1.0$ actually provides -0.75 and alternate bias port for $V_{gs}=-0.75$ actually provides -1.0 - the labeling is correct in actual layout).

Figure 6 -- Final Layout (page 11)

This figure illustrates the final layout of the complete two-stage HPA. All connection ports are labeled appropriately.

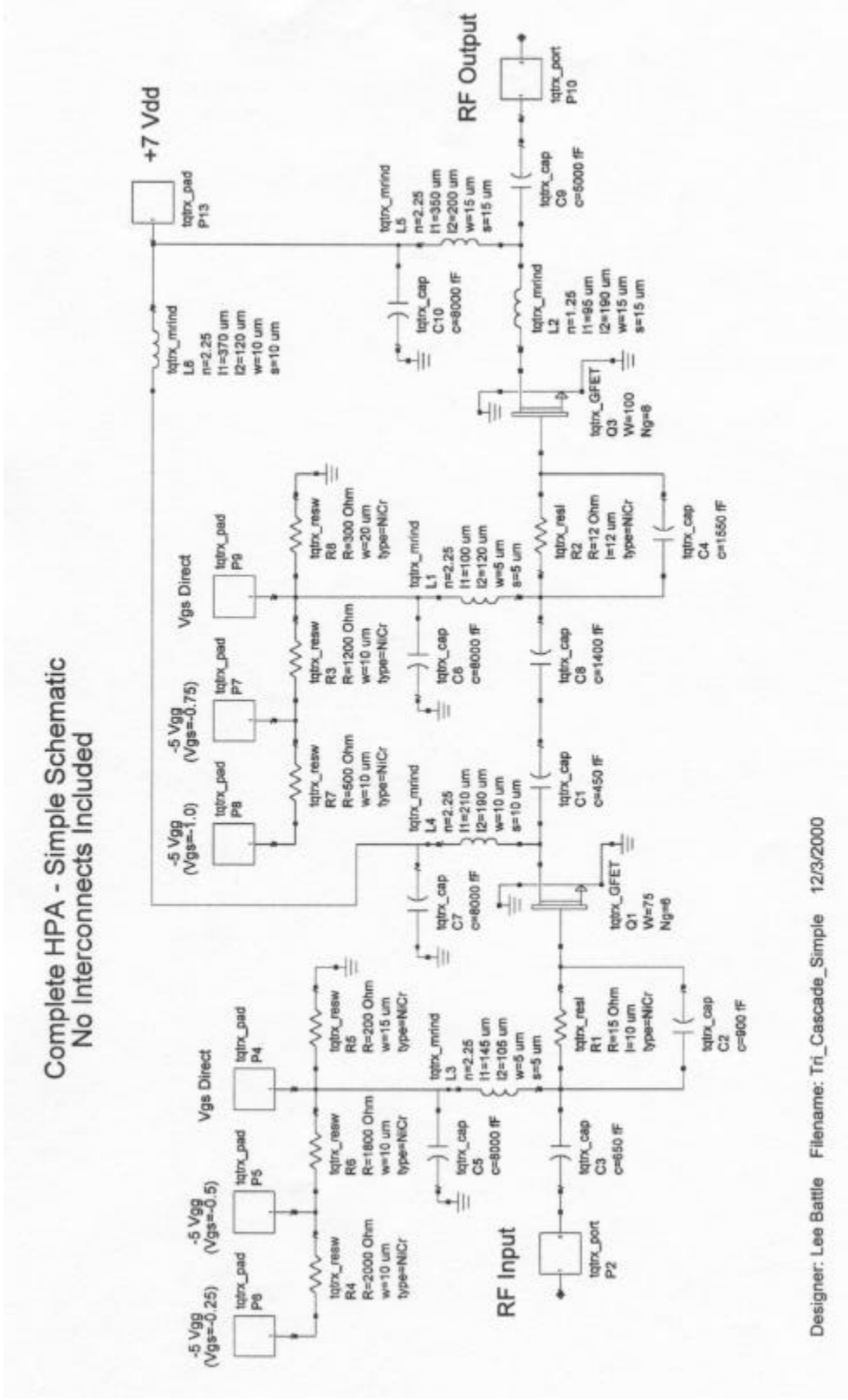


Figure 4 -- Simple Schematic (no interconnects)

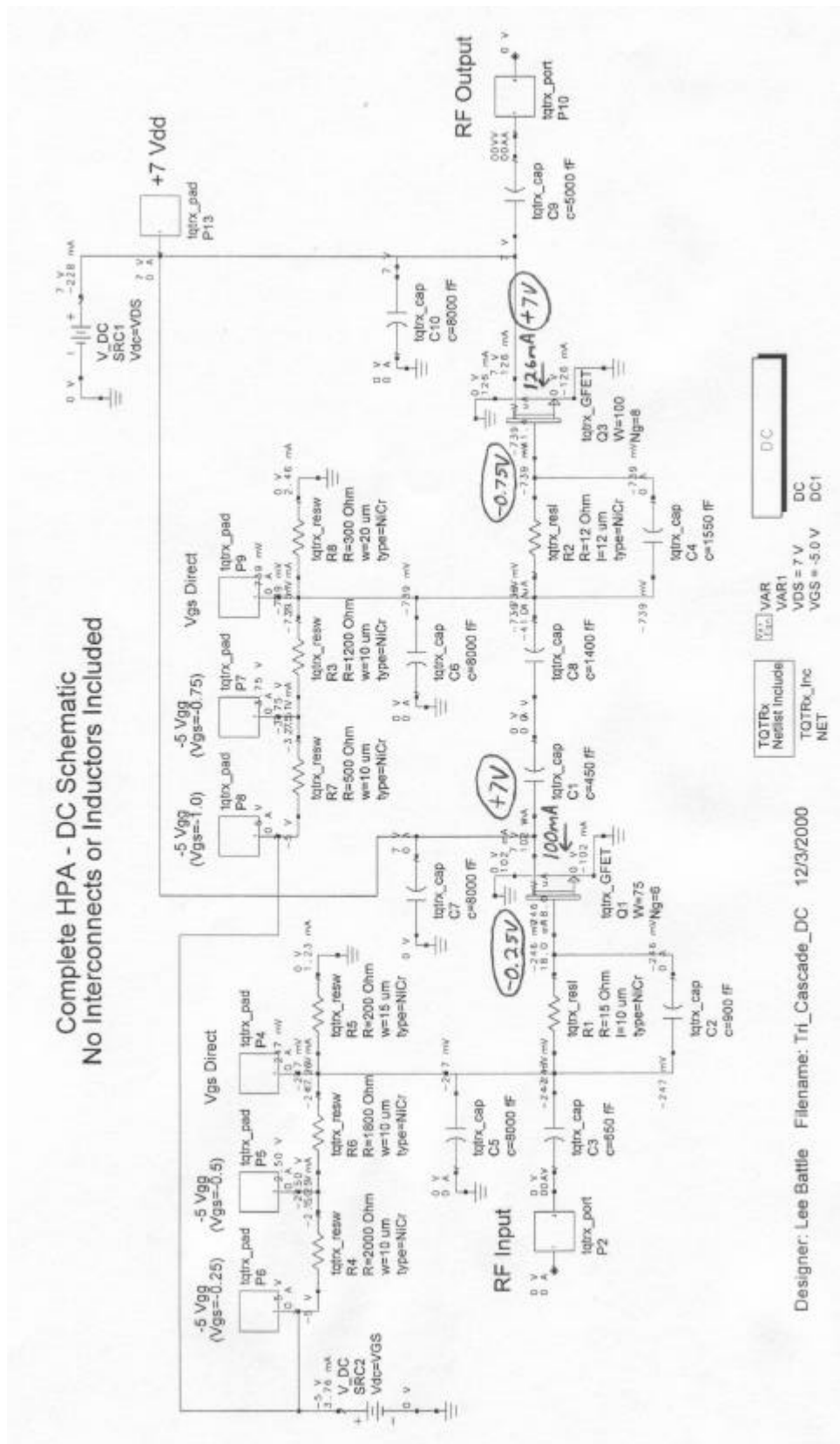


Figure 5 -- DC Schematic (no interconnects and inductors)

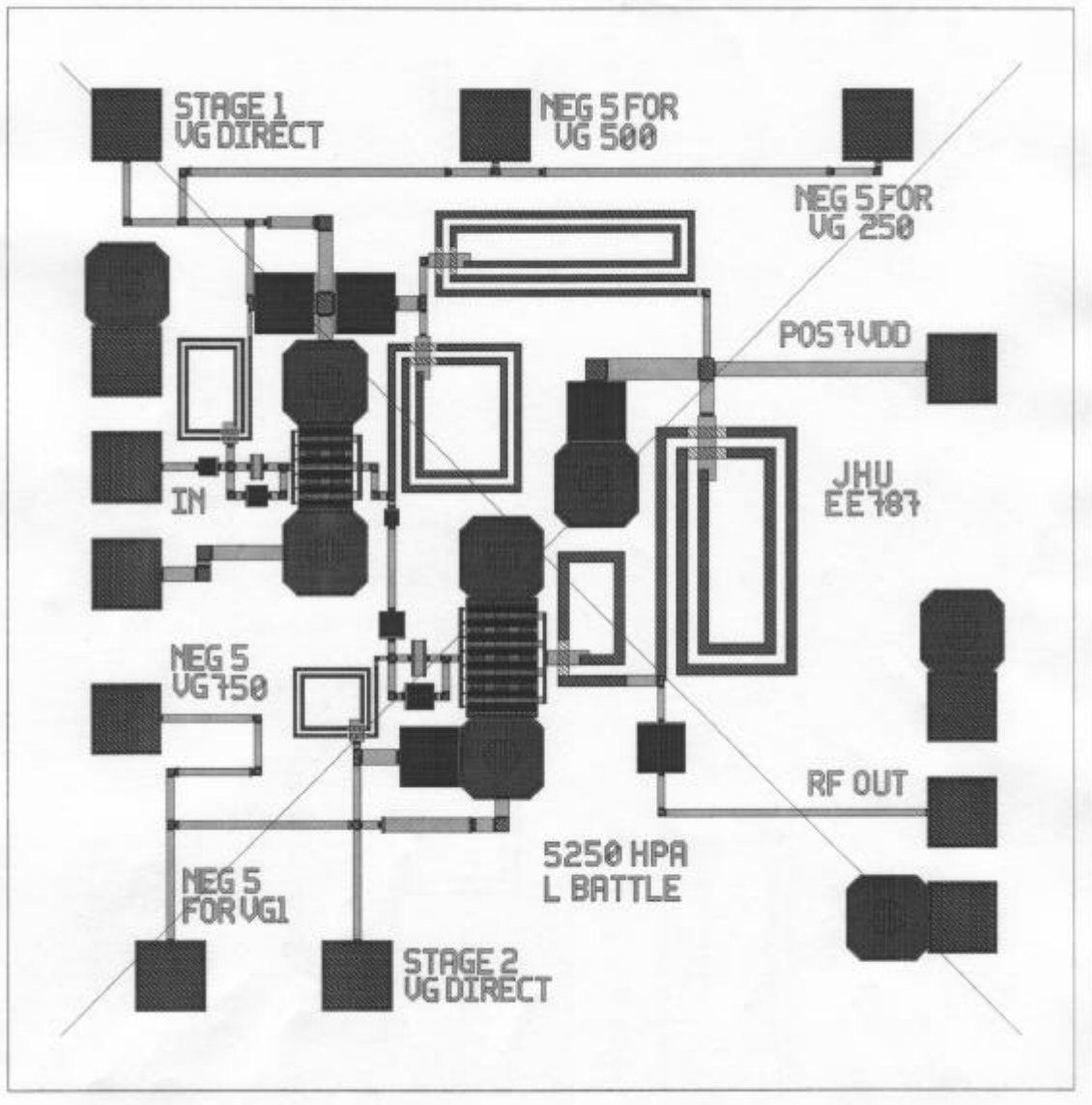


Figure 6 -- Final Layout

Test Plan

This section outlines the test plan for test of measurement of actual circuit after fabrication.

Equipment required

- Wafer probe station to provide connection capability to circuit under test
- Network analyzer with appropriate cables and calibration standards
- DC power supply for applying circuit bias
- DC voltage and current measurement equipment

Visual Inspection Testing

Purpose: To identify any visually obvious errors or defects prior to applying power to circuit and attempting performance measurements.

Setup: Requires inspection of circuit under test using wafer probe station.

- Procedure:**
1. Install the circuit under test into the wafer probe station (if not already installed)
 2. Visually inspect the circuit and compare to paper plot of layout generated during design phase. Verify proper circuit is to be tested and no obvious errors or defects exist (inverted circuit elements, missing elements, fabrication defects).

DC Testing

Purpose: To verify proper DC operation including verification of bias voltage and currents

Setup: Requires connection to circuit under test using wafer probe station, application of appropriate DC voltages with power supplies, and DC voltmeter/ammeter probe.

- Procedure:**
1. Install the circuit under test into the wafer probe station (if not already installed)
 2. Apply +7V DC to +7 Vdd connection port on circuit. Apply -5V DC to first stage -5 Vgg ($V_{gs}=-0.25$) connection port. Apply -5V DC to second stage Vgs Direct connection port (this will set second stage to pinch-off)
 3. Measure and record +7 Vdd current consumption and compare with expected (100 mA). Measure and record actual first stage Vgs voltage and compare with expected (-0.25 V)
 4. Repeat procedure placing first stage into pinch-off and applying -5V to appropriate connection ports (for $V_{gs}=-0.75$ V). Measure and record actual current and voltage and compare with expected values.
 5. Apply -5 V to appropriate bias connections for both first and second stage for normal operation. Measure and record actual total current consumption and compare with expected value.

Swept Frequency Testing

Purpose: To measure small signal circuit performance using a single tone, swept frequency input signal at a fixed power level.

Setup: Requires connection to circuit under test using wafer probe station, application of appropriate DC voltages with power supplies, and input signal injection and output signal measurement using a network analyzer.

- Procedure:**
1. Install the circuit under test into the wafer probe station (if not already installed). Apply appropriate DC bias to circuit.
 2. Setup and calibrate network analyzer for a narrow band frequency sweep from 5.0 to 5.5 GHz with a signal power level of approximately 0 dBm and connect analyzer to appropriate amplifier signal ports.
 3. Measure and record S-parameter performance and compare to expected values. Repeat measurements for different bias conditions if desired.
 4. Setup and calibrate network analyzer for a wide band frequency sweep from 0.5 to 10.5 GHz (or as restricted by test equipment) with a signal power level of approximately 0 dBm.
 5. Measure and record S-parameter performance and compare to expected values. Repeat measurements for different bias conditions if desired.

Swept Power Testing

Purpose: To measure circuit performance using a single tone, swept power input signal at a fixed frequency.

Setup: Requires connection to circuit under test using wafer probe station, application of appropriate DC voltages with power supplies, and input signal injection and output signal measurement using a network analyzer.

- Procedure:**
1. Install the circuit under test into the wafer probe station (if not already installed). Apply appropriate DC bias to circuit.
 2. Setup and calibrate network analyzer for a power sweep from -3.0 dBm to +4.0 dBm frequency of 5.25 GHz and connect analyzer to appropriate amplifier signal ports.
 3. Measure and record gain compression performance and compare to expected values. Repeat measurements for different bias conditions if desired. Measurements can also be made over other swept power ranges if desired.

Conclusions and Recommendations

Dependant upon results from actual circuit measurement, a second iteration of the design could improve a few areas. One area for possible improvement would be reevaluating the size of the particular transistors used. If actual measured data indicates margin in output power capability, the devices could be resized and/or bias changed to reduce the DC power consumption and improve efficiency. Also, matching networks could be tuned based on measured data to improve input/output match and an inter-stage matching network could be developed to possibly eliminate some components and reduce overall circuit footprint. A new attempt could be made at achieving Class F operation by trying one of three approaches. The first approach would be to develop a different circuit topology that does not require such a large value of inductance at the 2nd and 3rd harmonic frequencies. A second approach would be to consider use of an off chip inductor. This would help achieve the desired inductance value but possibly introduces some new problems related to packaging and proximity of matching network to transistor output. A third approach would be to consider Class F matching network requirements simultaneously with impedance and power capability when sizing the FET device. This may yield better results since the value of inductance needed for the matching network is proportional to the modeled R_{ds} and C_{ds} transistor values.

The design effort was considered successful since the majority of the design goals were achieved within the given time period. Goals not achieved include Class F operation and power added efficiency due mostly to difficulties realizing the desired circuit topology using the modeled elements. Aside from those requirements, all other design goals were achieved in some instances with respectable margin. The most difficult challenge to overcome during the design process was related to learning HP ADS software and gaining access to design equipment (computer lab). Quite a few years have passed since this designer has used this particular simulation package not to mention the various changes and updates that have occurred during that time. Accessing the simulation software and workstation while maintaining normal working hours at my job was difficult. This problem was somewhat alleviated when weekend hours became available.