

C BAND MMIC UP/DOWN
CONVERTER FINAL REPORT

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Abstract

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The need for Monolithic Microwave Integrated Circuit (MMIC) mixers that can operate as both up and down converters for a HIPERLAN 5.2 chip set is the driving force behind this work. This paper introduces a novel approach to the design and development of a MMIC C band up/down converter that fits on a 60 x 60 mil chip. The goals are to convert a 350 MHz IF up to 5150 to 5350 MHz RF with an LO of 4800 to 5000 MHz. The mixer must also be able to mix the RF frequencies down to an IF frequency of 350 MHz. Bias supply to the diodes are used for starved LO operation while a lumped element hybrid is used for supplying signals to the mixing diodes.

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GLOSSARY

DFET. TriQuint Semiconductor D-Type Field Effect Transistor

IF. Intermediate Frequency

LO. Local Oscillator

MMIC. Monolithic Microwave Integrated Circuit

MIM. Metal Insulated Metal

MLIN. Microstrip Line

MTEE. Microstrip Tee Interconnection

NiCr. Nickel Chromium

RF. Radio Frequency

Chapter 1

INTRODUCTION

This chapter introduces a description of the circuit as well as the design philosophy used to select the circuit topology and the trade-offs associated with this selection.

Circuit Description

The circuit topology selected is a 180-degree hybrid rat race mixer, with shunt FET diodes. The mixer is comprised of a lumped element 180-degree hybrid and 100 μ m DFETs with the drain and source tied together to form a schottky diode.

The local oscillator (LO) is applied to the shunt DFET diodes through a 180-degree lumped element hybrid where the LO signal is injected into the hybrid port and splits the LO into a 180-degree phase difference between the two shunt DFET diodes. RF and IF ports share the same port of the lumped element hybrid. The signals for the RF and IF are separated by using a simple inductor-capacitor high pass filter structure for the RF port and the IF port uses a low pass filter structure.

Bias is easily supplied to the DFETs through a bias line since the DFET diodes are in a shunt configuration. The bias voltage is divided with a pair of NiCr resistors in a voltage divider configuration in order to ease the power supply requirements when fine-tuning to lower voltages.

Design Philosophy

The design philosophy was driven by several factors. The first is the available choices of mixer circuits could be used in order to perform both up conversion and down conversion. This leads to selection of the popular double balanced mixers or the rat race mixer since 90-degree hybrid mixers can only mix up or down based on the orientation of the diodes.

The second criterion was which of the remaining choices would satisfy the other requirements. Since the double balanced mixer would require two more diodes than the 180-degree hybrid mixer, the LO requirements would be greater as well as the bias supply requirements. The double balanced mixer would also require baluns that would exceed the size specification of a 60 x 60 mil ANACHIP.

Therefore, the proper selection was that of a 180-degree lumped element hybrid rat race mixer. The classic approach is to tie the other side of the diodes together to form the IF port of the mixer. This however would make the routing more difficult since the diodes would be at opposite corners of the hybrid. To tie them together would require routing under or over the RF port of the mixer on the MMIC.

Therefore, a novel approach was taken were the DFET diodes would be used in a shunt configuration. This placed the IF port at the same port as the RF where by the phase and power between the diodes would be 0-degrees and evenly split.

Trade-Offs

The trade-offs of this approach are several. First the impedance matching of the DFET diodes at their bias condition greatly affects the VSWR of the 180-degree hybrid. Varying the bias of the DFET diodes moves the VSWR of the LO, RF, and IF match around. Baluns used in a double balanced configuration would

have better VSWR as opposed to a singly balanced 180-degree mixer whose VSWR is dependent on the diode match.

Second the port-to-port isolation is also dependent on the filters as opposed to that of a doubly balanced mixer. The LO to RF isolation however is equal to that of the hybrid isolation as evident in the compliance matrix. Since size was an important specification, the double balanced mixer was too large.

The shunt diode mixer on the other hand had several good trade-offs opposed to the classic hybrid mixer approach. The first is that the IF filter would have been necessary in the classic approach as well so no extra space was required. The shunt diode approach also provided a means of placing the DFET diodes at the corners of the hybrid without routing over or under the RF port. And finally, the injection of the bias for the starved LO was easy to achieve using shunt DFET diodes.

Since the conversion loss was greater than the specification, better matching for the DFET diode impedances over a larger range of bias conditions may be necessary to improve performance.

Chapter 2

MODELED PERFORMANCE

This chapter begins with the specification compliance matrix and then looks at plots of the simulated performance. The plots for the final layout version of the chip are illustrated.

Specification Compliance Matrix

The following table is the specification compliance matrix. All of the specifications were met except for the conversion loss, which was about 1 dB higher. Several of the goals were also reached in the design of this MMIC mixer.

Table 1. Compliance Matrix

Description	Specification	Design Goal	Simulated
Frequency	RF = 5150 to 5350 MHz	RF = 5150 to 5350 MHz	RF = 5150 to 5350 MHz
	LO = 4800 to 5000 MHz	LO = 4800 to 5000 MHz	LO = 4800 to 5000 MHz
	IF = 350 MHz	IF = 350 MHz	IF = 350 MHz
Isolation (LO/RF)	10 dB min.	16 dB	16 dB typical

Conversion Loss	10 dB max.	7 dB	11 dB typical
LO Power	+10 dB max.	+7 dB	+10 dB
VSWR, 50 Ohm	2.5:1 max.	1.5:1	1.6:1 RF 1.5:1 LO 2.3:1 IF
Supply Voltage	0 to +5 V	0 to +5 V	+2.8 V typical
Size	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP

Predicted Performance

This section begins with Figure 1, which shows the final layout simulated performance of the 180-degree hybrid. The port labeled S11 is the LO port, port S33 is the RF port, and ports 2 and 4 are the DFET diodes. The phase difference between the DFETs is about 180 degrees from the LO port. The power division between the RF/LO ports and the DFET diodes is around 3 dB.

The Hybrid layout uses the TriQuint elements such as spiral inductors, MIM capacitors, MLIN, and MTEE interconnections.

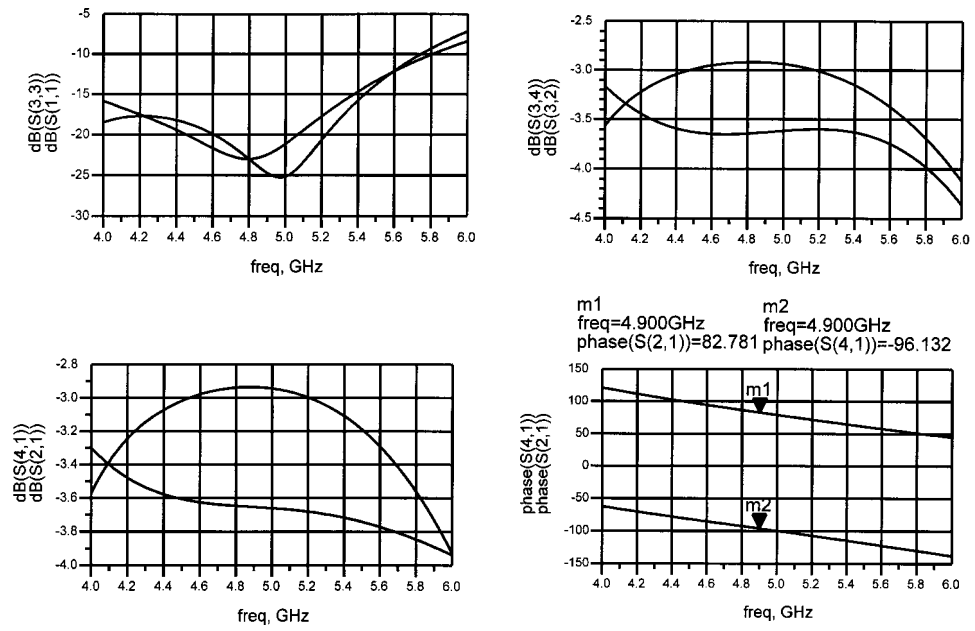


Figure 1. Final Hybrid

Figure 2 shows the simulated plots of the RF and IF filters used to separate the RF and IF signals that share the same port of the mixer.

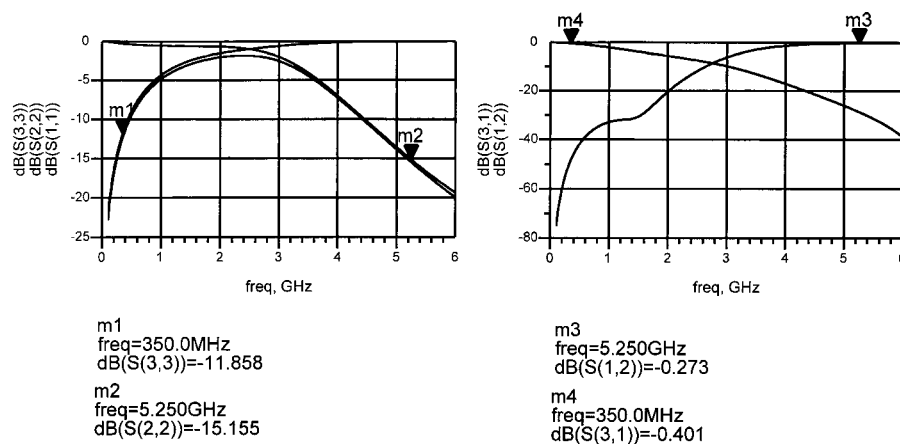


Figure 2. RF/IF Filters

Figure 3 shows the match and hence the compliance with the VSWR specification for the final layout of the mixer. This plot was obtained by setting the DC bias at around 0.7 V drops across the DFET diodes.

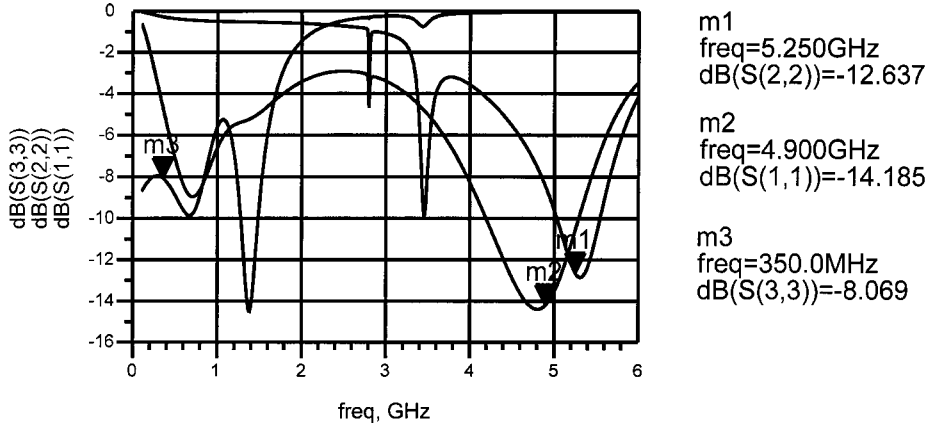


Figure 3. Mixer Match

Figure 4 shows a close up of the mixer matches at the RF, LO, and IF ports. The match is broad enough that slight variations in processing should still maintain the desired match at the ports.

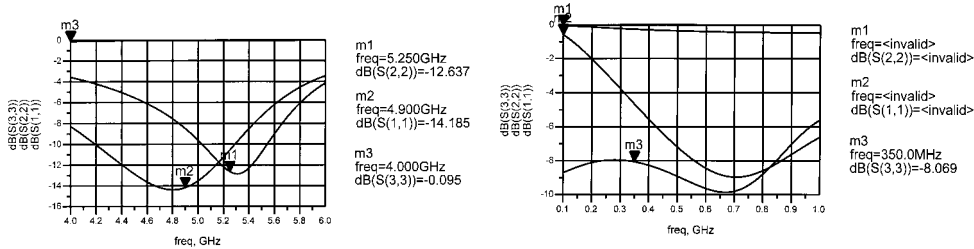


Figure 4. Port Matches

Figures 5, 6, and 7 show the mixer conversion loss and frequency spectrum for the low band, mid band, and high band response of the mixer as a down

converter. This was simulated using an LO power of +10 dBm and an RF input power of -20 dBm.

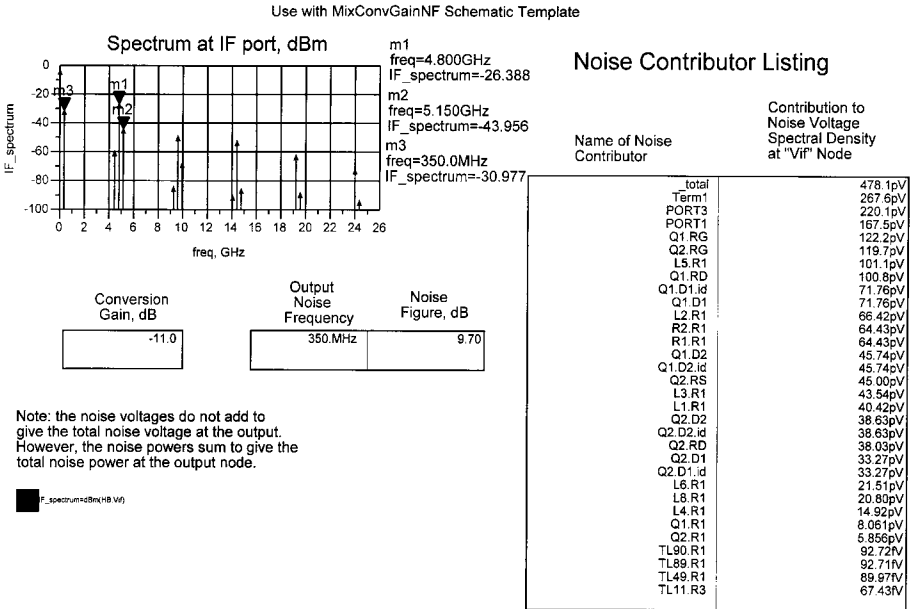
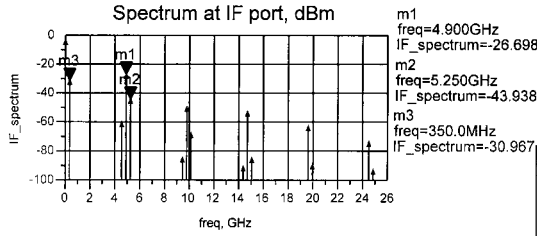


Figure 5. Down Converter (Low Band)

Use with MixConvGainNF Schematic Template



Conversion Gain, dB	Output Noise Frequency	Noise Figure, dB
-11.0	350.MHz	9.64

Note: the noise voltages do not add to give the total noise voltage at the output. However, the noise powers sum to give the total noise power at the output node.

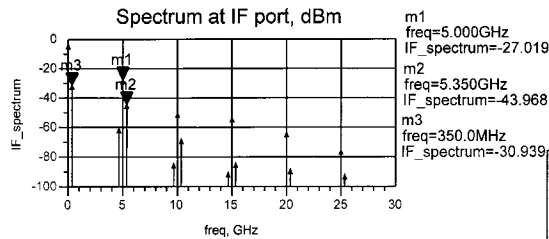
$F_{\text{spectrum}}(\text{dB}) = (\text{dB V})$

Noise Contributor Listing

Name of Noise Contributor	Contribution to Noise Voltage Spectral Density at "Vif" Node
_total	476.9pV
_Term1	267.2pV
PORT3	221.2pV
PORT1	169.2pV
Q1.RG	120.6pV
Q2.RG	118.8pV
L5.R1	100.7pV
Q1.RD	99.46pV
Q1.D1.id	71.62pV
Q1.D1	71.62pV
L2.R1	66.86pV
R2.R1	63.50pV
R1.R1	63.50pV
Q1.D2	45.87pV
Q1.D2.id	45.87pV
Q2.RS	43.79pV
L3.R1	43.53pV
L1.R1	40.78pV
Q2.D2	37.33pV
Q2.D2.id	37.33pV
Q2.RD	37.24pV
Q2.D1	32.50pV
Q2.D1.id	32.50pV
L6.R1	21.19pV
L8.R1	20.80pV
L4.R1	13.72pV
Q1.R1	8.131pV
Q2.R1	5.251pV
TL90.R1	92.97fV
TL89.R1	92.95fV
TL49.R1	89.62fV
TL11.R3	67.65fV

Figure 6. Down Converter (Mid Band)

Use with MixConvGainNF Schematic Template



Conversion Gain, dB	Output Noise Frequency	Noise Figure, dB
-10.9	350.MHz	9.61

Note: the noise voltages do not add to give the total noise voltage at the output. However, the noise powers sum to give the total noise power at the output node.

$F_{\text{spectrum}}(\text{dB}) = (\text{dB V})$

Noise Contributor Listing

Name of Noise Contributor	Contribution to Noise Voltage Spectral Density at "Vif" Node
_total	475.6pV
_Term1	268.9pV
PORT3	222.5pV
PORT1	170.5pV
Q1.RG	119.0pV
Q2.RG	113.9pV
L5.R1	100.3pV
Q1.RD	98.11pV
Q1.D1.id	71.85pV
Q1.D1	71.85pV
L2.R1	67.21pV
R2.R1	62.58pV
R1.R1	62.57pV
Q1.D2	46.30pV
Q1.D2.d	46.30pV
L3.R1	43.50pV
Q2.RS	42.61pV
L1.R1	41.22pV
Q2.RD	36.45pV
Q2.D2.d	34.70pV
Q2.D2	34.70pV
Q2.D1.d	30.63pV
Q2.D1	30.63pV
L6.R1	20.87pV
L8.R1	20.36pV
L4.R1	12.81pV
Q1.R1	8.540pV
Q2.R1	6.007pV
TL90.R1	93.25fV
TL89.R1	93.23fV
TL49.R1	89.28fV
TL11.R3	67.81fV

Figure 7. Down Converter (High Band)

Figures 8, 9, and 10 show the mixer conversion loss and frequency spectrum for the low band, mid band, and high band response of the mixer as an up converter. This was simulated using an LO power of +10 dBm and an IF input power of -20 dBm.

It can also be seen from these plots that since the LO power is +10 dBm and the LO leaking out of the RF port is typically -6 dBm, the LO to RF isolation is calculated to be 16 dB which is one of the goals of this design.

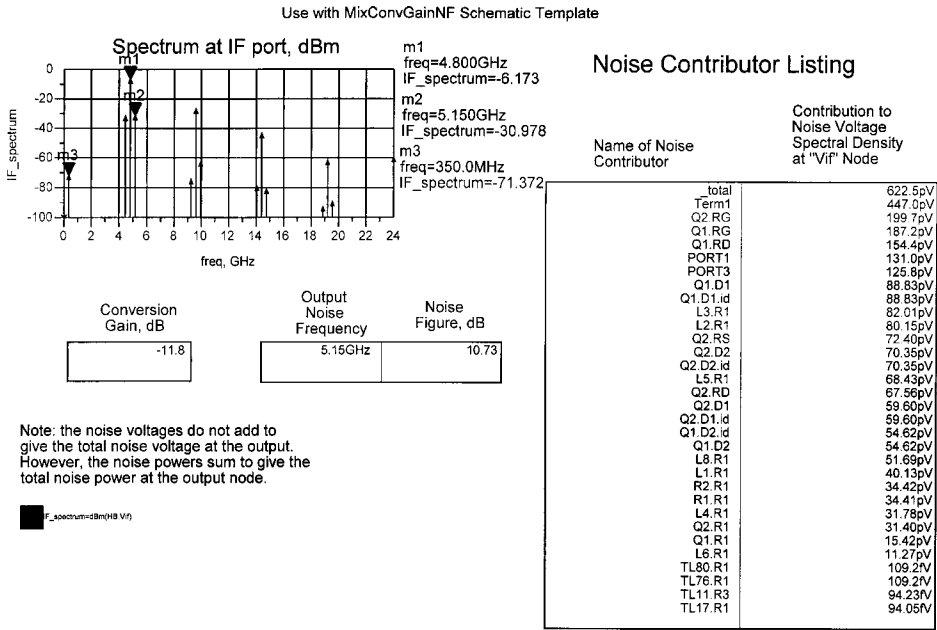


Figure 8. Up Converter (Low Band)

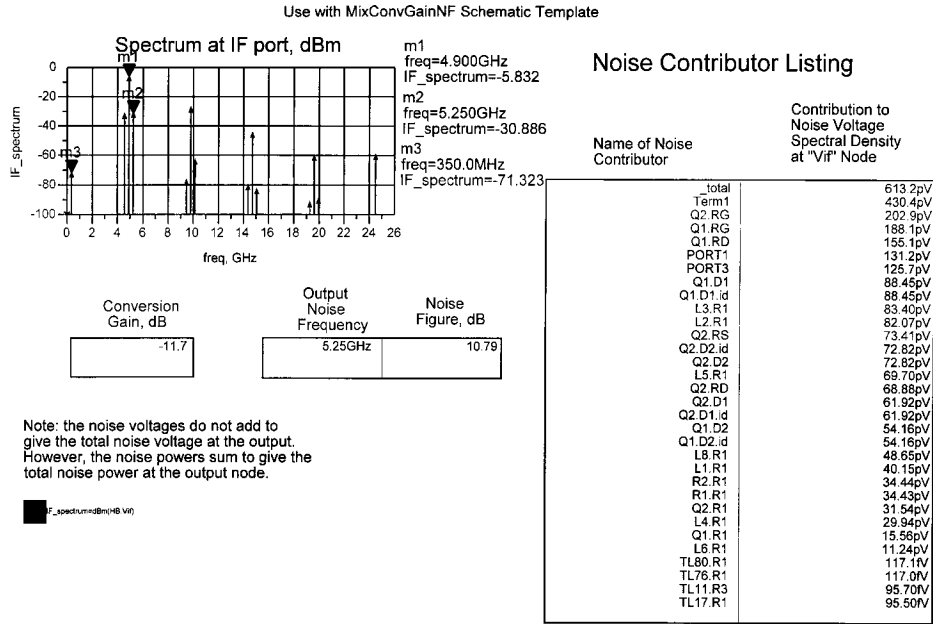


Figure 9. Up Converter (Mid Band)

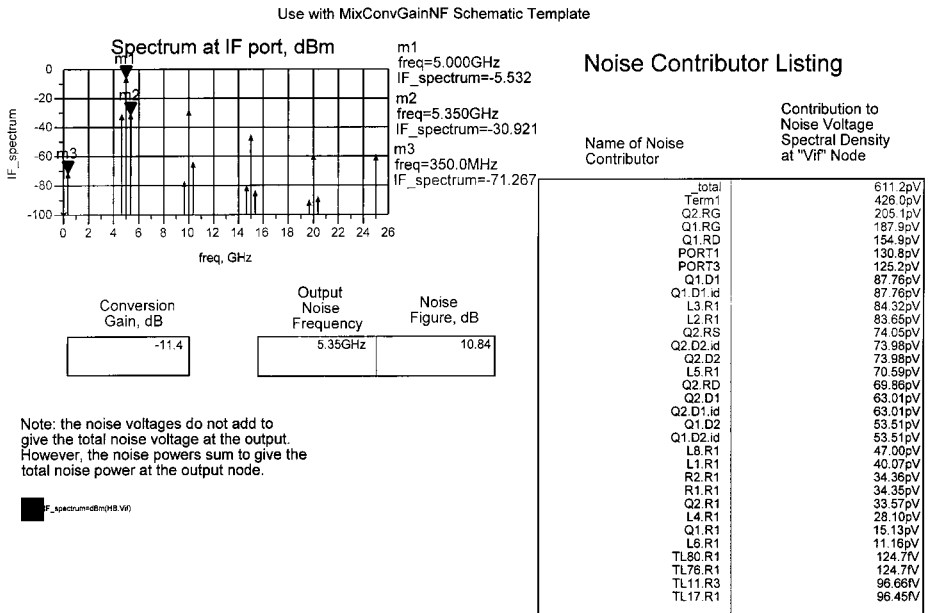


Figure 10. Up Converter (High Band)

Figure 11 shows the final layout of the C Band Up/Down Converter MMIC mixer.

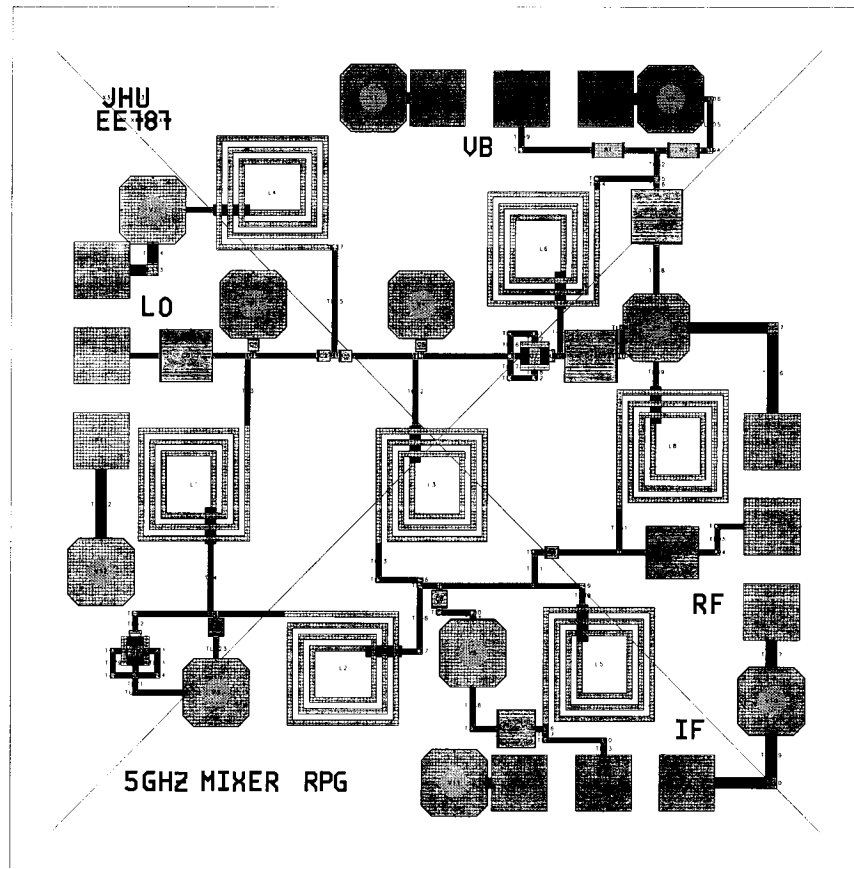


Figure 11. Final MMIC Mixer Layout

Chapter 3

SCHEMATIC DIAGRAM

The following Figure 12 is the simplified schematic for the C band up/down converter mixer.

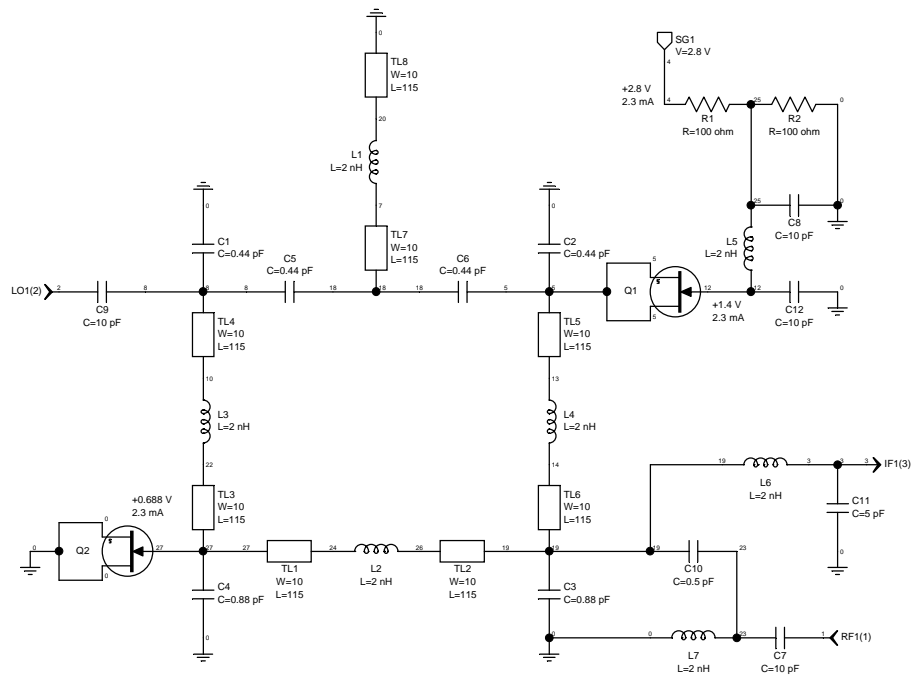


Figure 12. Simplified Mixer Schematic

The only other addition to this circuit necessary to make the mixer complete is the requirement of an external blocking capacitor for the IF port since there was no room on the MMIC to insert one.

Chapter 4

DC ANALYSIS

The schematic of Figure 12 in Chapter 3 shows the DC bias voltages and currents. The external biases for all the simulations were set to +2.8 V and a current of 2.3 mA. This gave a +0.7 V drop across the DFET diodes to turn them on and allow for operation of a starved LO.

The resistive divider allows for fine-tuning of the voltage drops across the DFET diodes without making difficult adjustments to the power supplies during test.

Chapter 5

TEST PLAN

The following test plan is offered to assist in the taking of the measurements of the mixer for comparison with the simulated results. Figure 13 shows the test equipment requirements and MMIC Mixer connections for measuring down and up conversion. The solid lines are for down conversion measurements and the dashed lines are for up conversion measurements.

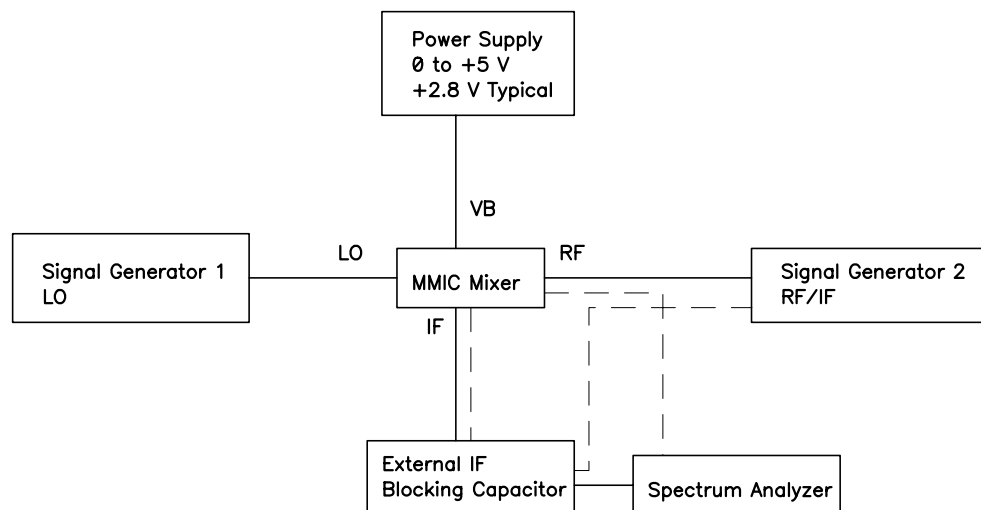


Figure 13. Test Setup

The signal generator for the LO should be set to +10 dBm and the other signal generator for the RF/IF should be set to a power level of -20 dBm. This will provide for measurements that are comparable to the simulated results. These results would be displayed on the spectrum analyzer in the form of a frequency spectrum similar to Figures 5 through 10.

For VSWR measurements a directional coupler should be placed at the LO, RF, and IF ports so that reflected power can be measured on a power meter and used to calculate the VSWR of each port. An alternative method would be if the Wiltron or some other vector network analyzer can accommodate mixer measurements, then the VSWR of each port could be swept over frequency rather than measuring the reflected power at specific frequencies.

Chapter 6

CONCLUSIONS AND RECOMMENDATIONS

A novel approach to a MMIC C band up/down converter was presented with simulated performance of a final layout version. The simulated results show that a shunt DFET diode mixer could be designed using a 180-degree lumped element hybrid with good results. This allowed for easier layout on a 60 x 60 mil ANACHIP and for bias supply injection.

The specifications were met with some of the goals achieved except for the conversion loss. Better matching of the DFET diodes could be achieved over a broader range if more room was available. This would provide better VSWR over a broader frequency range and would be less susceptible to process variations. Although the conversion loss was higher than desired, the conversion loss was very flat across the RF and LO frequencies.

Finally, sharper filters for the RF and IF ports could be used by adding more sections if more room was available. This would provide better RF to IF isolation which is dependent on the filters. Also an on-chip blocking capacitor for the IF port would be desired if more room on the chip could be achieved.

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