

WCS Band Frequency Doubler Design
Using Triquint TQTRx Process

by

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Abstract

WCS BAND FREQUENCY
DOUBLER DESIGN

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A balanced frequency doubler MMIC design is presented in this report. Given the performance requirements, the doubler was designed utilizing Agilent's Advanced Design System (ADS) package bundled with Triquint TQTRx design kit, and was laid out on a 60 x 60 mil Anachip. Along with other designs for the MMIC design class, the frequency doubler will be part of a chip set for use in the WCS band transceiver application.

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1 INTRODUCTION

1.1 Circuit Description

The designed frequency doubler will work at the LO port in the applications operating under Wireless Communication Service (WCS) band, which is from 2305 to 2360 MHz. The doubler's input frequency ranges from 1070 to 1170 MHz, and output from 2140 to 2340 MHz.

The schematic consists of three parts, which are the 180-degree hybrid, the multipliers, and the output stage amplifier. The 180-degree hybrid provides two output signals, with 180-degree phase difference to each other, feeding to the frequency multipliers.

The multiplier is a GFET biased at the point close to the pinch-off region of the FET DC IV curve. Operating at this bias point can generate strong second harmonic frequency output, and yet keep the higher order frequencies low in magnitude.

Due to the balanced configuration of design, combine the multiplier outputs from both branches will ideally eliminate all the odd-order harmonic frequencies. The second harmonic frequency, along with other weak higher-even-order components, will be boosted to the desired output power level by the last stage amplifier.

1.2 Design Philosophy

1.2.1 180 Degree Hybrid

In the beginning phase of the project, there are several approaches to design the frequency doubler. One of them is to drive the multiplier hard to generate harmonic components and the filter out unwanted frequencies. The balanced configuration was adopted because it has the advantage of the simplicity of the

circuitry, since the filter stage design could be bypassed. Due to the size limitation of the anachip and the low operating frequency, the width and line spacing of the spiral inductors in the hybrid has decreased half to 5 μm to minimize the size and save the chip space. This results in more resistance in the Triquint inductors, and creates more attenuation of the signal. More amplification at the output stage is therefore required to compensate the loss here.

1.2.2 Class AB Amplifier (Multiplier)

The 600 μm (100X6) GFET was chosen for use in the multiplier because of its power handling capability and ability to generate stronger second harmonic frequency. The GFET is biased at $V_{gs}=-2\text{V}$ and $I_{ds}=10\text{mA}$, which is very close to the pinch-off region. A 200 ohm shunt resistor at the input side is introduced to provide a connection point for the bias voltage, V_{gs} .

1.2.3 Output Stage Amplifier

The output stage utilizing another 600 μm (100X6) GFET, no input matching network since this transistor already has -10 dBm S11 without any matching circuitry, which is already sufficient for our application. Output matching network has been designed to have better output VSWR, since the output power, by specification requirement, is not high (0 dBm), and with the VSWR optimized OMN, this amplifier has a very high power compression point already..

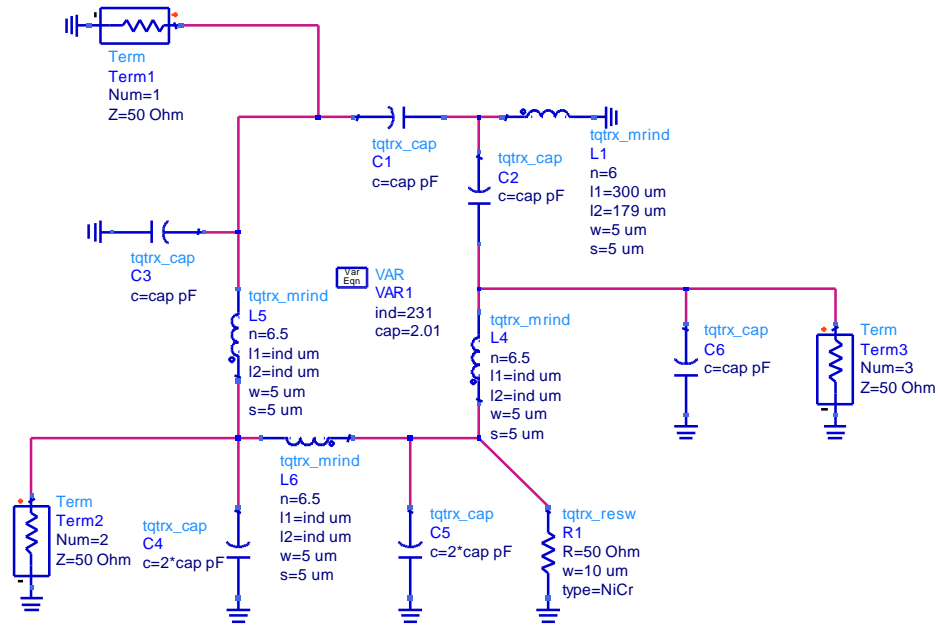
1.3 Trade-Offs

The first trade-off I have encountered in the project is the size of the hybrid and the loss. Due to the relatively low frequency, the size of the hybrid would be very remarkably large. With limited space in Anachip, I have to compromise the loss with the space. In this design project, the loss is two more dB, which can be easily compensate by either the class AB amplifier or the output stage amplifier.

Second would be the trade-off between the power gain and the current. Worries about the loss in the hybrid make me try to achieve higher power gain at both the class AB amplifier and the output stage amplifier by using larger GFET (600 μm). This became to be very rewarded in return, with +10 dBm input, this frequency doubler could achieve +17 dBm output, which is way over the requirement and failed the specifications. At the same time, the current in the design became very large, such as in the output stage amplifier, and bias current $I_{\text{ds}}=110 \text{ mA}$.. As the result, I should compromise with the gain performance, since the overall requirement is not hard to achieve.

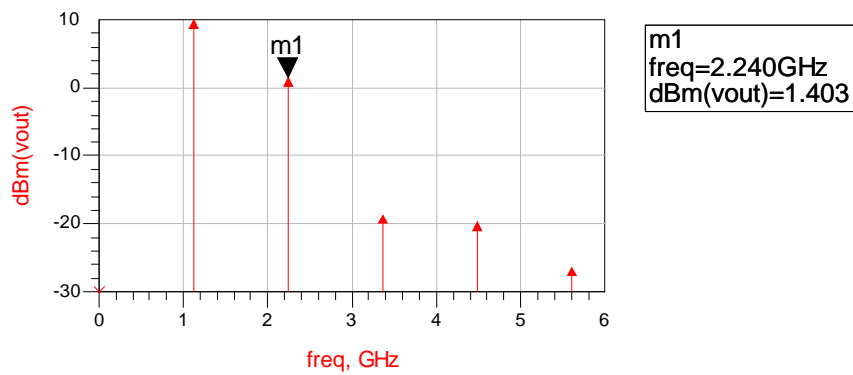
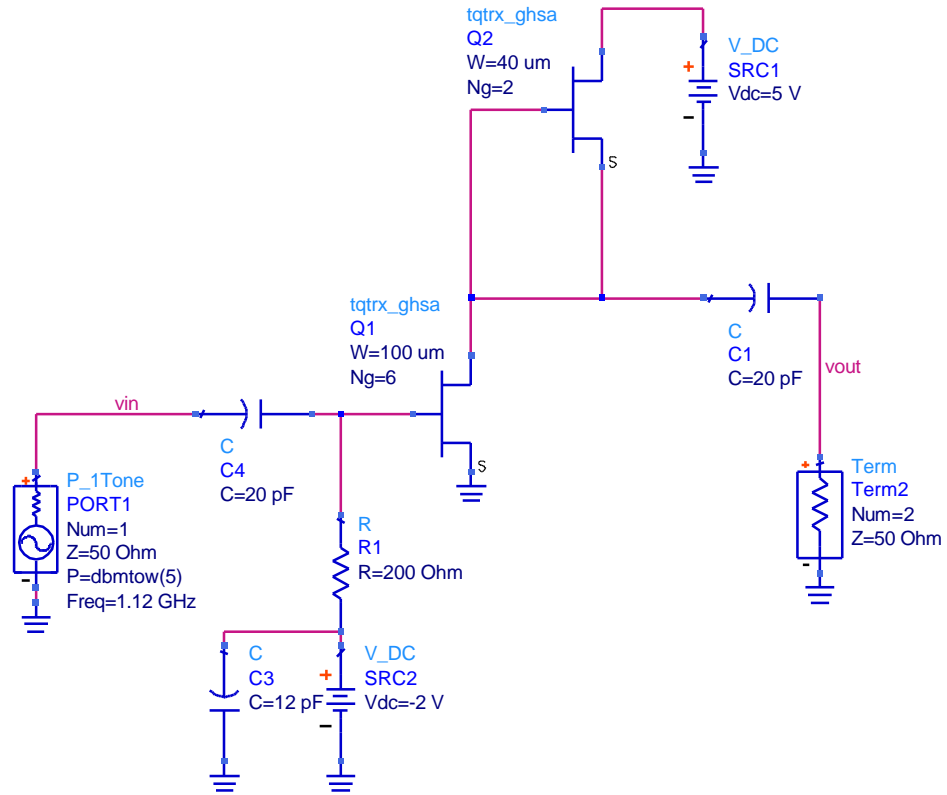
2 SCHEMATIC DIAGRAMS

2.1.1 180 Degree Hybrid Schematic



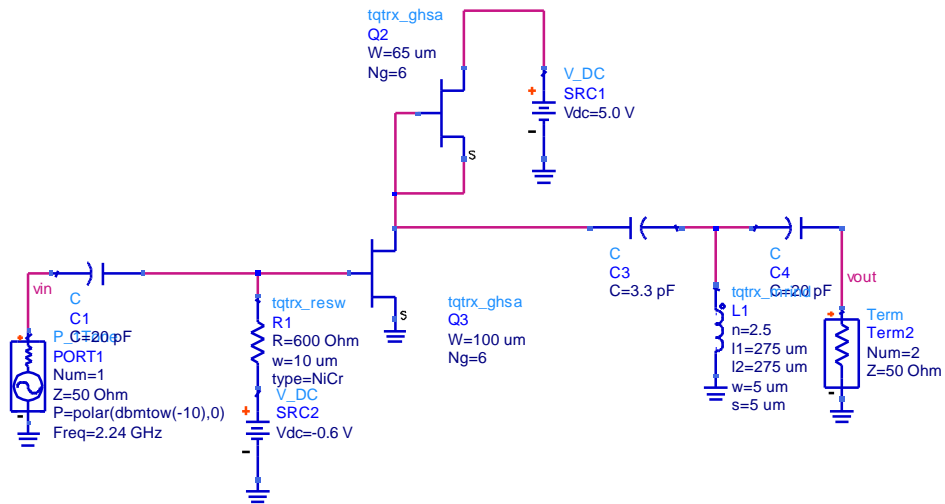
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2.1.2 Class AB Amplifier Schematic



the class AB shows very good second order harmonic frequency output, at the same time, the higher order harmonics still have at least 30 dBc compression compare to the fundamental frequency.

2.1.3 Output Stage Amplifier Schematic



the 600 um (100 x 6) GFET with the active 390 um (65 x 6) GFET load, which providing 109 mA I_{ds} to have the output stage working as a linear class A amplifier. Note that there is a stabilized 600 ohm shunt resistor on the input side, and the OMN here is not to optimize output power performance, but just to achieve better output VSWR.

3 MODELED PERFORMANCE

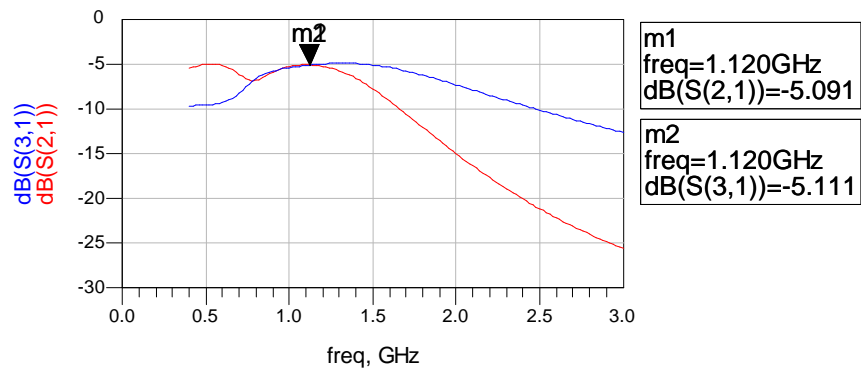
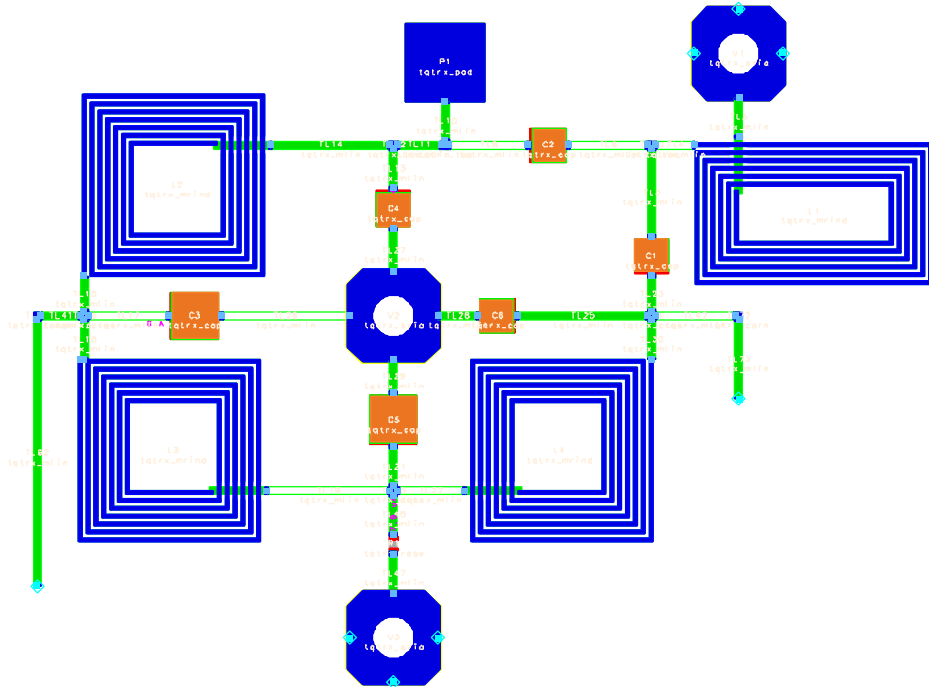
3.1 Specification Compliance Matrix

The compliance matrix summarizes all the design parameters and requirements of the frequency doubler.

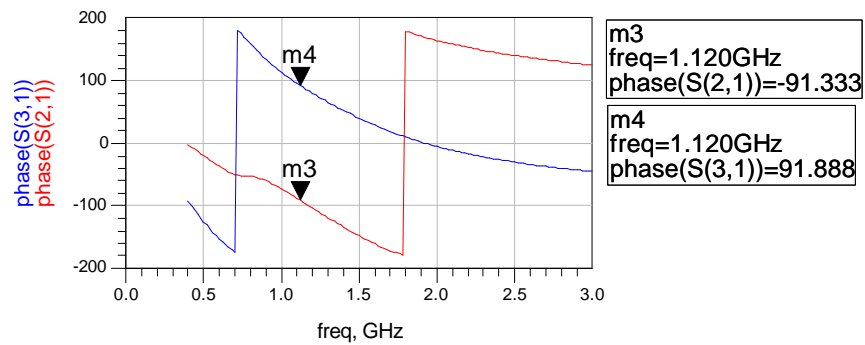
	Specification	Simulation Result
Input Frequency	1070 – 1170 MHz	
Output Frequency	2140 – 2340 MHz	
Conversion Loss	3 dB max., 0 dB goal	
Input Power	+10 dBm	
Spurious – Fundamental	16 dBc min., 25 dBc goal	
Spurious – Third	20 dBc min., 30 dBc goal	
VSWR (50Ω)	2.5:1 max., 1.5:1 goal	
Supply Voltage	± 5 Volts, goal: +5 V only	
Size	60 x 60 mil Anachip	

3.2 Predicted Performance

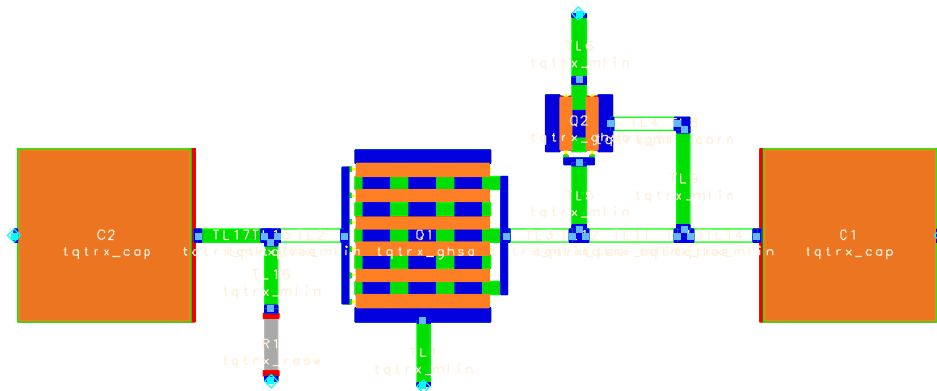
3.2.1 180 Degree Hybrid Performance



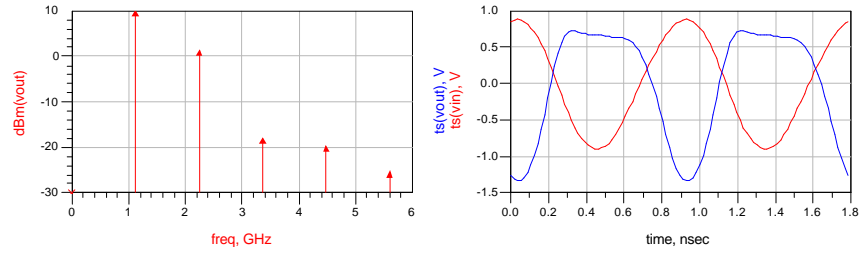
using the smaller width and line spacing inductors turns out to have more resistance and therefore, the output of the hybrid becomes more lossy. The phase difference is also off by 2 degree.



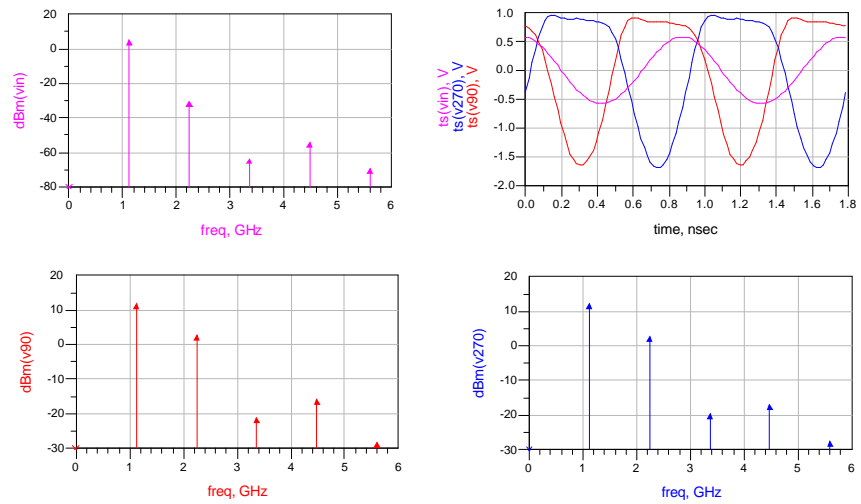
3.2.2 Class AB Amplifier Performance

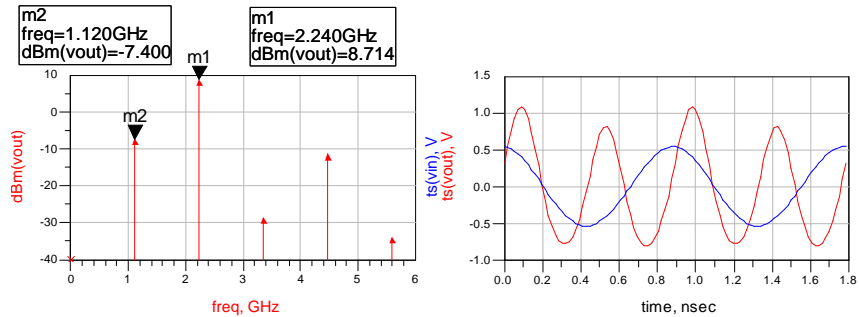


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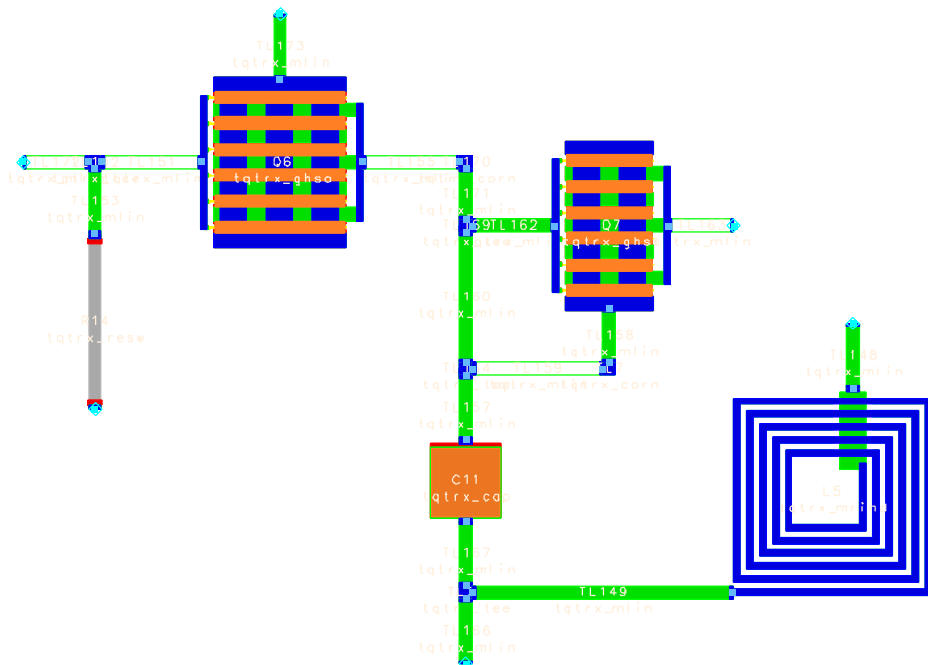
Connect the 180 degree hybrid and the two class AB amplifiers: v90 and v270 are the outputs from two branches.





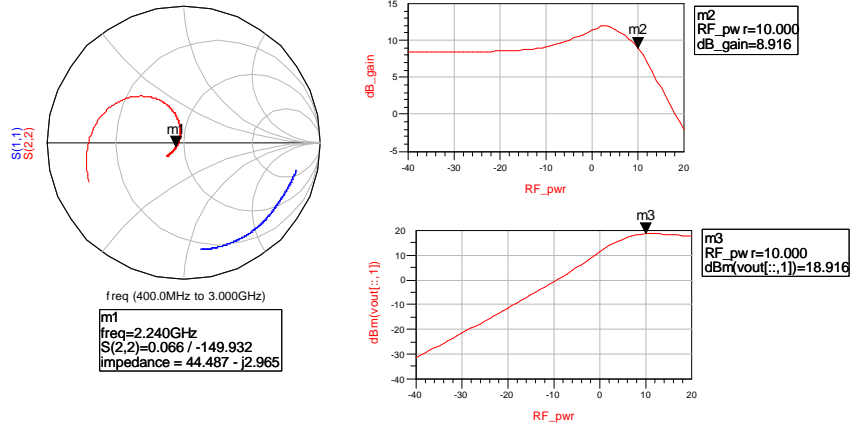
Combine the outputs of the two class AB amplifiers, all odd-ordered harmonics should be canceled, however, in our design and simulation, due to the slight mismatch of the two outcomes, there will be some considerable amount of the fundamental frequency that will feed into the output stage amplifier.

3.2.3 Output Stage Amplifier Performance



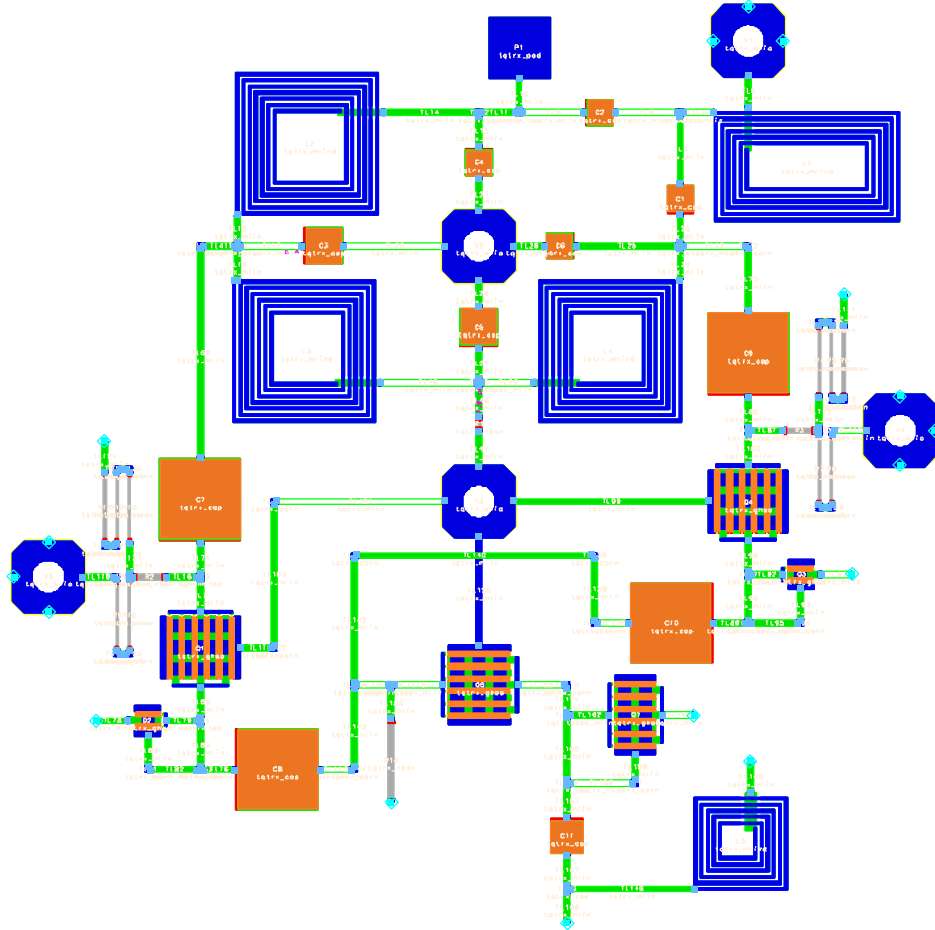
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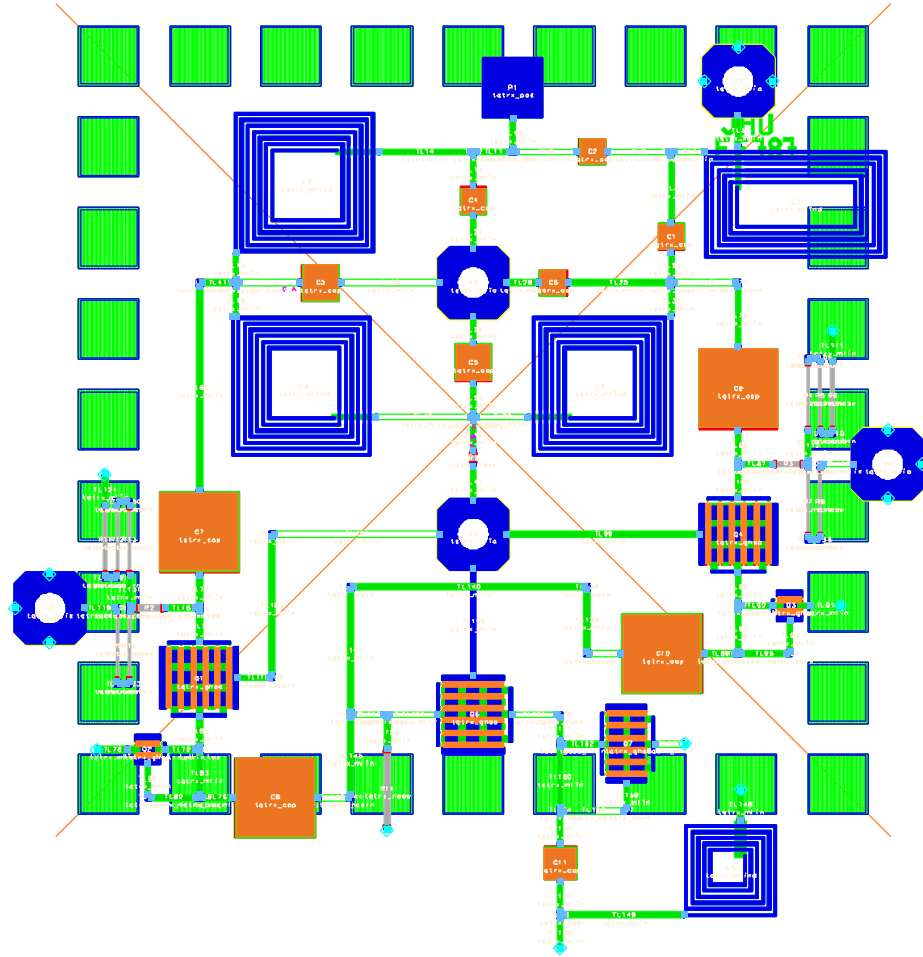


the output stage has very good output VSWR and the input P1dB is at 10 dBm, and can handle the power up to 18.9 dBm.

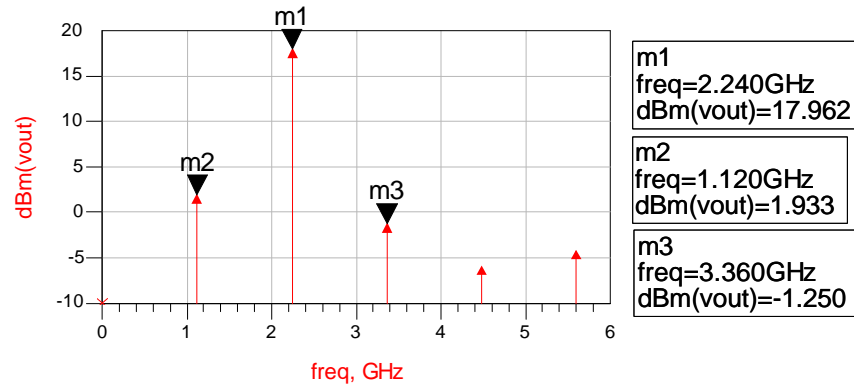
3.2.4 The Frequency Doubler



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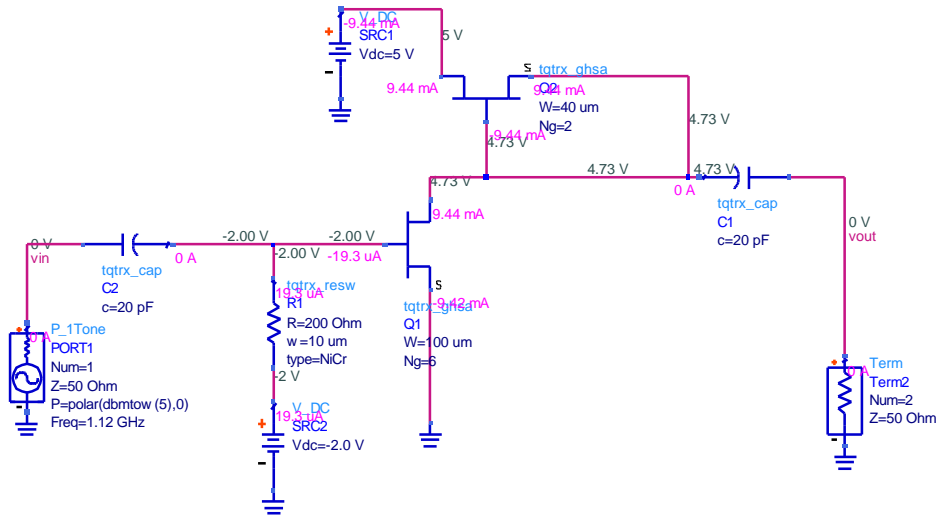


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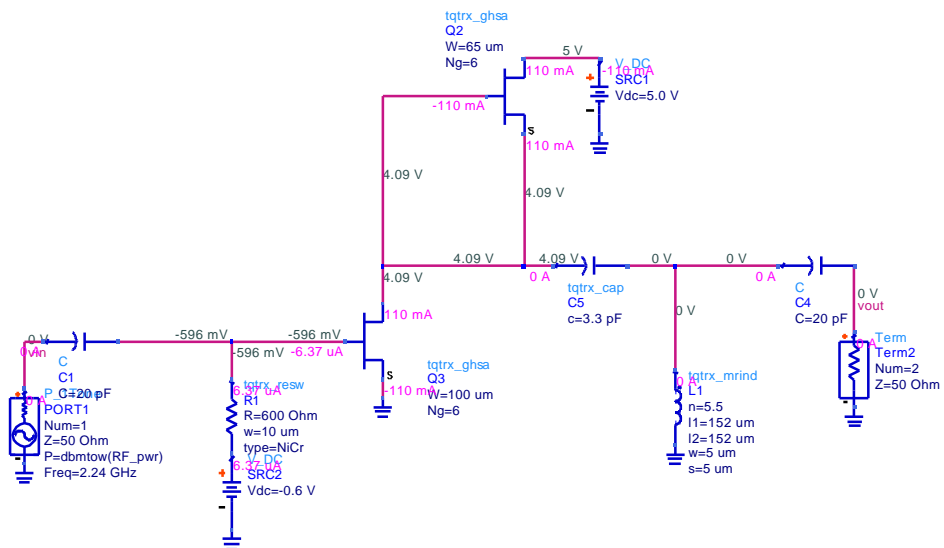
4 DC ANALYSIS

4.1 Class AB Amplifier



the 600 um GFET is biased under $I_{ds}=9.44$ mA, $V_{gs}=-2$ V

4.2 Output Stage Amplifier



the 600 μm GFET is biased at $I_{\text{ds}}=110 \text{ mA}$, and $V_{\text{gs}}=-0.6 \text{ V}$.

5 TEST PLAN

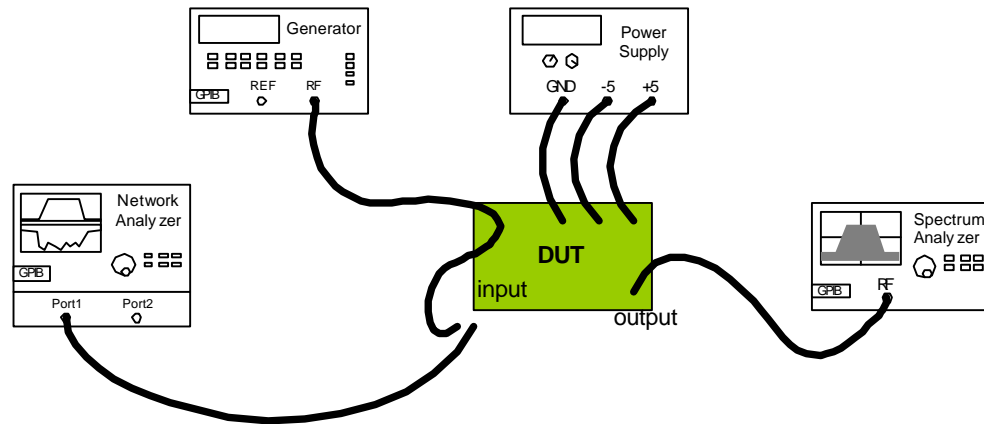
This section of report outlines the test plan and setup configuration to evaluate the fabricated chipset.

5.1 Test Equipment

Test Equipment

Wafer probe station	1
RF signal generator	1
Spectrum analyzer	1
Network Analyzer	1
DC power supply	1
Digital multi meter	1

5.2 Test Setup



5.3 Test Procedures

1. Mount the DUT chip on the probe station, apply DC voltage ($\pm 5V$).
2. Input +10 dBm signal, frequency 1070 MHz, 1120 MHz, and 1170 MHz (B, M, T), measure the output power with spectrum analyzer, read and record the values at 2140 MHz, 2240 MHz, and 2340 MHz, respectively.
3. Input +10 dBm signal, frequency 1120 MHz, measure the output power with spectrum analyzer, read and record the values at 1120 MHz, 2240 MHz, and 3360 MHz, respectively.
4. Using network analyzer, measure the input VSWR/ input return loss.
5. Refer to section 3.1 for test specifications.

6 CONCLUSION AND RECOMMENDATION

The choice of using the balanced design with 180 degree hybrid turned out to simplified the circuitry a lot. However, the hybrid itself would take as much as space as the filter stage would take.

More improvement could be done easily done, due to time constraint, I could only work on the design after the submit ion of the report:

1. I've over estimated the effect of the lossy hybrid. The class AB amplifier and the output stage could be redesigned, to reduce the operation current and at the same time, meet the gain requirement.
2. The DC bias circuitry could be redesigned and achieve the goal of using only one DC supply.

3. The input VSWR could be tuned to have better performance.
4. The spurious performance can be optimized by tuning the two output branches of our design.