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525.787.91		Monolithic Microwave Integrated Circuit Design			1(23)
<i>Prepared By</i>	<i>Email</i>	<i>Phone</i>	<i>ID</i>	<i>Date</i>	
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John Penn	john.penn@jhuapl.edu	443-778-6814	n8lrich@apl.jhu.edu	VCO	

An Initial Swing at Controlled Instability

An
L - Band VCO

Center Frequency = 1120 MHz
Bandwidth = 100 MHz

A Student Project Designed By
Mark F. Petty

For
The Johns Hopkins University – Applied Physics Laboratory
Class # 525.787 - Monolithic Microwave Integrated Circuit Design

Instructors:
Craig Moore
John Penn

Fall 2002

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ABSTRACT:

This paper describes an L-Band voltage controlled oscillator, VCO, designed for a student's semester final project for the Johns Hopkins University, Monolithic Microwave Integrated Circuit, MMIC, class # 525.787. This VCO is one of several student designs used to form a "Wireless Communications Service", WCS, system or an "Industrial, Scientific and Medical", ISM, system. The computer aided design, CAD, tools used for this project include Agilent's Advanced Design System, ADS, version 1.5, and MathWork's Student Edition of Matlab release 12. The VCO's target of fabrication is TriQuint Semiconductor's Texas 0.6 μm Gallium Arsenide fab. TriQuint provided the device library used to describe the circuit elements within the VCO. The VCO requirements include: a center frequency of 1170 MHz; a tuning range of +/- 50 MHz; minimum output power of +10dBm, desired output power of +13dBm; supply voltage of +/- 5 volts, desired supply voltage of + 5 volts only; frequency tuning voltage of 0 – 5 volts; output impedance of 50 ohms, nominal; sized to fit on the 60 x 60 mil TriQuint ANACHIP.

INTRODUCTION:

Sustained oscillation results from, in short, an unstable amplifier. Since the amplifier circuit is a basic building block of electrical circuitry, much work has been performed to predict and prevent the instability of amplifiers. Pozar [1] discusses the derivation of stability circles for the input and output ports of networks, and the "K and Δ " stability parameters. The S-Parameter derived K and Δ stability parameters are further messaged into centers and radii for source and load stability circles, which are then plotted on Smith Charts. Edwards [2] developed the μ , and μ' , stability parameters which allowed for the direct comparison of the stability in designs. Figure 1 illustrates the common problem of amplifier design, the last piece of the design, the output matching network, OMN, yields a reflection coefficient in the unstable region.

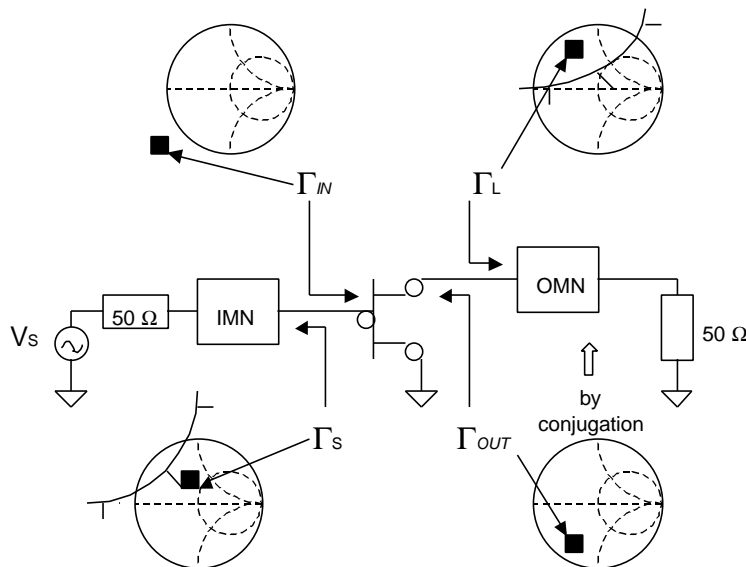


Figure 1. Illustration of the stability problem in designing an amplifier. Tick marks designate stable side of stability circles. Redrawn from Edwards [3].

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So, to design an oscillator, simply design an amplifier with an input and/or output reflection coefficient in their corresponding unstable region. Unfortunately it is not that easy. Remember, the above example was designed from the start to yield a stable amplifier, and it resulted in a possible oscillator. Yet, that is still the core of oscillator design methodology, find an unstable amplifier and don't stabilize it with input and output matching networks.

At the core of an oscillator there is an amplifier, and at the core of an amplifier there is an active device. The TriQuint Texas GaAs fabrication process yields three versions of MESFETs, to choose as the active device. A GFET was chosen because the negative gate to source voltage, V_{GS} , allows for easily biasing the transistor with a single power source. The GFET was sized at 600 μm wide to ensure that enough current flow was available to meet the power output spec. A common source amplifier design was chosen for its straightforward simplicity.

A MESFET with one terminal grounded reduces to a two-port device. The frequency response of a two-port device, or network is described by its two-port S-Parameters. Two port S-Parameters are readily available from the device manufacturer for many packaged parts or quickly computed by the ADS software for transistors designed as part of a MMIC chip. Multiple S-Parameter described devices, or networks, can be connected and the combined S-Parameters calculated to accurately describe the frequency response of the resultant network. The resultant network for this VCO consists of a resonance generator, and two-port amplifier, and a load, as shown in figure 2.

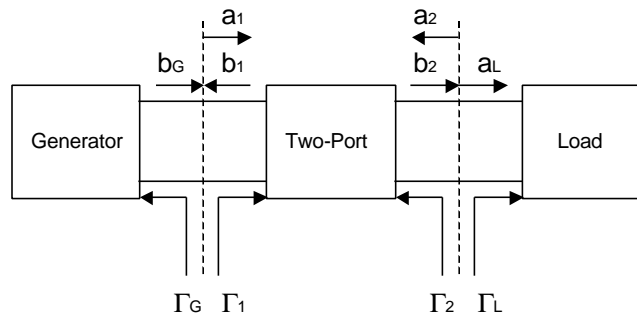


Figure 2. Loaded two-port network connect to generator.

The S-Parameter conditions needed for oscillations are, $k < 1, \Gamma_G \cdot S'_{11} = 1, \Gamma_L \cdot S'_{22} = 1$, Vendelin [4]. Where $k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12} \cdot S_{21}|}$, $\Delta = S_{11} \cdot S_{22} - S_{12} \cdot S_{21}$. And $\Gamma_1 = S'_{11} = \frac{b_1}{a_1}$.

There are two solutions where the product of two variables equals one. A – Both variables equal one. B – Each variable is the multiplicative inverse of the other. Which means one of these two reflection coefficients, Γ_G or Γ_1 is greater than one. A reflection coefficient greater than one results from an input impedance with negative resistance. The generator for the VCO contains only passive components, which yield a $\Gamma_G < 1$. Therefore, $\Gamma_1 > 1$ or, the input impedance of the two-port amplifier must contain a negative resistance. To begin the design of an oscillator, first meet the condition of negative impedance for the two-port amplifier. Next, design a resonance circuit with an output reflection equal to the input reflection of the two-port amplifier. Third, design an output-matching network to maximize power transfer to the load.

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Inside the two-port amplifier box resides a common-source connected mesfet amplifier. DC power is applied through a parallel L-C resonator to the mesfet's drain. The resonant frequency of the L-C tank equals the target frequency of the VCO, 1.12 GHz. The TriQuint GaAs process yields devices with good inherent stability. So, add a 10 Ω source resistor to aide in the design of an unstable amp. The shunt source capacitor increases the negative resistance of the circuit, while also increasing the effective capacitance looking into the gate of the transistor, Rhea [5]. The source resistor value also sets the DC operating condition $V_{GS} = -0.6$ V, since the gate is grounded. The circuit contains approximately 60 mAmps of current flow through the device.

A parallel L-C resonance tank serves as the oscillation signal generator. The shunt inductor of the parallel resonator doubles as the DC bias ground for the mesfet's gate. The resonator's variable capacitance is constructed with two 100 x 12 μm drain to source shorted mesfet varactors. The tuning voltage connects to the circuit at the drain-source common node between the two mesfets. The gate of one mesfet is grounded and the second gate connects to the inductor and amplifier. The tuning voltage biases both varactor mesfets because both gates are DC connected to ground, one gate is directly grounded and the second gate is grounded through the inductor. As figure 3 shows, include the emitter, feedback, and amplifier input capacitances and the amplifier input inductance to accurately calculate the resonant frequency, f_0 . Assumed varactor capacitance of 0.55 pF at bias voltage, $V_b = 0$ V, 0.4 pF at $V_b = 1$ V, and 0.3 pF at $V_b = 2$ V. Varactor characterization performed on 300 μm GFET, Penn [6], scale accordingly.

$$f_0 = \frac{1}{\sqrt{2p\sqrt{LC}}} \quad f_0 = \frac{1}{\sqrt{2p\sqrt{9 \times 10^{-9} \cdot 2.51 \times 10^{-12}}}} = 1.059 \times 10^9 \text{ Hz}$$

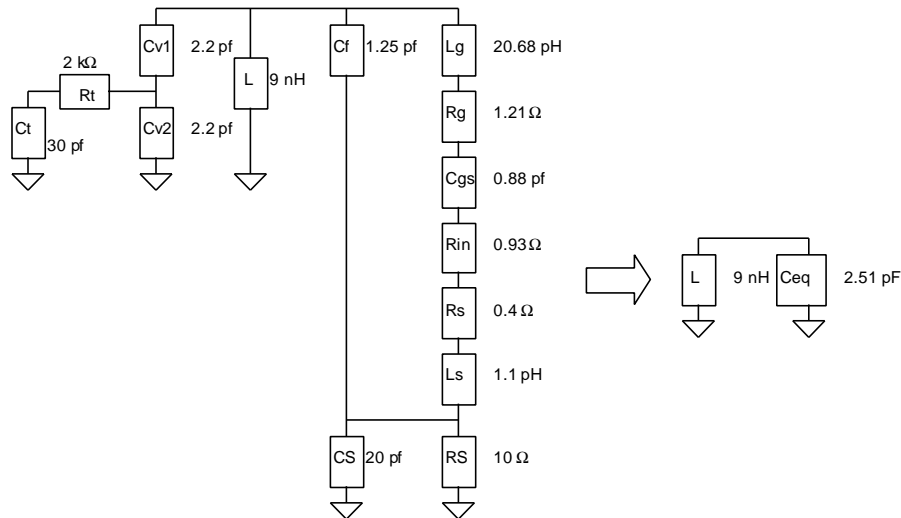


Figure 3. TriQuint linear GaAs MESFET model incorporated into the L-C resonance calculation.

Design the output-matching network with S_{11} equal, or as close as possible, to the conjugate of S_{22} of the two-port amplifier, for maximum power transfer to the load. Some matching sacrifice may need to be made here due to the practicality of device sizes.

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MODELED PERFORMANCE:

Specifications Compliance Matrix for L-Band Voltage Controlled Oscillator

	Specification	Pre-Layout	Post-Layout	Fabbed IC
Frequency Range	1070 to 1170 MHz	1056 to 1171 MHz	1012 to 1056 MHz	
Output Power	> +10 dBm > +13 dBm goal	~ +19 dBm	~ +19 dBm	
Control Voltage	0 to 5 Volts	0 to 2 Volts	0 to 0.5 Volts	
Supply Voltage	± 5 Volts + 5 Volts only goal	Single +5 Volt Supply	Single +5 Volt Supply	
Output Impedance	50 Ω, nominal	50 Ω, nominal	50 Ω, nominal	
Size	60x60 mil ANACHIP	Fits	Fits	

Design performance is questionable. Although the pre-layout design meets specs and the goals, the post-layout design fails to meet the specs. The predicted frequency shifts down, out of the specified range. And, the application of tuning voltage greater than approximately 0.5 volts causes the oscillator to fail.

SCHEMATIC DIAGRAMS:

List of the appended schematics and simulations:

Biased MESFET Schematic
 Resonant Tank Input Matching Network Schematic
 Input Matching Network's S22 overlaid in the Biased MESFET Source Stability Circles
 Output Matching Network Schematic
 Output Matching Network's S11 conjugate match with the S22 of the Biased MESFET
 Biased MESFET Instability Simulations
 IMN and Biased MESFET Schematic
 IMN and Biased MESFET Start-Up Transient Simulation
 IMN, Biased MESFET, & OMN Schematic
 IMN, Biased MESFET, & OMN Start-Up Transient Simulation
 IMN, Biased MESFET, & OMN Harmonic Balance Pre-Layout Schematic
 IMN, Biased MESFET, & OMN Harmonic Balance Pre-Layout Simulation
 IMN, Biased MESFET, & OMN Harmonic Balance Post-Layout Schematic
 IMN, Biased MESFET, & OMN Harmonic Balance Post-Layout Simulation
 VCO Layout within 60x60 mil ANACHIP
 Simplified DC Schematic Annotated with DC Bias Values

DC Analysis:

DC analysis shows that the source resistor is too thin to carry the ~ 60 mAmps of current. The 10-Ω NiCr resistor needs a width greater than 60 mm. New layout required prior to fabrication.

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TEST PLAN:

Apply tuning voltage, to “VTUNE” labeled pad on IC, equal to zero volt first, to discharge the varactor connected mesfets. Next connect the +5 volt supply to “VDD” labeled pad. Connect spectrum analyzer to pad labeled “VOUT”. Compare DC current to predicted current value from the DC analysis above. Compare oscillator output frequency and power with values predicted by Harmonic Balance simulations above.

CONCLUSION & RECOMMENDATIONS:

With its undersized source resistor this design should NOT be fabricated. If everything else simulated properly after layout it still would not hurt to clean up the layout a little more. The ground-signal-ground probe pads for the VTUNE input are unnecessary because VTUNE is a DC bias voltage. The VDD input trace has an unneeded section between the bend and the input cap. And the ground connection under the varactor mesfet should also be straight.

Countless hours were spent trying to understand and bring together the methodologies of several authors’ texts, more than those referenced. The confusion acquired by reading several texts simultaneously, then achieving ADS simulation results in disagreement with that author’s predictions can be summarized by the following passage.

“Although the negative resistance analysis characterizes the conditions leading to oscillation and predicts the oscillation frequency accurately, the author’s experience is that relating the results of the analysis to the noise performance of the oscillator is unreliable. This is a controversial position to take because of the existence of a paper by K. Kurokawa which contains a rigorous analysis of the noise performance of the negative resistance oscillator...” Rhea [7]

Even “experts” still disagree about microwave design.

My goal was to complete a design on a topic that was not discussed in class for the specific reason of testing myself. Unfortunately, I fell short of that goal. Too much time was lost with a too complicated initial design. Because it simulated successfully sometimes while I attempted to dial in the frequency I ignored the overall fragility of the design. I still don’t understand what broke the design when it was transferred from circuit without interconnects to one with interconnects. What parasitic components crippled my design? I hope that the Dorsey Center will be available between semesters so I may have the opportunity to build a better oscillator.

ACKNOWLEDGEMENTS:

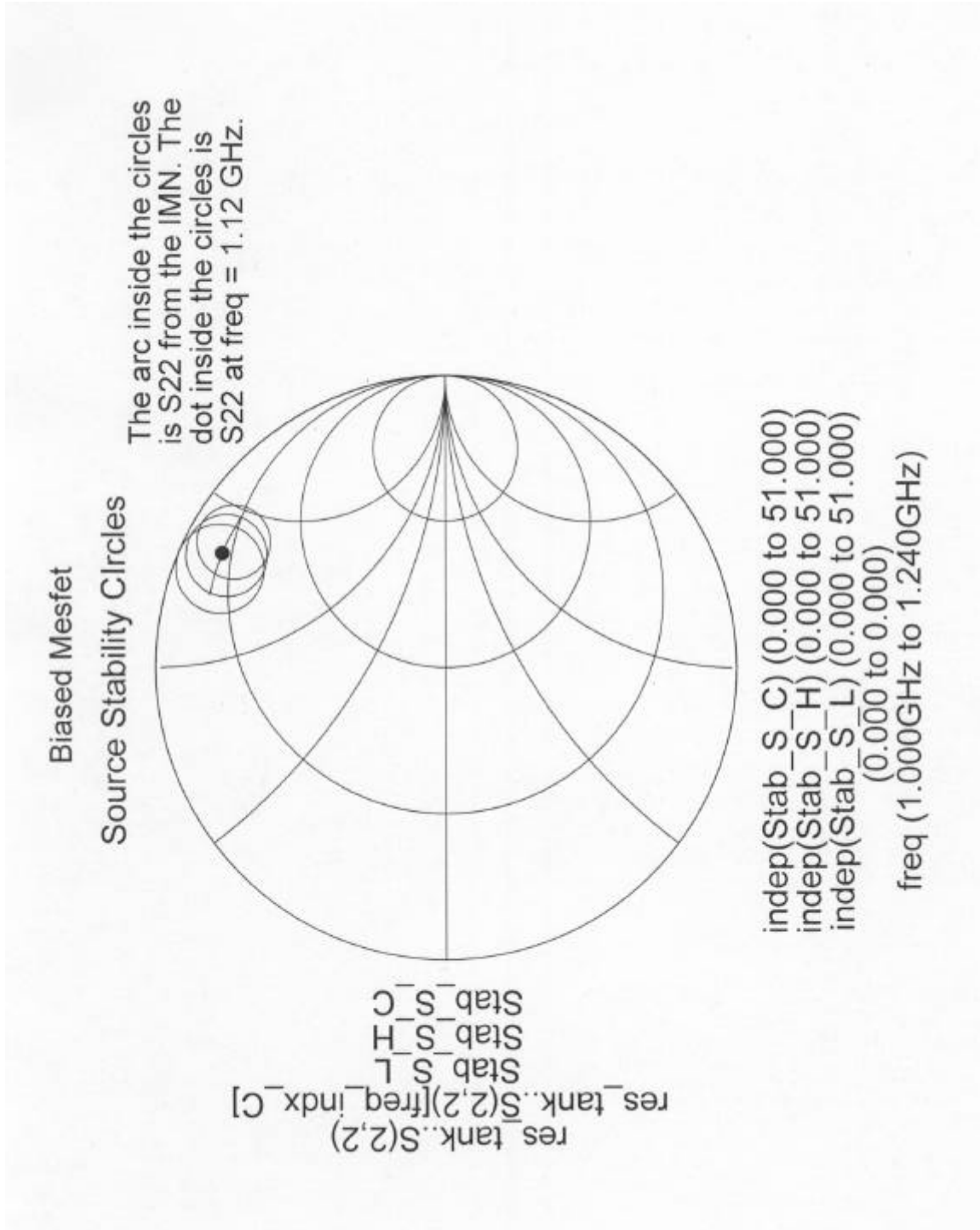
With corporations demanding experience workers at all levels, and that new hires be productive immediately upon starting employment. Realistic design oriented courses offered at colleges and universities are the only manner for someone to change their technical career track. It is with sincere gratitude that I thank all those involved in making the Monolithic Microwave Integrated Circuit design course at Johns Hopkins University a reality. My thanks go to instructors Craig Moore and John Penn. To the Agilent Corporation for providing the ADS simulation software. To TriQuint Semiconductor Corporation for providing the GaAs process library and agreeing the fabrication student designs. And to Gray Wray for supporting the ADS tool for a bunch of whining students.

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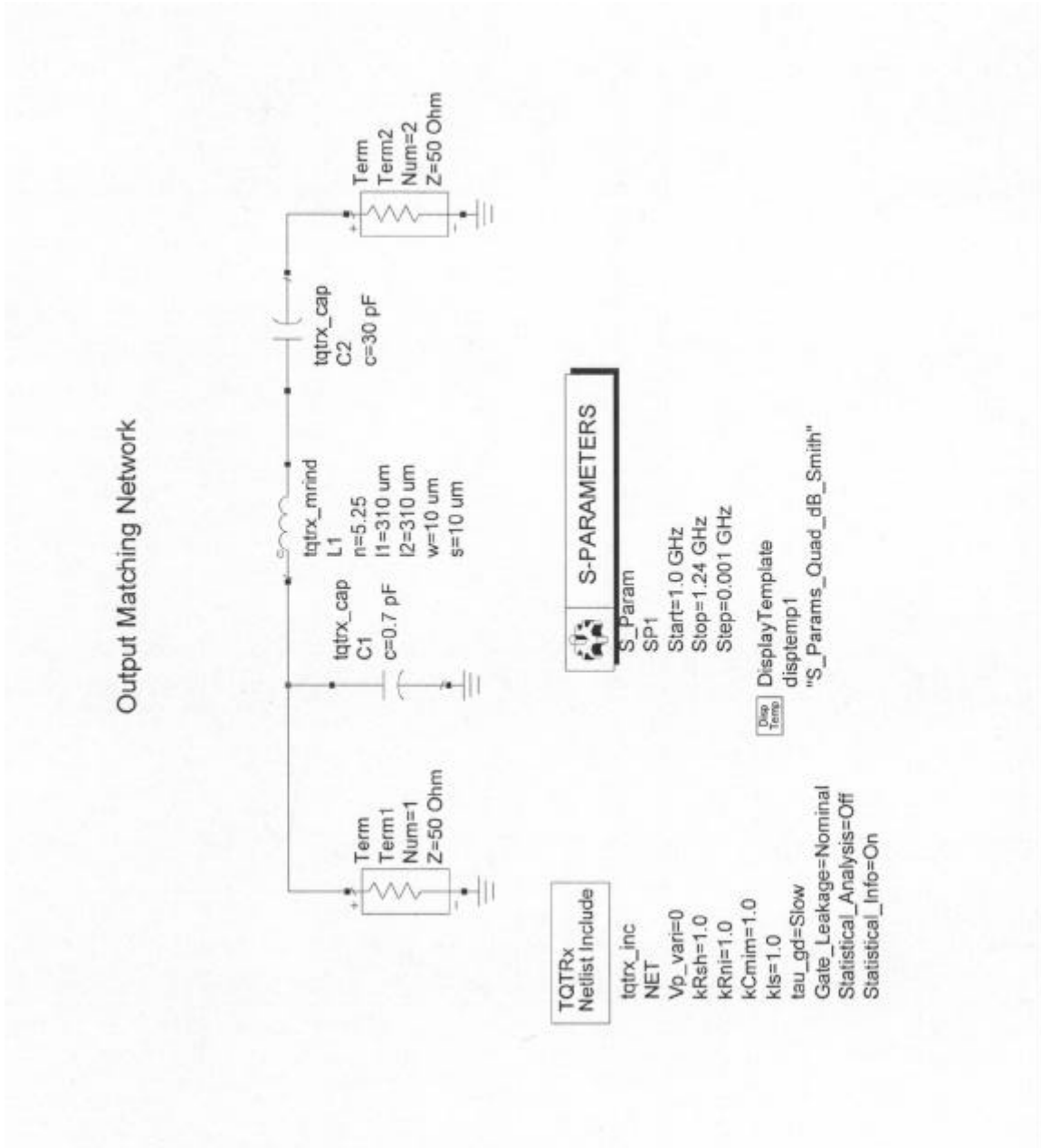
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1. D. M. Pozar, *Microwave Engineering*, New York, NY: John Wiley & Sons, 1998, pp. 612-616.
2. M. L. Edwards and J. H. Sinsky, "A new criterion for linear 2-port stability using a single geometrically derived parameter," *IEEE Trans. Microwave Theory Tech.*, vol. 40, no. 12, pp. 2303-2311, Dec. 1992.
3. M. L. Edwards, S. Cheng, and J. H. Sinsky, "A Deterministic Approach for Designing Conditionally Stable Amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 7, pp. 1567-1575, July 1995.
4. G. D. Vendelin, *Design of Amplifiers and Oscillators by the S-Parameter Method*, New York, NY: John Wiley & Sons, 1982, pp. 132.
5. R. W. Rhea, *Oscillator Design and Computer Simulation*, Atlanta, GA, Noble, 1990, pp. 67.
6. J. Penn and C. Moore, "Notes for Lecture #4, TriQuint Process Active MMIC Circuit Elements," Johns Hopkins University course 525.787.91, pp. 70, Fall 2002.
7. R. W. Rhea, *Oscillator Design and Computer Simulation*, Atlanta, GA, Noble, 1990, pp. 66.

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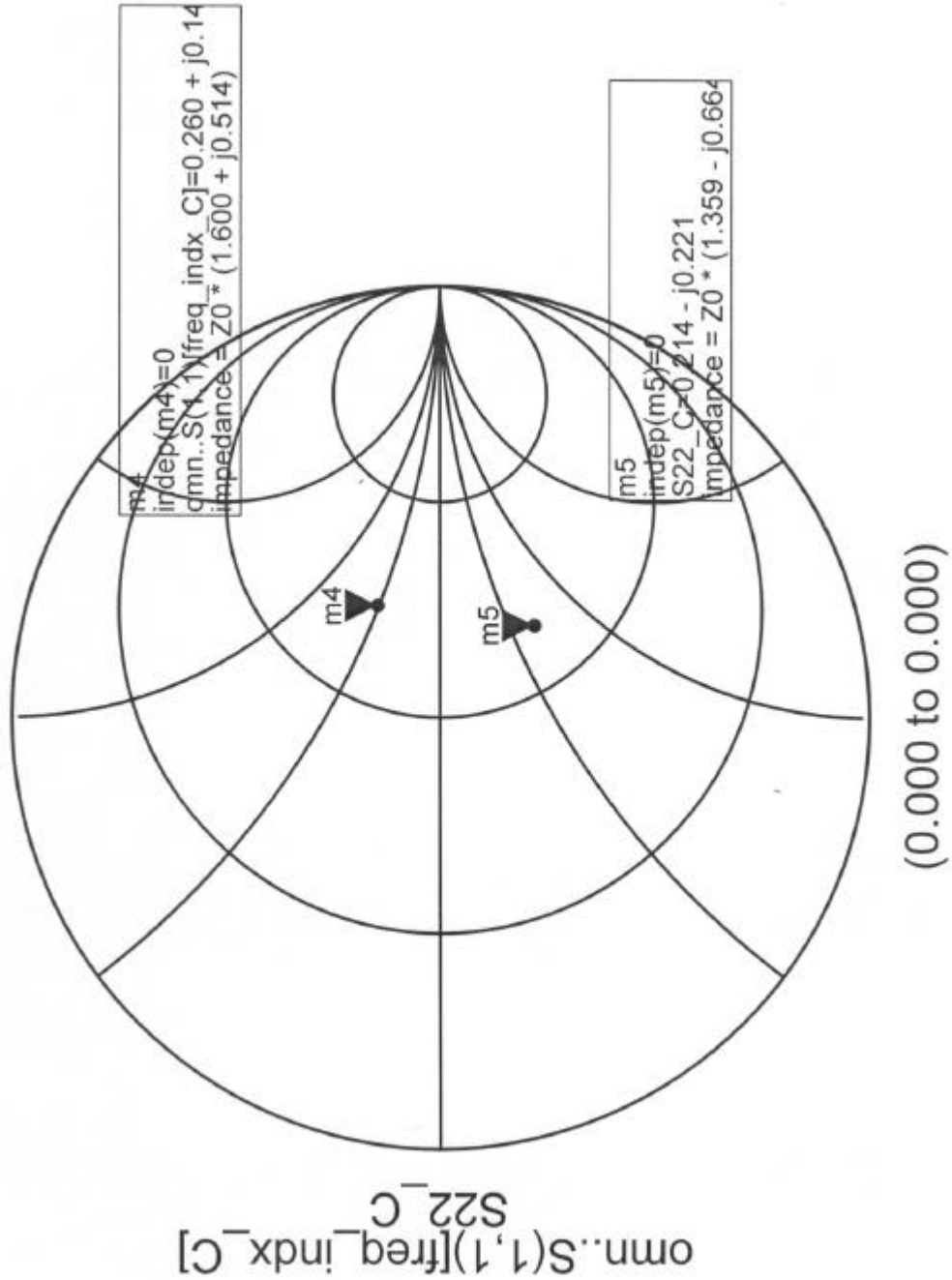


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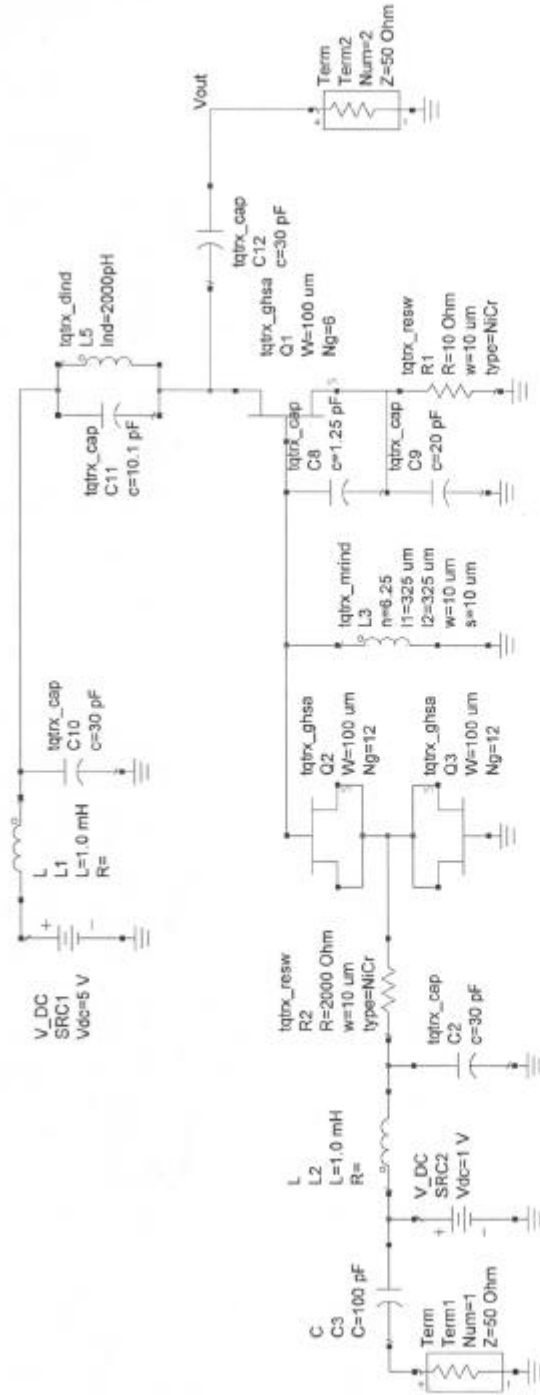


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Biased Mesfet Conjugate Output Match



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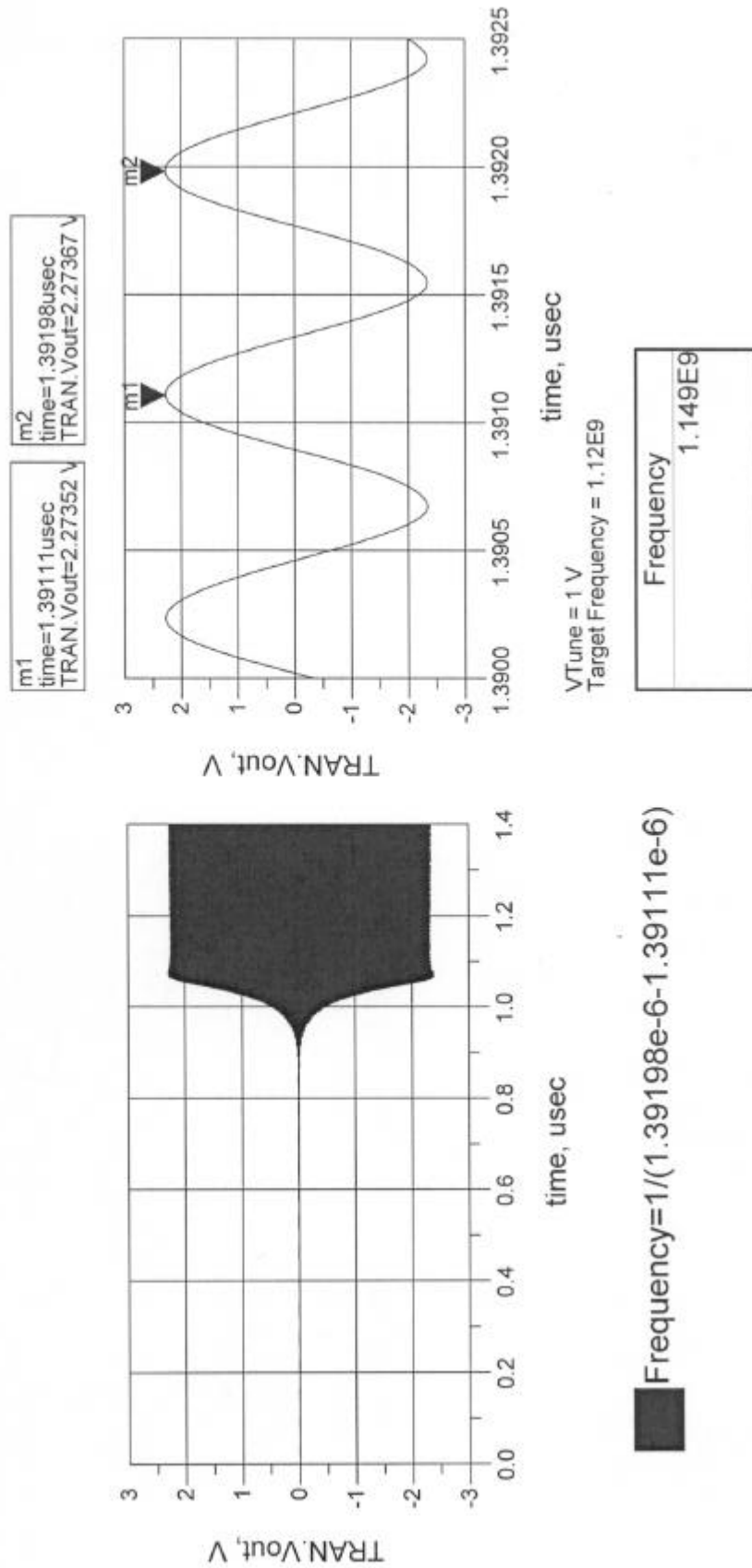
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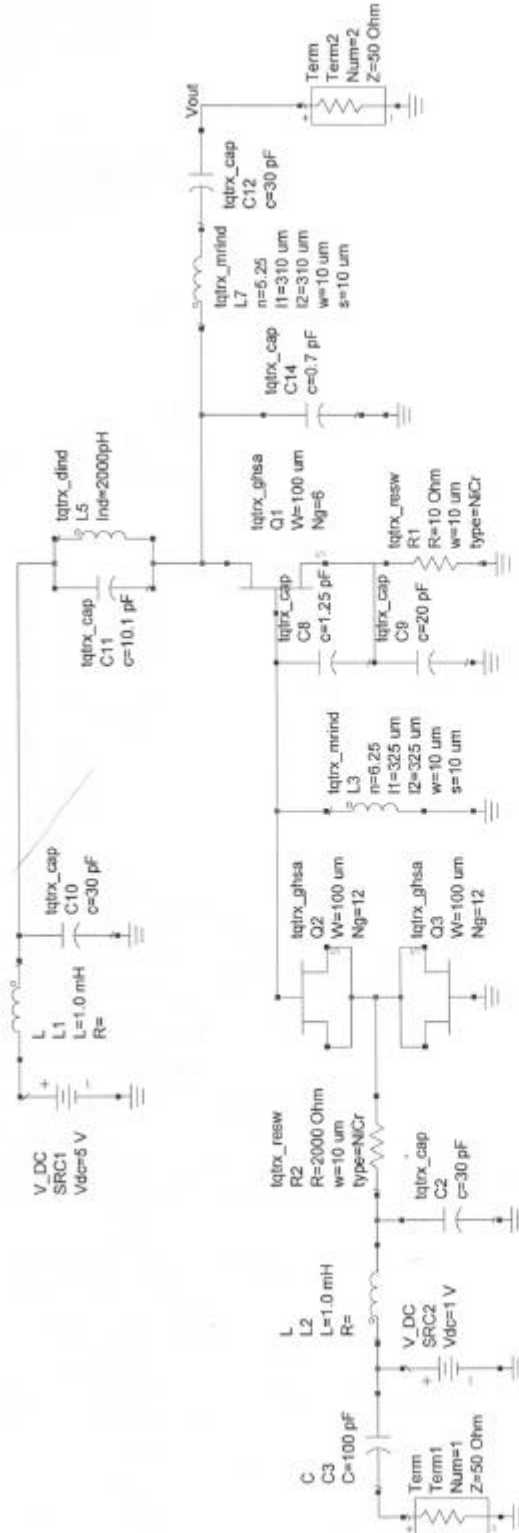
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Oscillator Start-up Transient without OMN



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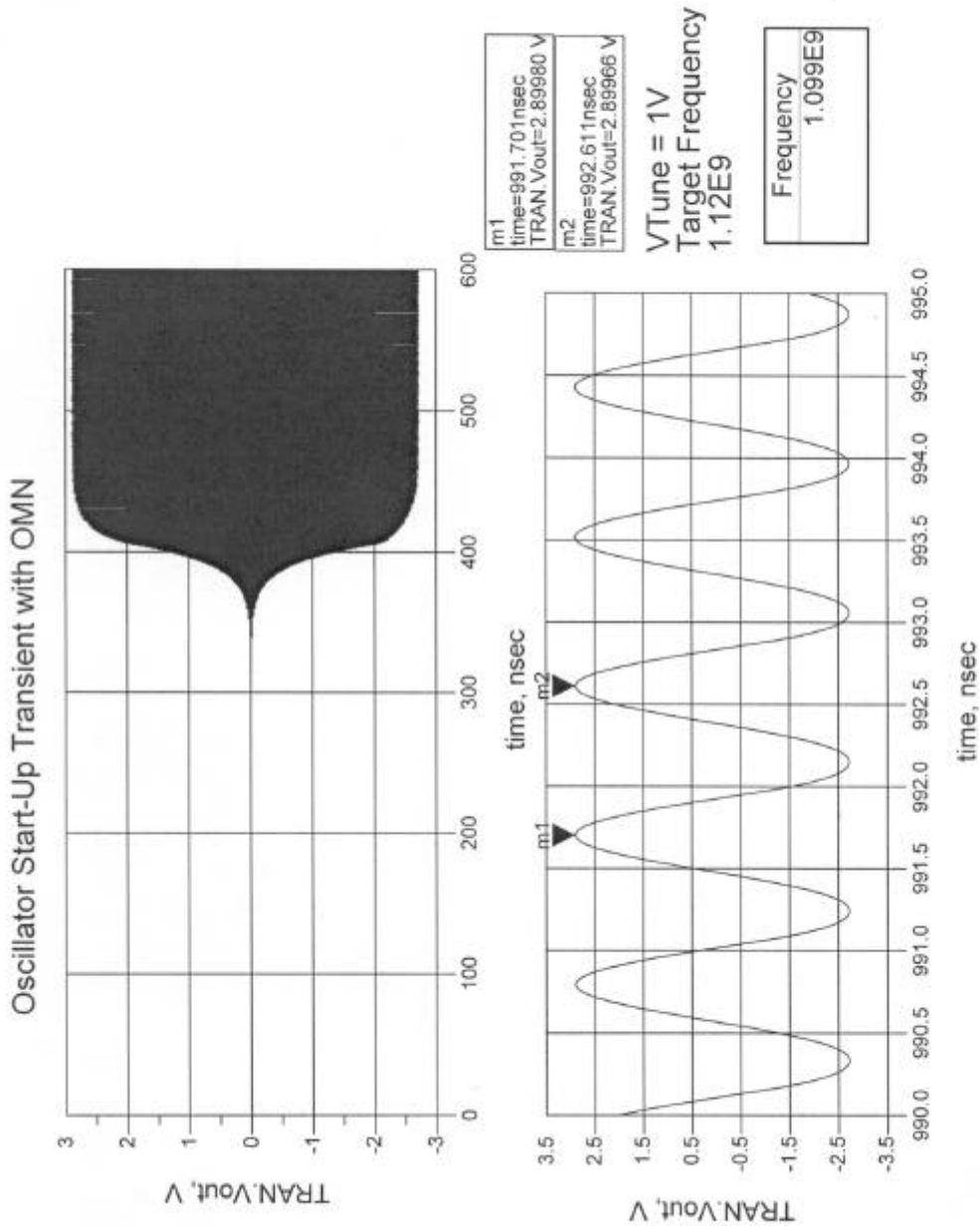
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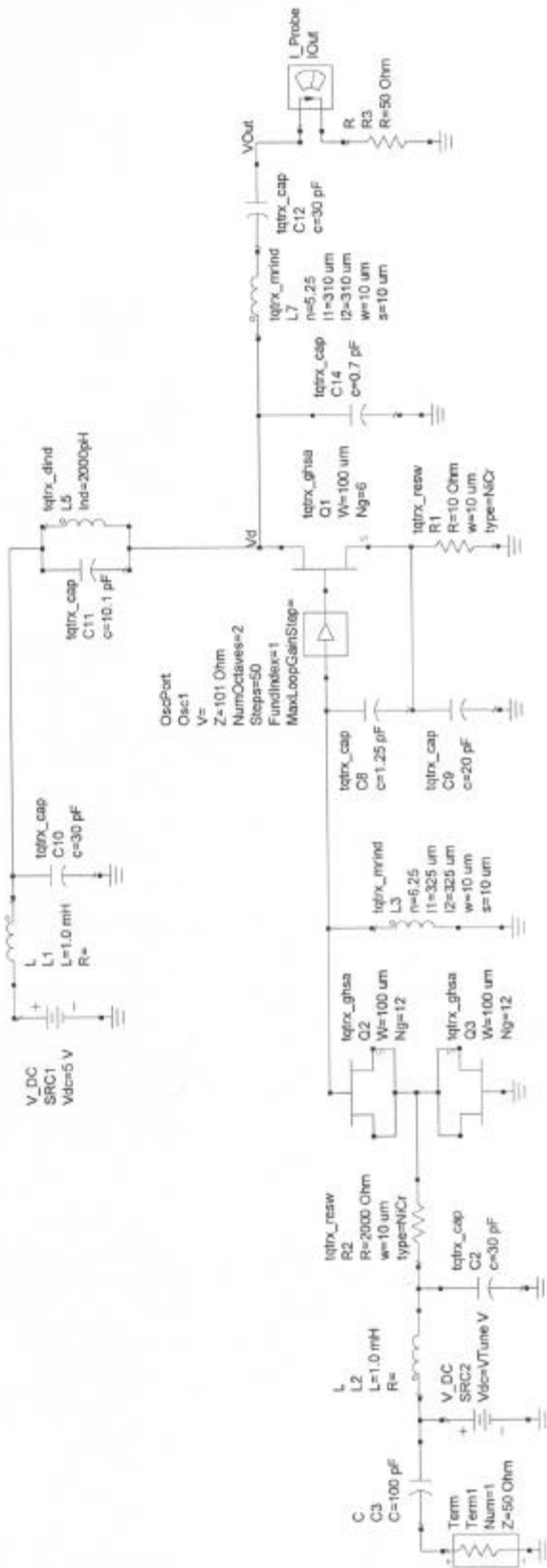
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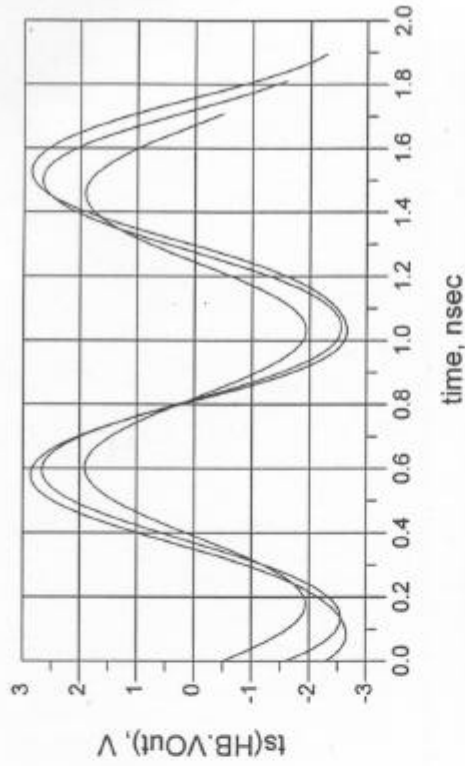
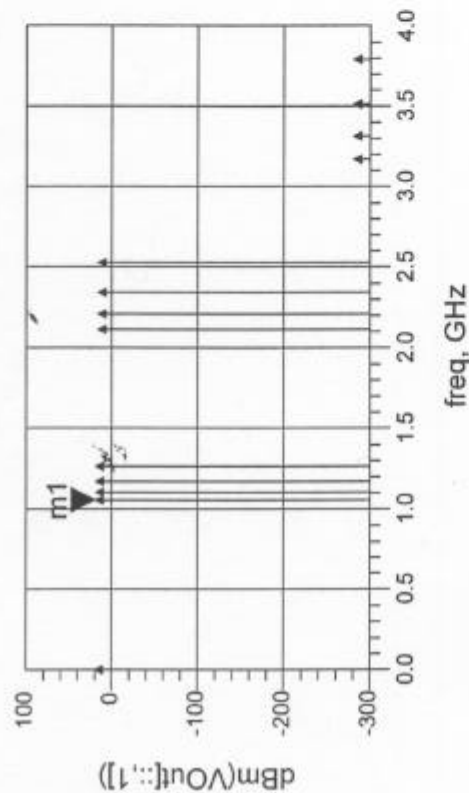
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Harmonic Balance Simulation Results without Layout Interconnects



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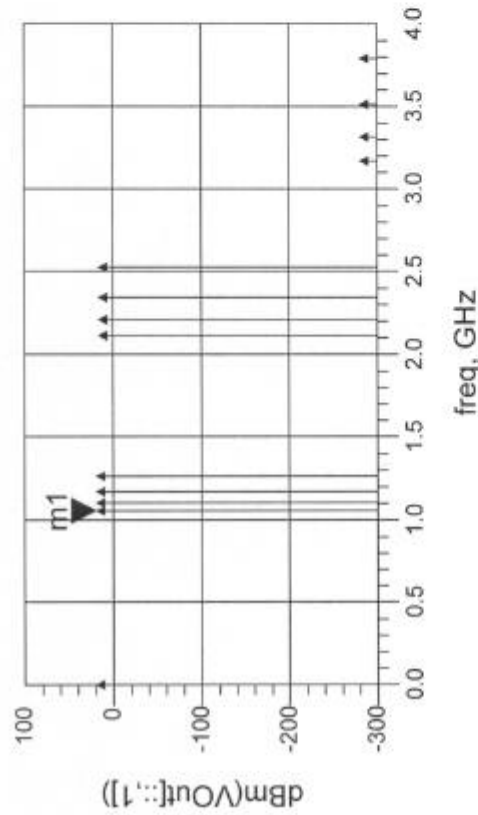
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Harmonic Balance Simulation Results without Layout Interconnects



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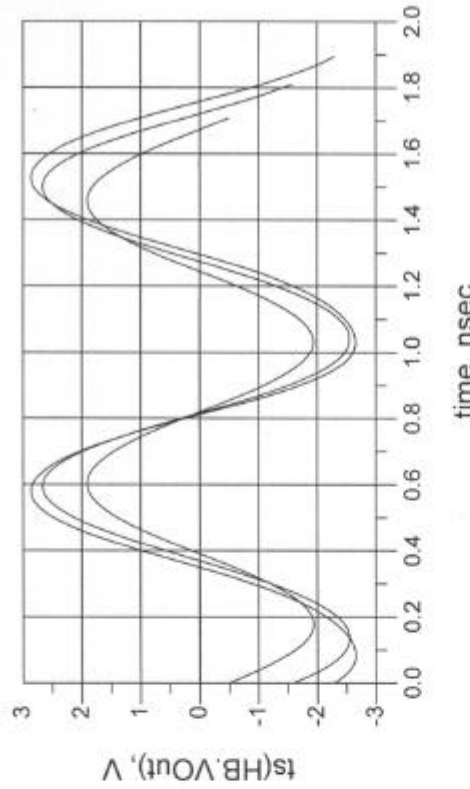
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