

Course Description

605.411 Foundations of Computer Architecture

This course provides a detailed examination of the internal structure and operation of modern computer systems. Each of the major system components is investigated including the following topics: the design and operation of the ALU, FPU and CPU; microprogrammed vs. hardwired control, pipelining, RISC vs. CISC machines; the memory system including caches and virtual memory; parallel and vector processing, multiprocessor systems and interconnection networks; superscalar, superpipelined and VLIW systems; as well as bus structures and the details of low level I/O operations using interrupt mechanisms, device controllers and DMA. The impact of each of these topics on system performance is also discussed. The instruction set architectures and hardware system architectures of a number of different machines are examined and compared as examples of systems that make use of the concepts, techniques and architectural features discussed in the course.

Prerequisite: A course in programming with a high-level language such as C, C++ or Java, as well as an introductory course in basic computer organization and assembly language programming (including computer arithmetic and the internal representation of data.) May be taken concurrently with 605.401 Foundations of Software Engineering.

Text: Patterson, D.A. and Hennessy, J.L., "Computer Organization and Design The Hardware/Software Interface", Morgan Kaufmann, third edition, 2005.

References:

1. Stallings, W., "Computer Organization and Architecture", Prentice Hall, fourth edition, 1995.
2. Tanenbaum, A. S., "Structured Computer Organization", Prentice Hall, third edition 1990.
3. Baron, R.J. and Higbie L., "Computer Architecture", Addison-Wesley, 1992.
4. Kane, G. and Heinrich, J., "MIPS RISC Architecture", Prentice-Hall, 1992

Note: Since this is not a programming course and students are expected to be familiar with assembly language programming, no lab assignments are given. However, there is a cross-assembler and simulator available for students to use in investigating the architecture of the MIPS machine described in the course.

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Course Outline

Class 1

Review of the classical von Neumann Architecture
Classification of Computer Architectures
Instruction Set Architecture
Hardware System Architecture
The Hierarchical View of Computer Systems
RISC versus CISC Approaches
Computer Performance Metrics
Overview of a RISC Architecture (MIPS)

Class 2

ALU Operation

Data Representation
Integer Arithmetic
Booth's Algorithm for Multiplication
Restoring and Non-restoring Division Algorithms
Floating Point operations and data

Class 3

The Digital Logic Level
ALU Implementation
CPU and Control Unit Implementation
The Data Path
Hardwired Implementation
Single versus Multiple Clock Cycle Implementation

Class 4

The Control Unit
Microprogrammed Implementation
Horizontal versus Vertical Microprogramming
Microprogramming Examples
Exceptions

Class 5

Pipelined Processors
Data Pipelining
Instruction Pipelining

Class 6 Mid Term Review

Class 7 Mid Term Examination

Class 8

Pipeline Control and Data Hazards
Superpipelining
Multiple Functional Units
Superscalar Machines
VLIW machines

Class 9

Memory Types
Memory Organization
 Segmentation
 Banked Memory
 Interleaved Memory
Cache Memory
Associative Memory
Virtual Memory and Paging

Class 10

The I/O System
Direct Programmed Controlled I/O
Direct Memory Access
Hardware Interrupt Mechanisms
System Interconnection and Bus Systems

Class 11

SISD, SIMD and MIMD Machines
Parallel Processors
Array Processors
Vector Processors

Class 12 Example Architectures

Class 13 Final Review

Class 14 Final Examination

Computer Science 605.411
Foundations of Computer Architecture

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Grading:	8 problem sets	(50% of overall grade)
	Midterm exam	(25%)
	Final exam	(25%)