

# **Digitally Controlled C Band Attenuator**

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## **Abstract**

A digitally controlled attenuator operating over a frequency band from 5150 MHz to 5875 MHz is described in this paper. The circuit was designed and modeled using the Advanced Design System (ADS) software package by Agilent. The design technique allowed for very precise selection of attenuation. The simulations of the circuit showed stable performance across a broad frequency band. A layout for a physical design was also completed as part of the project.

## Introduction

The description of this project will start with the list of specifications. I will then outline the designs considered for the project and the reason behind the one selected. The procedures used to finalize this design and implement the layout will be discussed. I will conclude with the simulation results and a plan for testing the circuit.

Numerous systems require precisely controlled power levels at different points in the system. One way to accomplish this is a variable attenuator. The specifications for the digital attenuator describe in this paper are shown below in Table 1.

FREQUENCY	5150 to 5875 MHz
BANDWIDTH	> 800 MHz
INSERTION LOSS	< 3 dB min IL (2 dB goal)
POWER HANDLING	> +10 dBm @ 1 dB compression
VSWR, 50 Ohm	< 1.5:1 input & output
SUPPLY VOLTAGE	$\pm 5$ Volts
CONTROL	TTL
SIZE	60 x 60 mil ANACHIP

Table 1. Circuit Requirements

In addition to these listed requirements, the attenuation is required to range from 0 dB to 6dB in four 2 dB steps. It should be mentioned that the insertion loss of the system, which is a built in attenuation, will be added to the variable attenuation.

## Design Approach

Before discussing the mechanism for switching between attenuation levels, the method of attenuation must be looked at. A good attenuator should match perfectly to 50 Ohms and reduce the RF power by an arbitrary amount. Fortunately there are two well know designs for achieving these requirements shown in Figure 1.

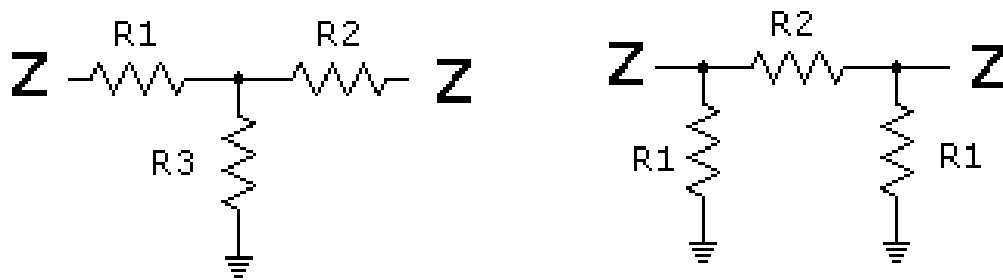


Figure 1. Designs for attenuators matched to 50 Ohms

The design on left was chosen because it requires only one via. These are the equations for determining R1, R2, and R3:

$$R1 = R2 = Z0 \frac{K-1}{K+1} \quad \text{Eqn. 1}$$

$$R3 = 2 * Z0 \frac{K}{K^2 - 1} \quad \text{Eqn. 2}$$

K is the attenuation level.

With the attenuator design we can move on to the method of control for the circuit. A number of designs were considered as possible mechanisms to allow for the switching between circuits. The first is shown in Figure 2. It is the most straight forward, but it also has a large number of components.

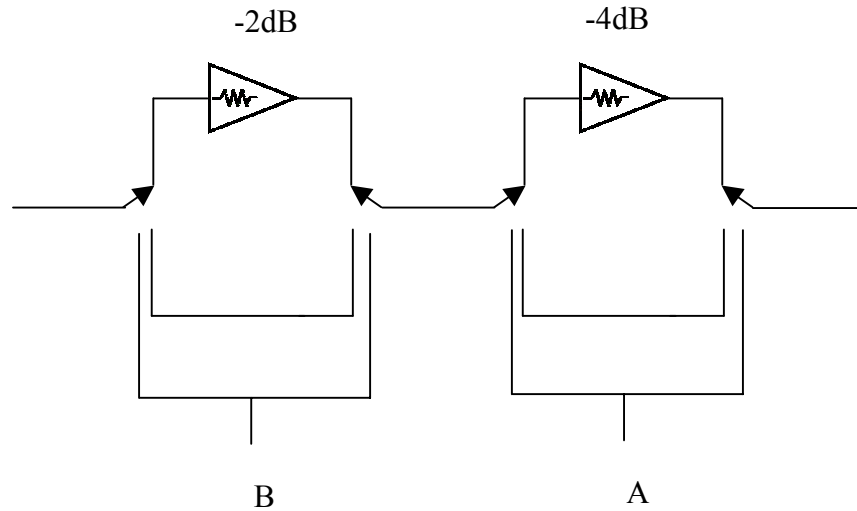


Figure 2. Possible designs for variable attenuator

Although this circuit might meet the requirements, it is needlessly complex and the large number of components could dissipate too much power to satisfy the insertion loss requirement. Figure 3 shows a much simpler design. Unfortunately, when the switch is closed, the 50 ohm line is in parallel with the attenuator. This has a resistance between one hundred and two hundred ohms. When put in parallel with the 50 ohm transmission line this results in an appreciable amount of attenuation. I was unable to meet the insertion loss requirements with this design.

This was overcome by inserting a switch between the attenuator and ground. The basic schematic for the switched is shown in Figure 4.

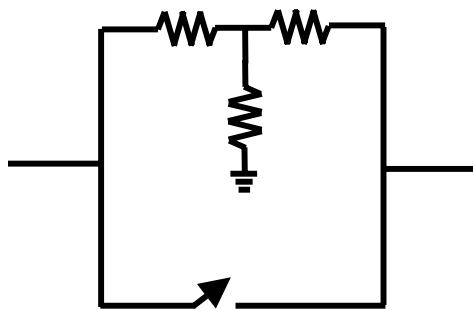


Figure 3. Simplified Circuit

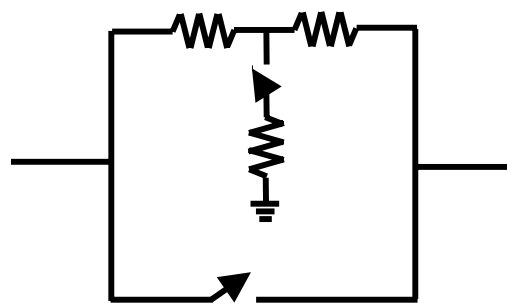


Figure 4. Final Attenuator

Prior to testing the circuit shown in Figure 3, the transistor was evaluated. The default transistor from the Triquint pallet showed low resistance, power handling over what is required by the circuit, and a small flat attenuation over the bandwidth of interest.

Using TTL logic, the on state has a minimum voltage of 2.0 V and the off state has a maximum voltage of 0.8 V. This means that there can be a maximum of 1.2 volts between the switch being open and into saturation. The circuit needs to perform well at these worst case values, and this performance cannot change significantly over the range of voltage allowed by the parameters of TTL logic. The transistor's S-parameters were measured at 0 volts and -1.2 volts. It turned out that it did perform well at the these values.

To meet all the requirements, the VSWR had to be made as small as possible. A simple two element matching network was added to the input and output. Blocking inductors were needed to isolate the gate from the RF line. A resistor that shifts the voltage into compliance levels for TTL was added. This elements are shown later in the report in the final circuit design.

The design and simulation of the circuit was an iterative process. The first simulation was done to verify the calculated values of the resistors. Several basic circuit layouts were simulated. The design gradually increased in complexity as more elements were added to comply with specifications. The next section will discuss the results of the simulation of the final circuit.

## Simulations

The circuit was simulated to determine its S-parameter characteristics in the four possible input states. The results of these simulations are shown below in Figure 4.

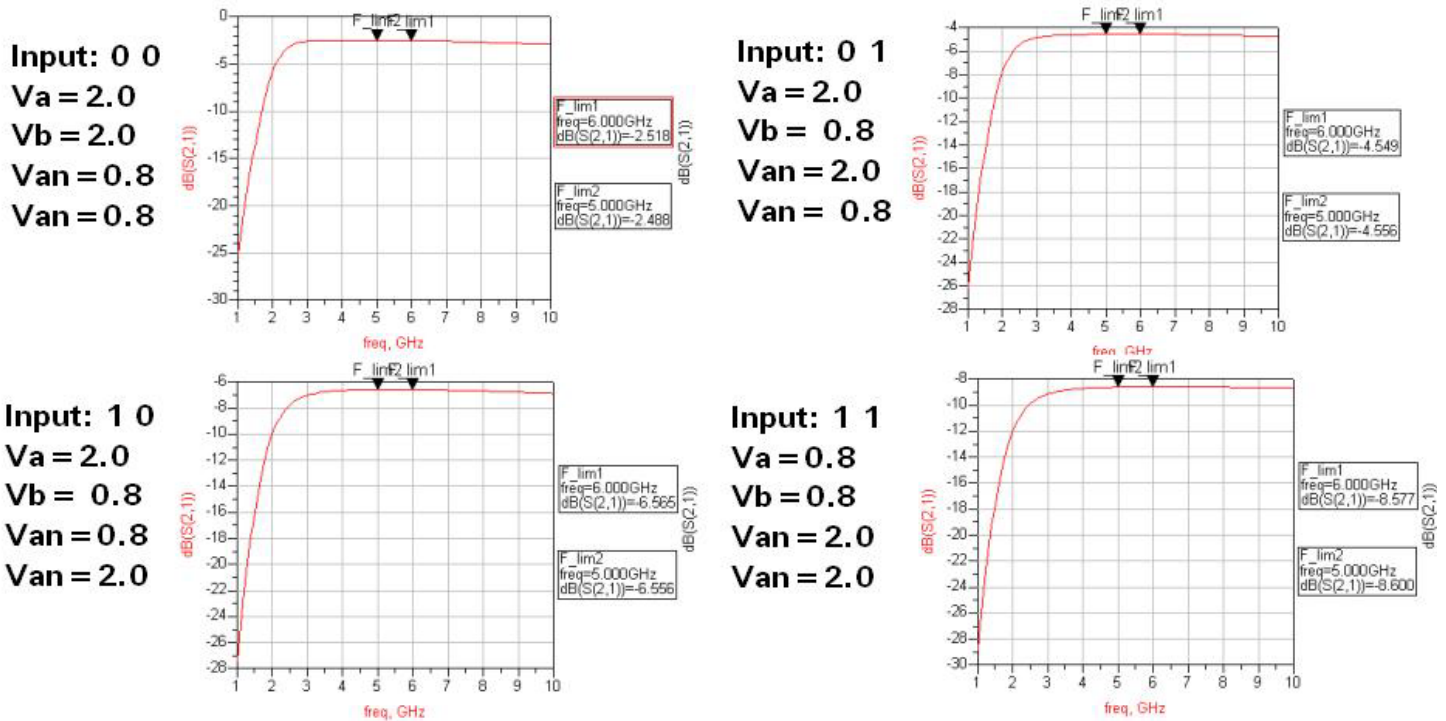


Figure 4. S-parameters of the attenuator in four logic states

As can be seen from this figure in the worst case scenario of voltages, the circuit easily meets the design specifications of four states separated by 2dB attenuation each. A typical value for the VSWR is shown in figure 5. The specifications call for a VSWR less than 1.5 which this circuit easily meets.

The final specification that has to be met is the power handling capabilities of the circuit.

The input RF power at 5.8 GHz was swept from a low value to 10 dBm. Figure 6 shows the results of this test.

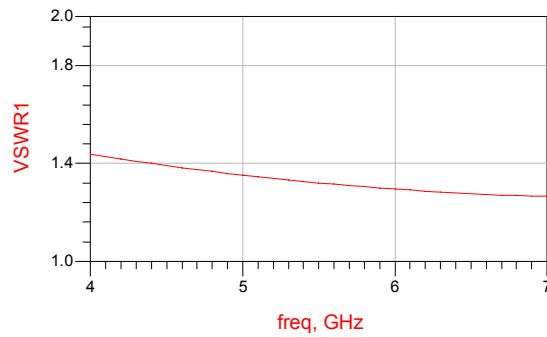


Figure 5. VSWR of the circuit

In figure 6, the linearity of the circuit begins to break down near the limit. It should be noted that the output power is plotted on the horizontal axis and that the input power should be increased by the attenuation level.

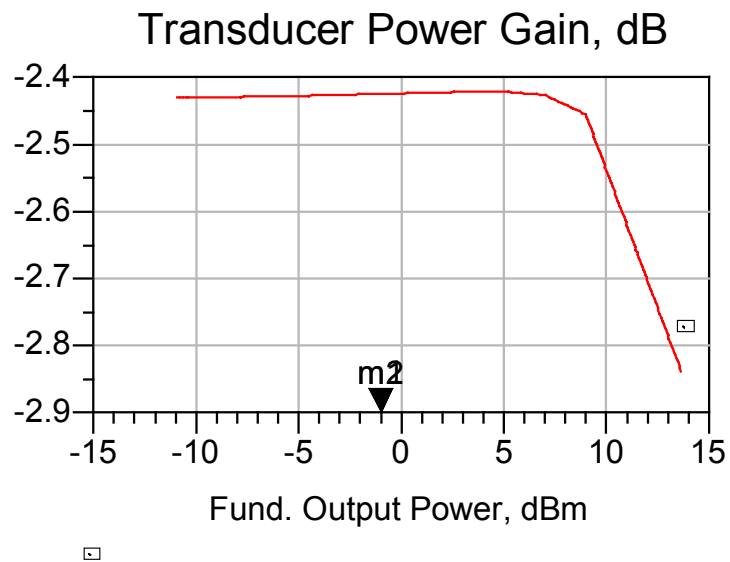


Figure 6. Power Sweep

The DC performance of the circuit was simulated. The circuit draws very little current. During the design, it became obvious that the voltage level of the circuit

would have to be shifted in order to allow it to be driven by TTL. The results of the DC simulation are shown in Figure 7.

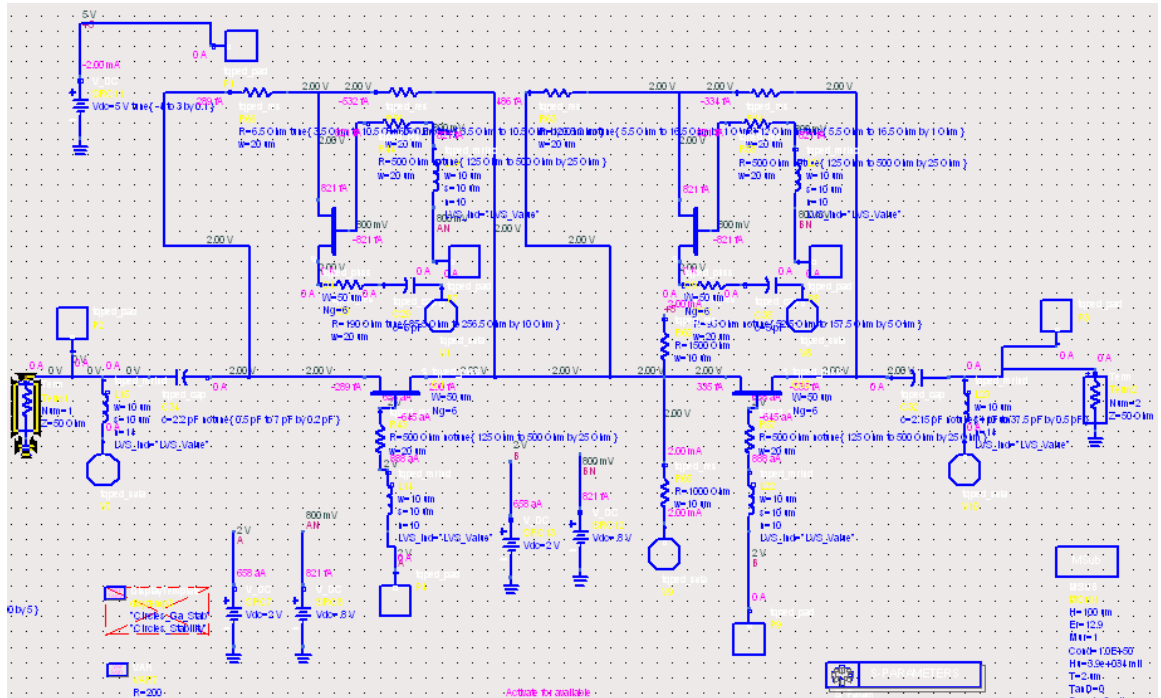


Figure 6. DC annotated Circuit layout.

The next section will discuss the components of the layout.

## Schematic

Figure 7 shows the annotated DC solution with the components of the circuit labeled.

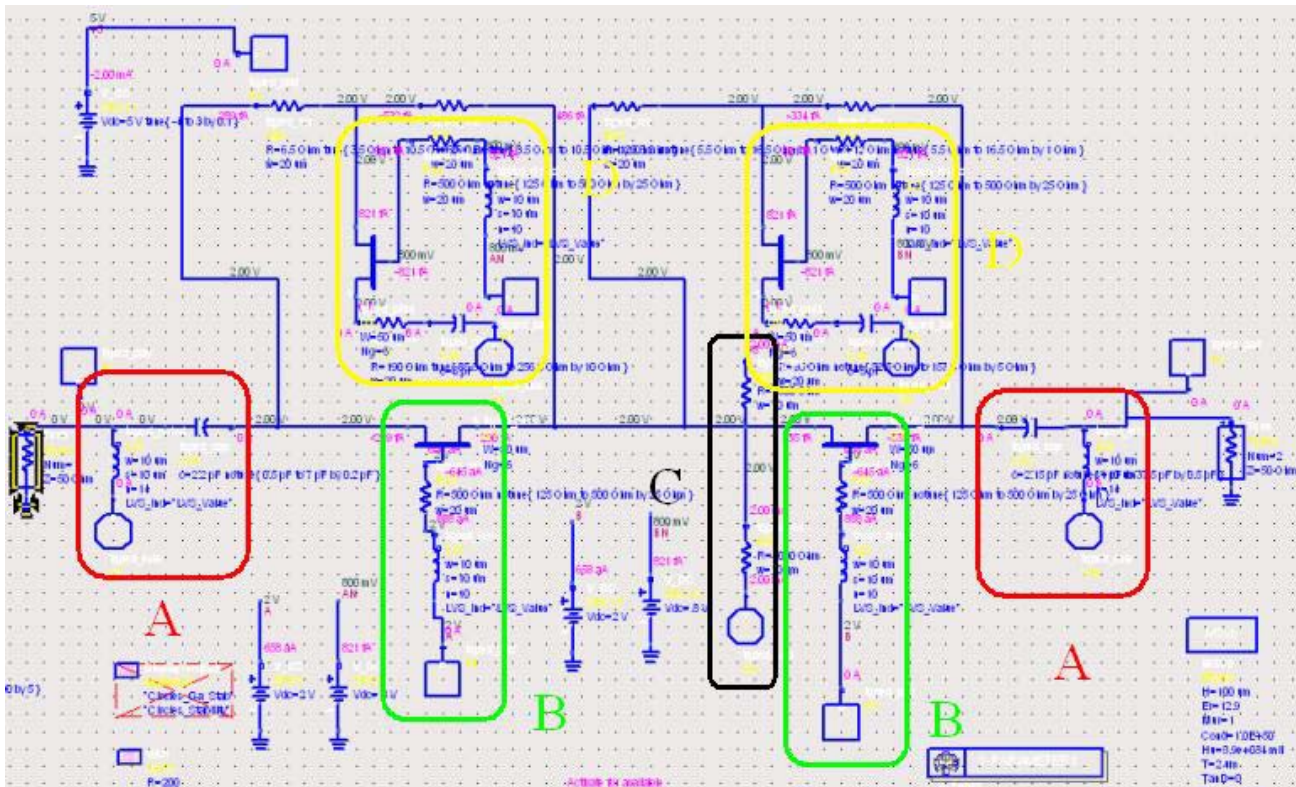


Figure 7. Annotated Layout of the circuit.

- A. Matching network
- B. Through switch and control pad
- C. Voltage shifter
- D. Attenuator switch and control pad

## Layout

Figure 8 shows layout of the circuit.

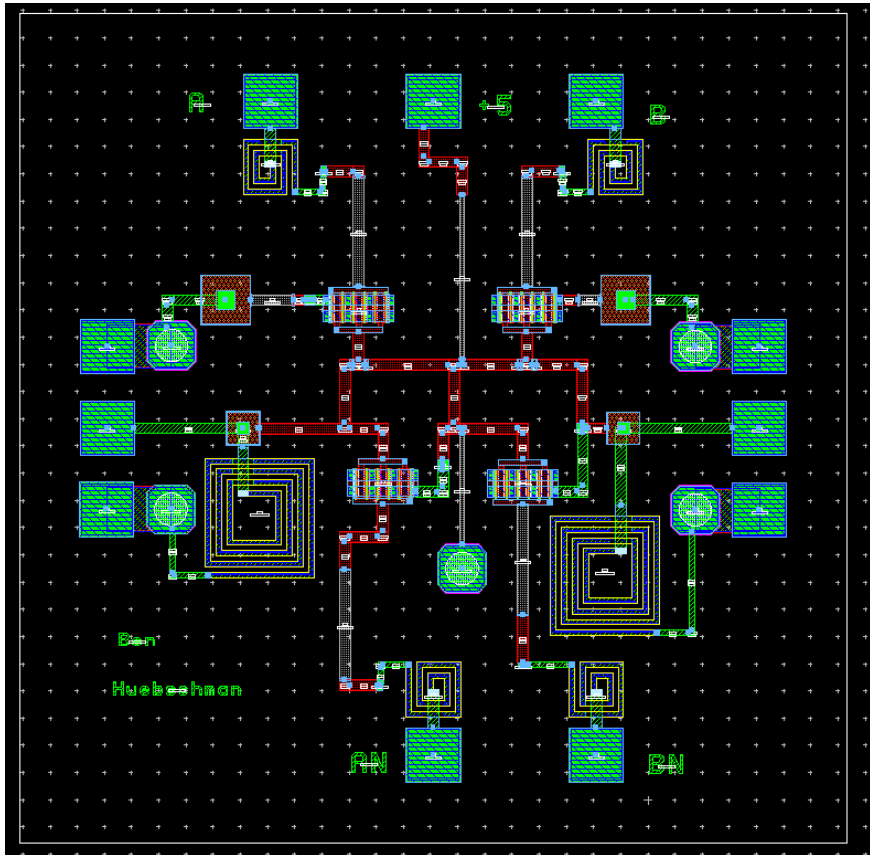


Figure 8. Circuit Layout

## **Test Plan**

To thoroughly test the circuit, we would need a vector network analyzer, a mechanism for measuring power, and DC power sources to bias the circuit. If we are just interested in validating the attenuation, the power measurement system is unnecessary. The test will begin by connect the DC bias and the network analyzer. S-parameters for each of the four logic states would be measured. From these we could extract attenuation and VSWR. To test the power response of the system, the vector network analyzer would have to be replaced by the power source at the desired frequency and a power meter. The power would then be increased until we began to observe changes in the attenuation.

## **Summary**

This paper describes the design procedure and layout of a digitally controlled variable attenuator. The circuit fulfills are design requirements and specifications. It consumes virtually no DC power. It uses as a power source a +5 V DC input, but this could be reduced to +2 V. The circuit could easily be redesigned to have any number of steps or an arbitrary attenuation level. As the voltage requirements for the transistors decreases, the required voltage of the DC power could be reduced appropriately. This basic design can be adapted to other attenuator requirements.