



EE525.787 – Microwave Monolithic Integrated Circuit (MMIC)
Engineering and Applied Science Programs for Professionals

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C-Band Low Noise Amplifier (LNA)

Microwave Monolithic Integrated Circuit (MMIC)

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1 Abstract

This report gives the detail description for a GaAs Low Noise Amplifier (LNA) Monolithic Microwave Integrated Circuit (MMIC), designed for use in a duplex transceiver as part of the first stage of a receive array operating in the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies.

2 Introduction

As the first stage of the receive array of the duplex transceiver, the LNA receives signals in the WLAN and ISM frequencies. It then processes these signals and outputs to the next stage as input with 15 dB gain and a noise figure of less than 2 dB.

3 Design Approach

The initial approach was to design a LNA that would meet the design specifications. The first step was to select a linear transistor model to use. After the linear transistor was chosen, it needed to be stabilized. Three different stability circuits were looked at which was a series resistor, a series and shunt resistor, and a feedback resistor configuration. After running the simulation for each circuit configuration, it was apparent that the specifications could not be met with a single stage design and thus two stages were needed to meet or exceed the requirements. I decided to try each combination of the circuits cascaded and recorded the results for each one at 5.5 MHz. The results are tabulated below.

Circuit	Gain dB(S21)	Input Match dB(S11)	Output Match dB(S22)	Mu1	MuPrime 1	nf(2)	Nfmin
5a	20.391	-3.960	-29.202	1.858	1.212	2.630	2.374
5b	19.983	-8.083	-11.643	2.505	1.866	2.607	2.369
5c	12.068	-2.663	-5.250	1.743	1.325	2.601	2.353
5d	13.064	-11.668	-4.993	1.714	3.461	2.602	2.361
5e	15.437	-2.581	-13.842	3.345	1.282	2.561	2.324
5f	15.385	-9.872	-12.095	3.637	2.868	2.586	2.342
5g	24.714	-0.023	-13.520	0.009	0.737	0.999	0.997
5h	9.124	-3.584	-7.969	2.401	1.487	3.788	3.237
5i	0.097	-3.514	-4.800	1.734	1.496	4.203	3.538
5j	2.463	-3.503	-4.669	1.706	1.493	3.913	3.329
5k	2.138	-3.540	-12.172	4.020	1.500	4.066	3.439
5l	3.944	-3.529	-11.406	3.669	1.497	3.914	3.331
5m	12.516	-2.825	-11.289	3.171	1.347	2.604	2.311
5n	13.804	-2.884	-8.999	2.410	1.338	2.470	2.223
5o	4.783	-2.674	-4.870	1.738	1.355	2.615	2.320
5p	7.374	-2.701	-4.813	1.724	1.357	2.493	2.239
5q	6.988	-2.728	-12.326	3.985	1.363	2.526	2.258
5r	9.128	-2.715	-11.491	3.576	1.357	2.470	2.223

I chose the circuit 5n because I felt this gave me the best tradeoff between gain, match, stability and noise figure and allowed me enough room to optimize the circuit.

After the linear circuit was stable and it met the requirements, I replaced the linear model with the non-linear TriQuint model and tuned the circuit to get the final results.

3.1 Specifications vs. Goals

For the design, the following specifications to design to were also my goals to achieve.

	Specifications	Goals
Frequency	5150 – 5875 MHz	5150 – 5875 MHz
Bandwidth	> 800 MHz	> 800 MHz
Gain	> 15 dB	> 15 dB
Gain Ripple	± 0.5 dB	± 0.5 dB
Noise Figure	< 3 dB	< 3 dB
Input IP3	> + 5 dBm	> + 5 dBm
VSWR, 50 Ohm	< 1.5:1	< 1.5:1
Supply Voltage	+ 5 Volts	+ 5 Volts
Size	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP

3.2 Tradeoffs

The LNA design has many tradeoffs associated with it such as balancing gain, stability, match and noise figure. This particular design has its major tradeoff between gain and noise figure. Care was taken to not over compensate for one by sacrificing the other. By tuning the output matching circuit of the second stage, I was able to achieve my goal of 15 dB gain while also achieving a noise figure less than 2 dB.

3.3 Circuit Description

The LNA is a two-stage design with two transistors cascaded using the output from the first stage as the input to the second stage. Each stage was designed to fulfill different purposes. The first stage for low noise and the second stage for output match and gain bandwidth. Both stages of the LNA utilize a TriQuint 6x50 0.5 μ m PHEMT biased at 3V of drain voltage and 15 mA drain current.

The first stage of the LNA utilizes a series and shunt resistor for stability. Because this particular design has very low noise, it is used in the design as the first stage since this stage sets the overall noise figure.

The second stage of the LNA utilizes a feedback resistor for stability. This design is used in the second stage to improve output match and increase the gain bandwidth of the amplifier.

4 Simulations

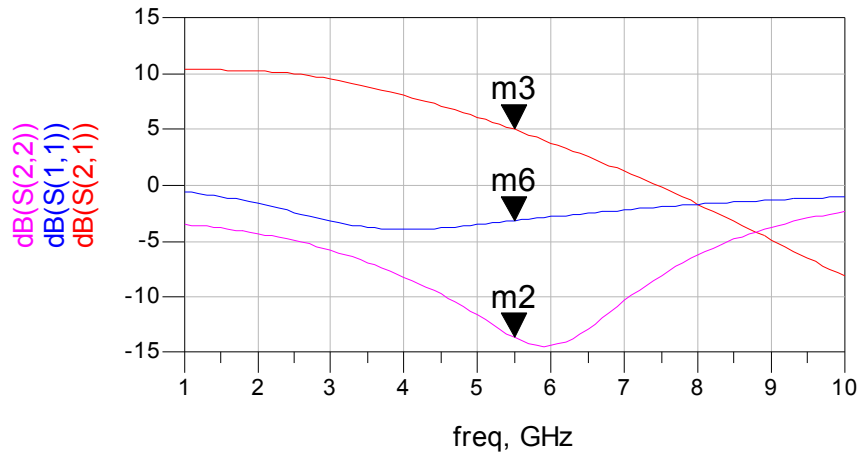
4.1 Linear

4.1.1 First Stage Gain $S(2,1)$, Input Match $S(1,1)$, Output Match $S(2,2)$

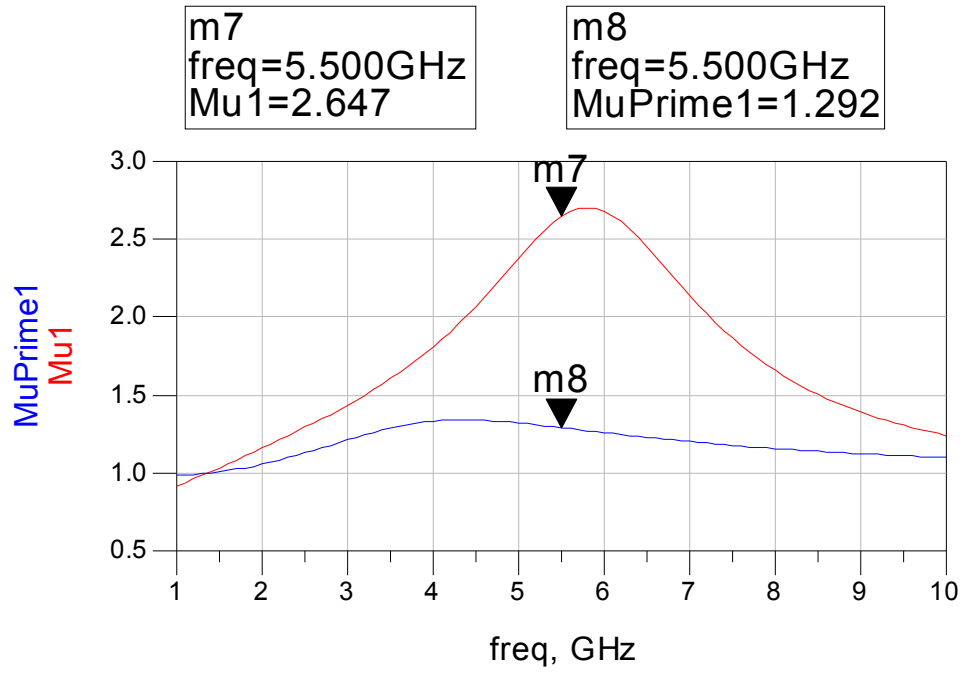
m3
freq=5.500GHz
dB(S(2,1))=5.001

m6
freq=5.500GHz
dB(S(1,1))=-3.157

m2
freq=5.500GHz
dB(S(2,2))=-13.616



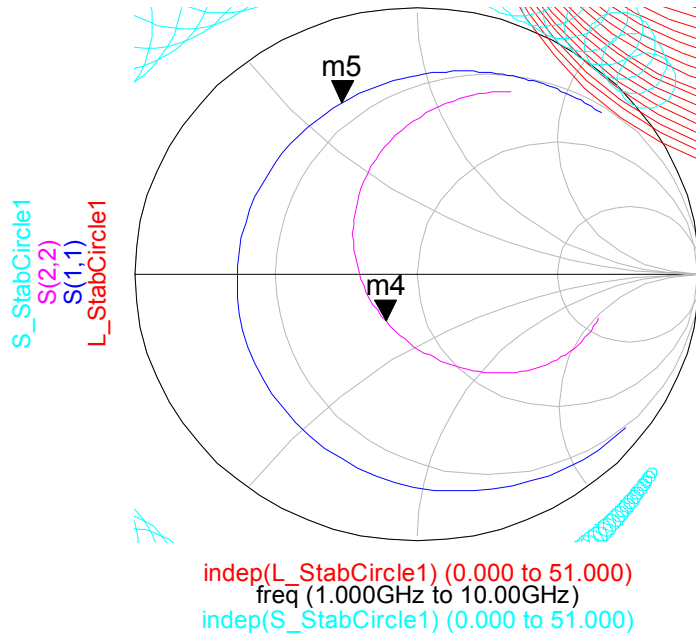
4.1.2 First Stage Stability



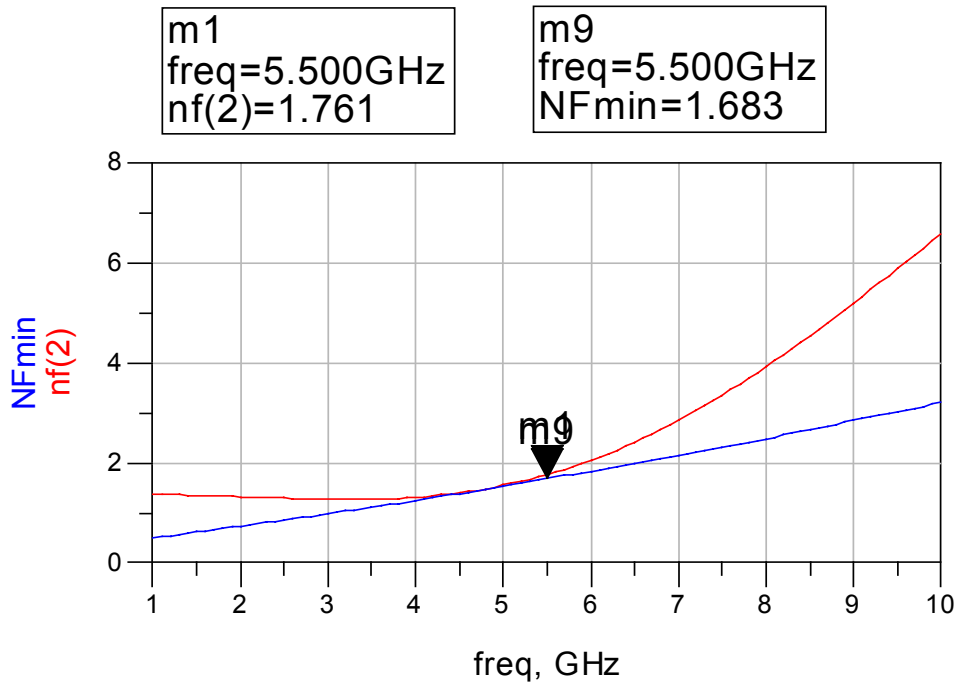
4.1.3 First Stage Stability (Smith Chart)

m4
freq=5.500GHz
S(2,2)=0.209 / -121.677
impedance = $Z_0 * (0.758 - j0.281)$

m5
freq=5.500GHz
S(1,1)=0.695 / 112.269
impedance = $Z_0 * (0.257 + j0.640)$



4.1.4 First Stage Noise Figure $nf(2)$, Minimum Noise Figure (Nfmin)

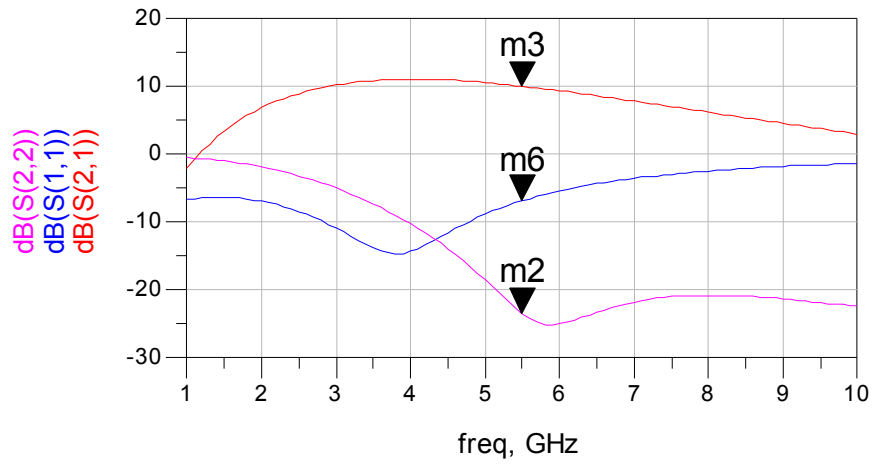


4.1.5 Second Stage Gain $S(2,1)$, Input Match $S(1,1)$, Output Match $S(2,2)$

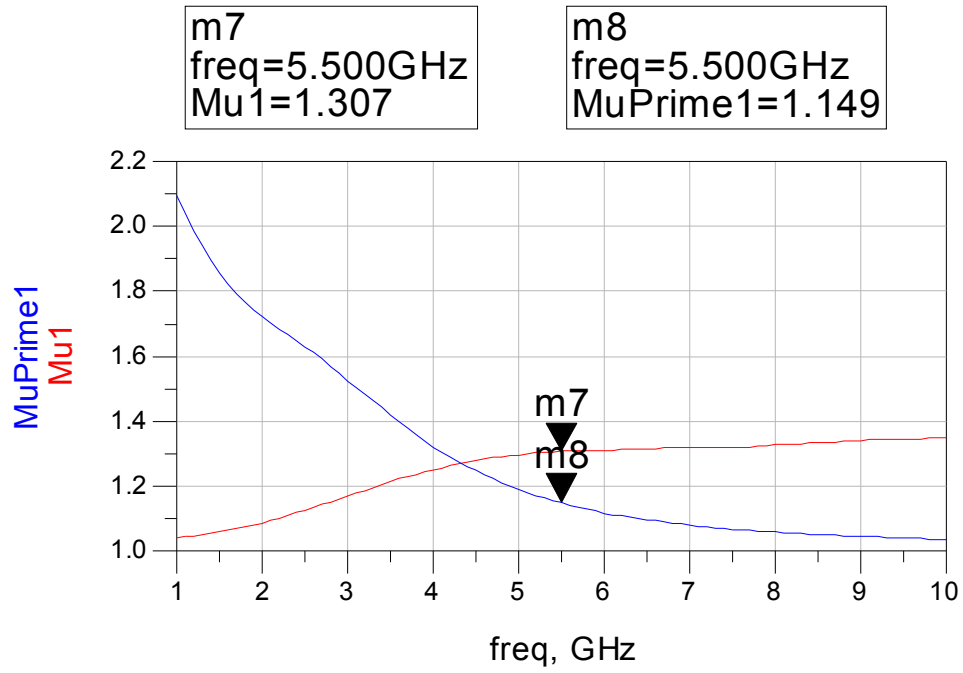
m3
freq=5.500GHz
dB(S(2,1))=10.019

m6
freq=5.500GHz
dB(S(1,1))=-6.804

m2
freq=5.500GHz
dB(S(2,2))=-23.397



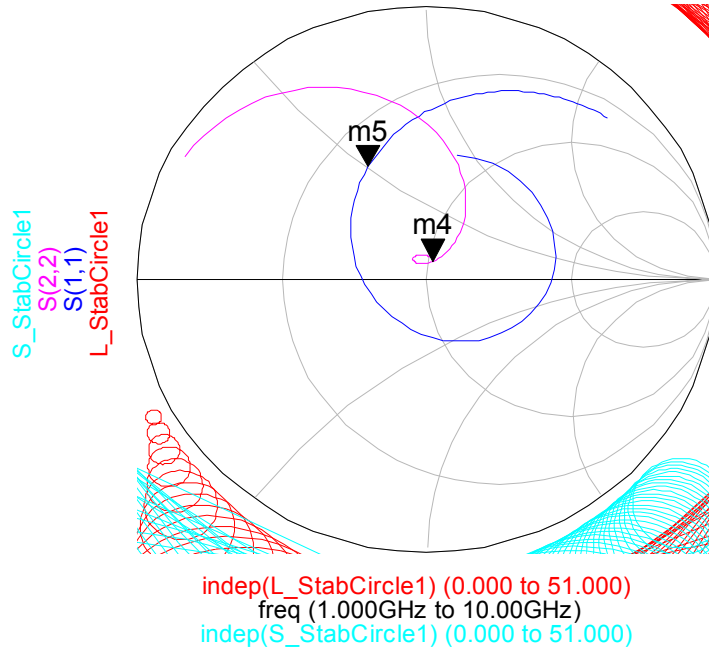
4.1.6 Second Stage Stability



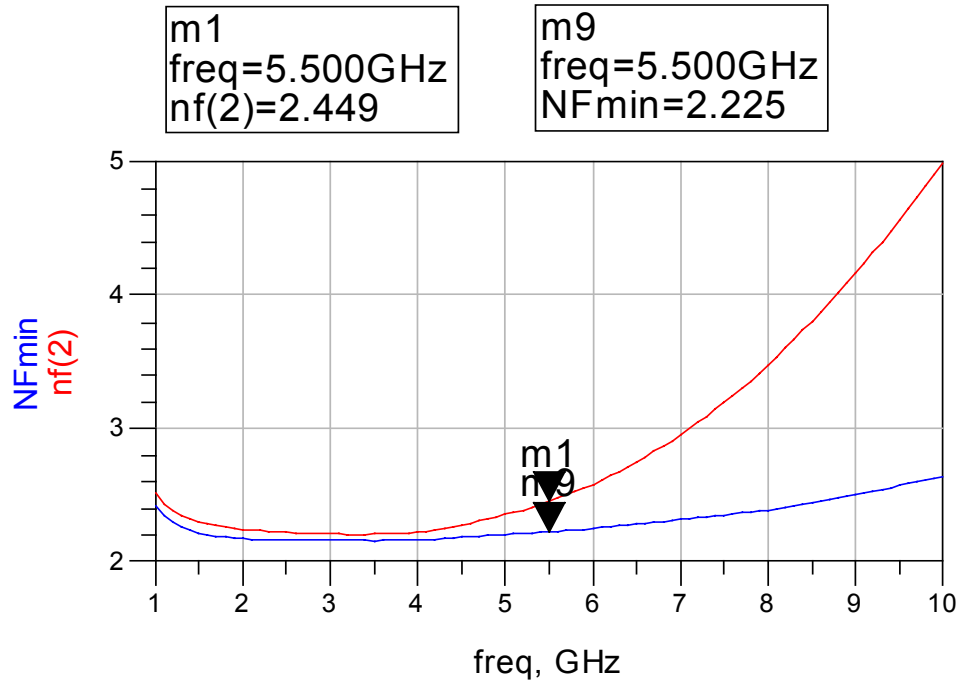
4.1.7 Second Stage Stability (Smith Chart)

m4
freq=5.500GHz
S(2,2)=0.068 / 71.084
impedance = Z0 * (1.036 + j0.133)

m5
freq=5.500GHz
S(1,1)=0.457 / 116.374
impedance = Z0 * (0.490 + j0.507)



4.1.8 Second Stage Noise Figure $nf(2)$, Minimum Noise Figure (Nfmin)

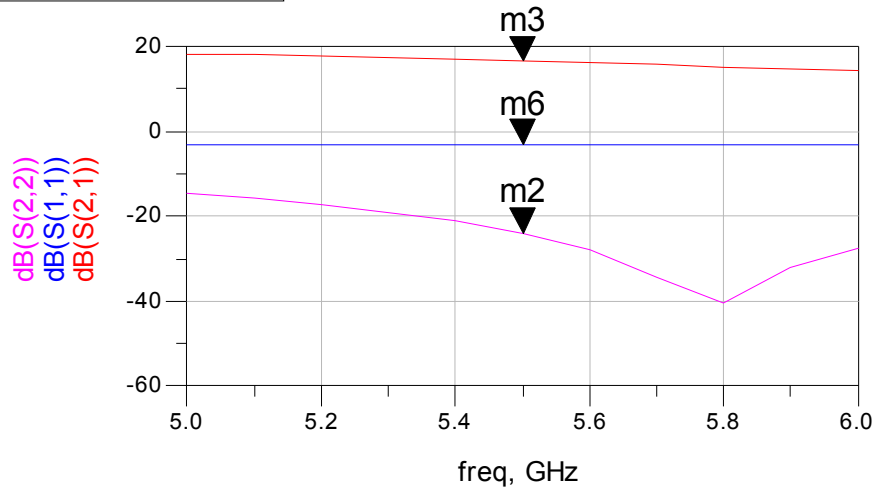


4.1.9 Both First and Second Stage Gain $S(2,1)$, Input Match $S(1,1)$, Output Match $S(2,2)$

m3
freq=5.500GHz
dB(S(2,1))=16.550

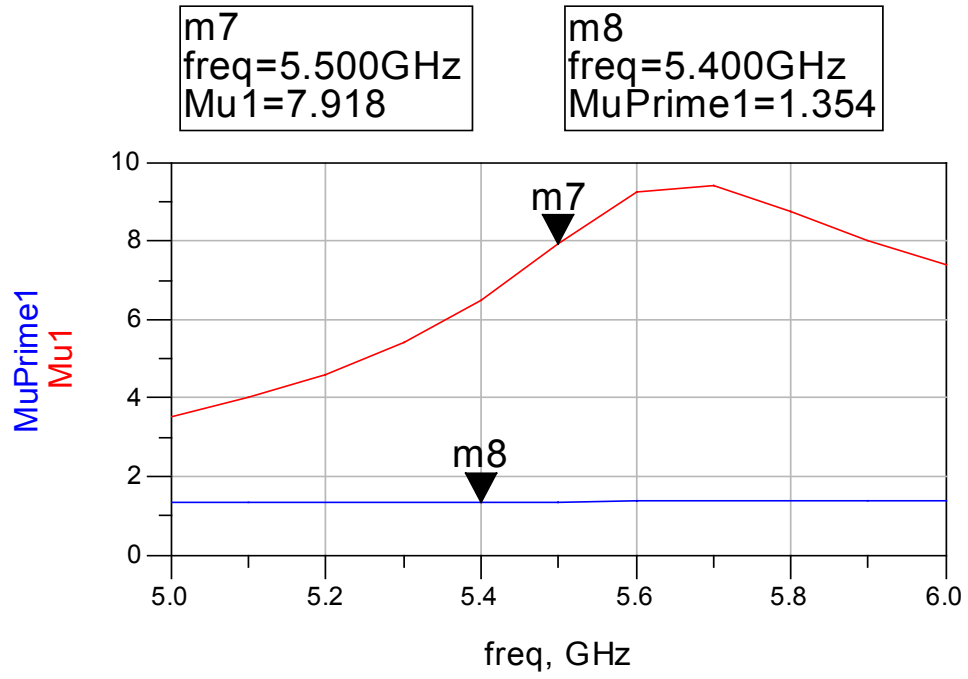
m6
freq=5.500GHz
dB(S(1,1))=-3.171

m2
freq=5.500GHz
dB(S(2,2))=-24.006



4.1.10

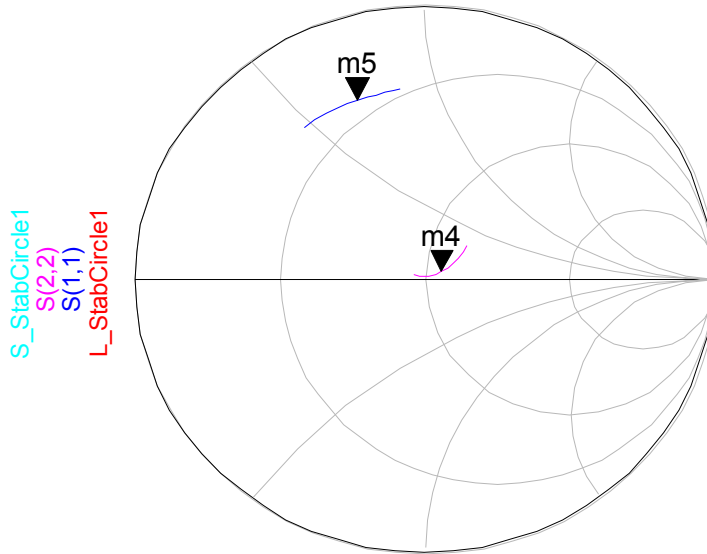
Both First and Second Stage Stability



4.1.11 Both First and Second Stage Stability (Smith Chart)

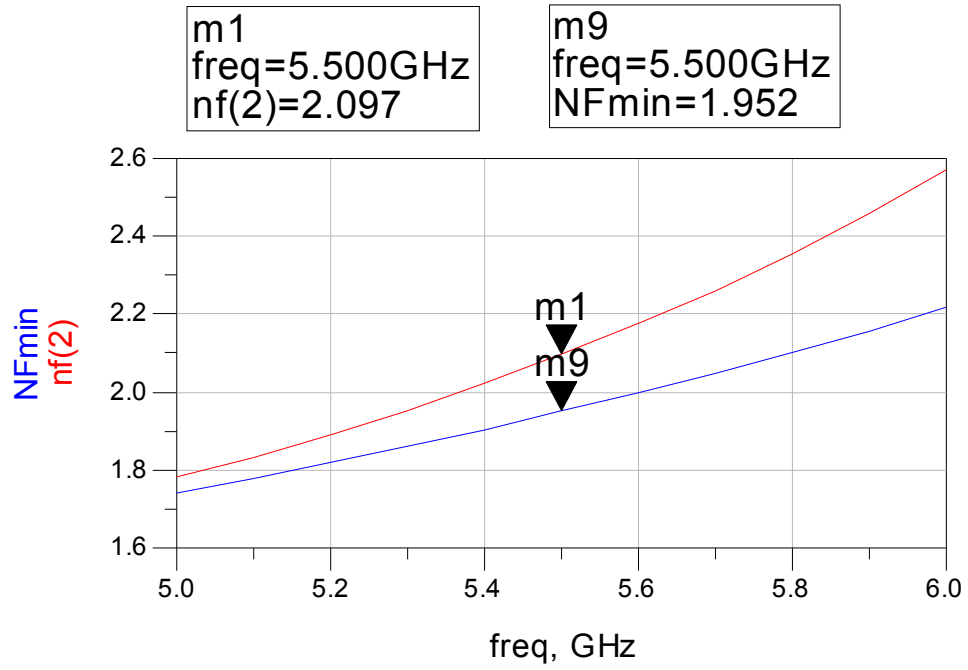
m4
freq=5.500GHz
S(2,2)=0.063 / 24.453
impedance = Z0 * (1.120 + j0.059)

m5
freq=5.500GHz
S(1,1)=0.694 / 109.534
impedance = Z0 * (0.266 + j0.672)



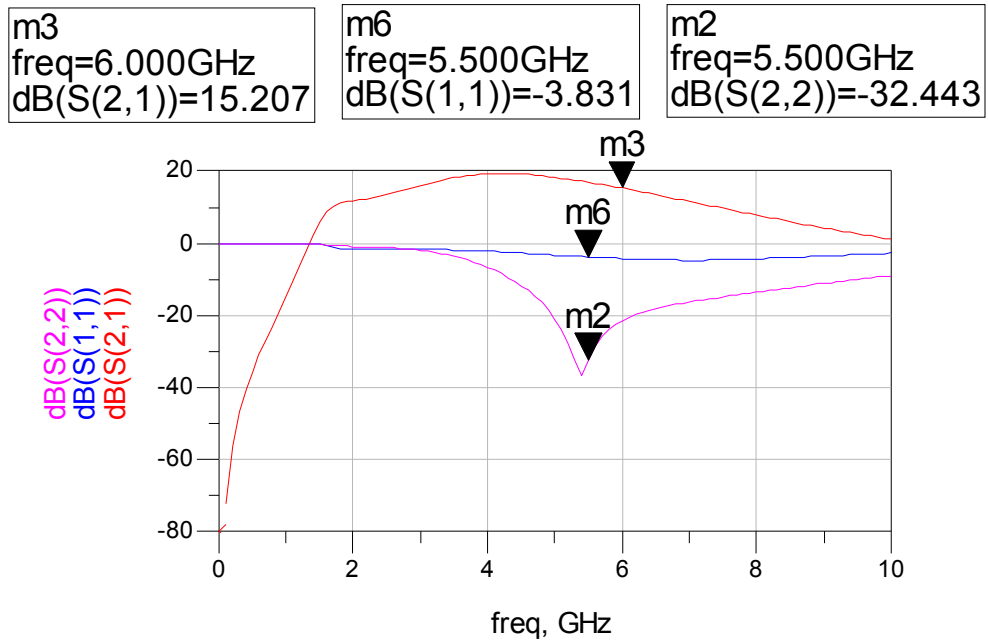
indep(L_StabCircle1) (0.000 to 51.000)
freq (5.000GHz to 6.000GHz)
indep(S_StabCircle1) (0.000 to 51.000)

4.1.12 Both First and Second Stage Noise Figure $nf(2)$, Minimum Noise Figure (Nfmin)

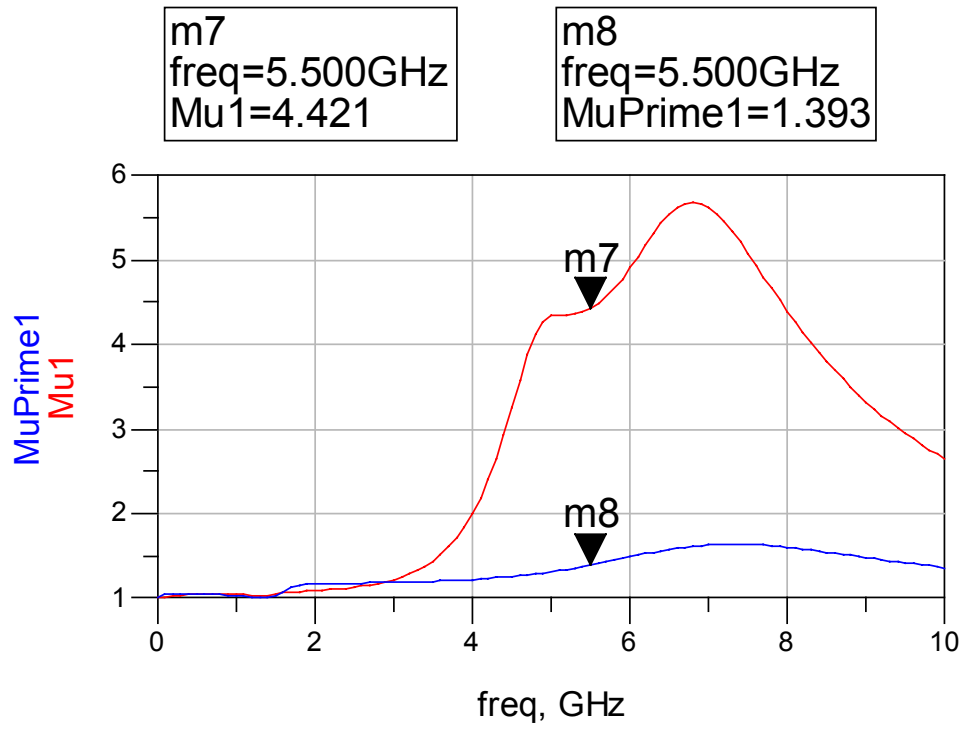


4.2 Non-Linear

4.2.1 Gain S(2,1), Input Match S(1,1), Output Match S(2,2)



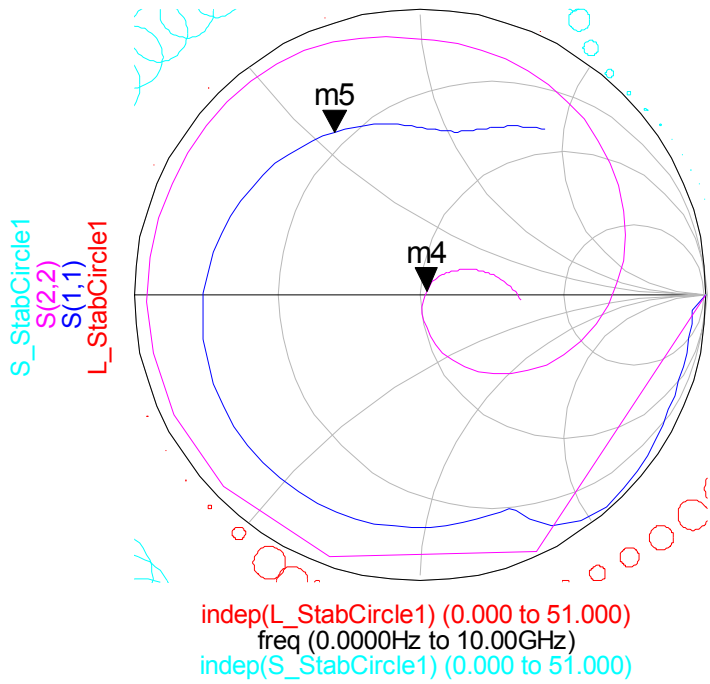
4.2.2 Stability



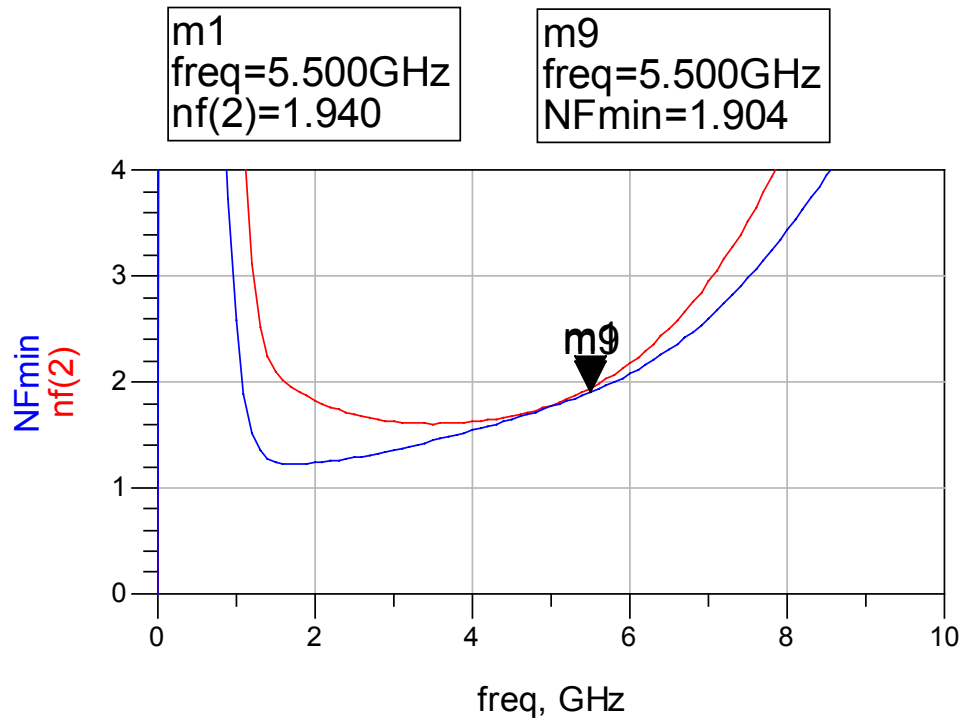
4.2.3 Stability (Smith Chart)

m4
freq=5.500GHz
S(2,2)=0.024 / 31.067
impedance = Z0 * (1.041 + j0.026)

m5
freq=5.500GHz
S(1,1)=0.643 / 117.824
impedance = Z0 * (0.291 + j0.565)



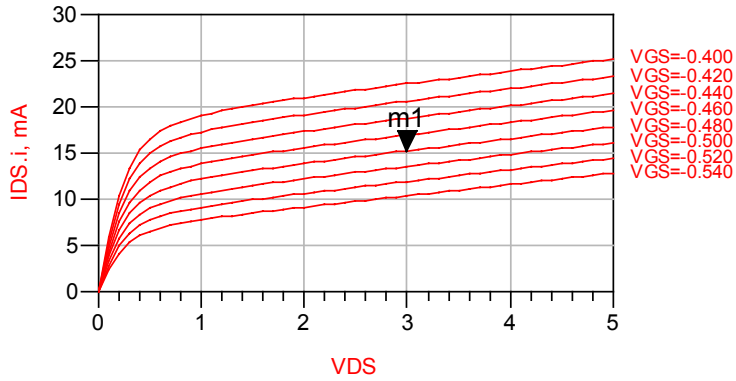
4.2.4 Noise Figure $nf(2)$, Minimum Noise Figure (Nfmin)



4.3 Bias

FET Bias Characteristics

Use with FET_curve_tracer Schematic Template



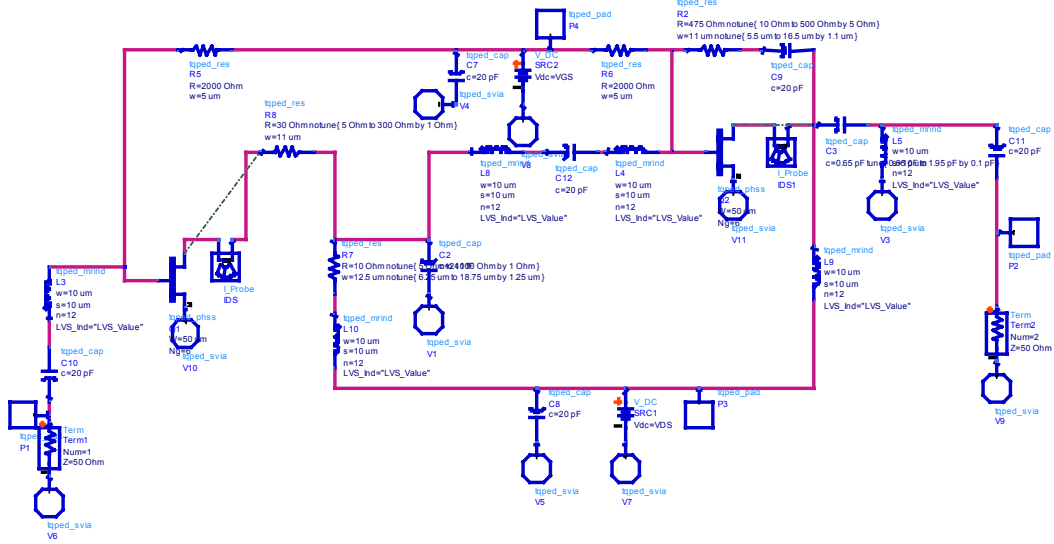
Values at bias point indicated by marker m1.
Move marker to update.

VDS	Device Power Consumption, Watts
3.000	0.046

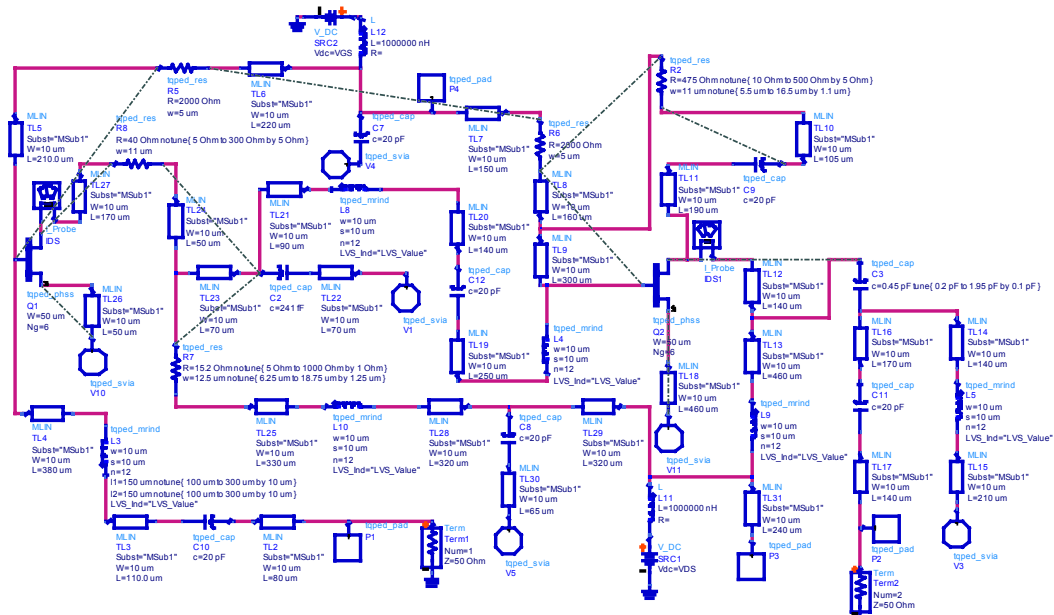
m1
VDS=3.000
IDS.i=0.015
VGS=-0.480000

5 Schematic

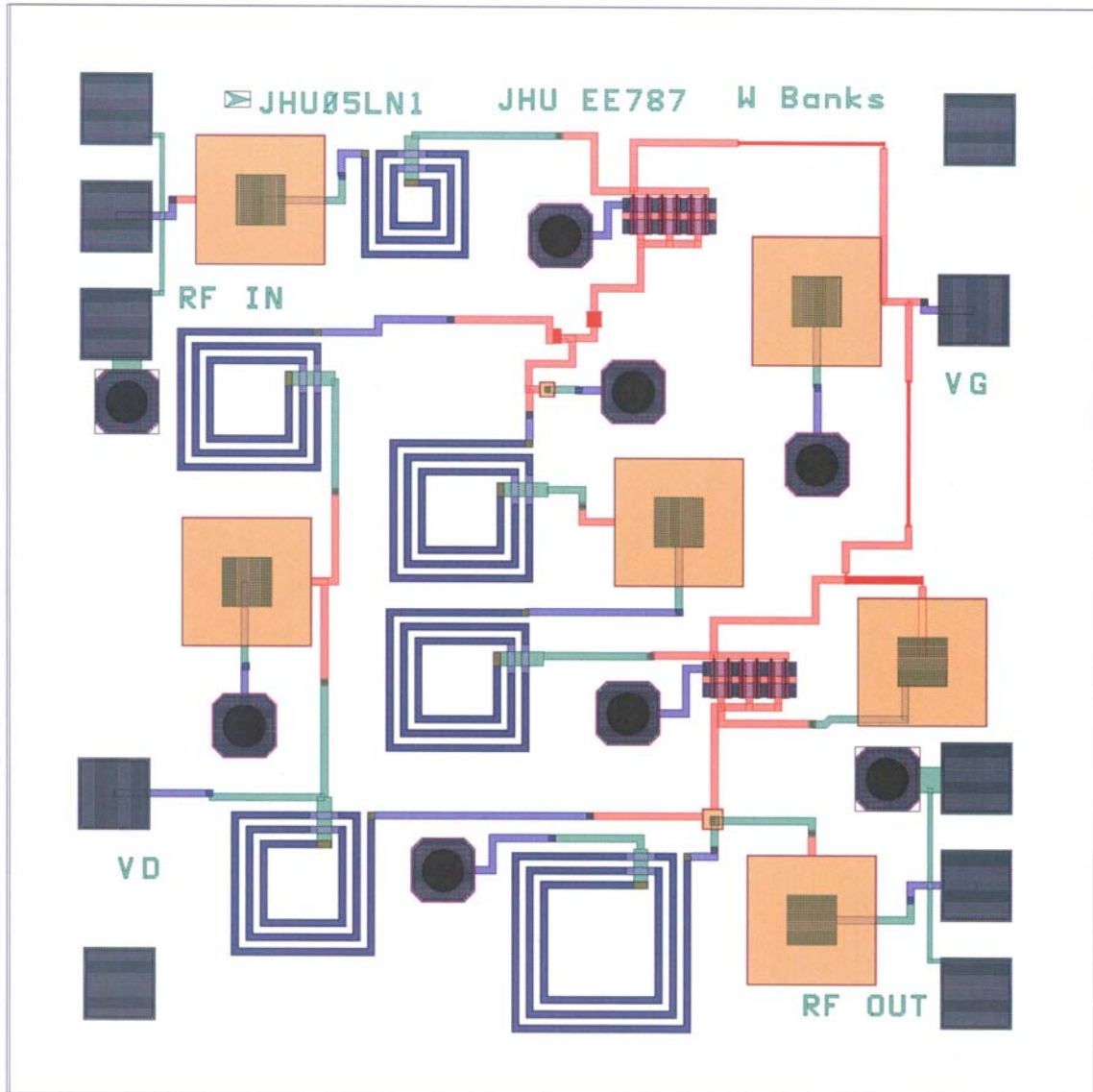
5.1 RF Schematic without interconnect



5.2 RF Schematic with interconnect



6 Layout Plot



7 Test Plan

Verifying the design of the LNA MMIC will require the measurement of such parameters as the noise figure and S-parameters.

7.1 Test Equipment

The use of the following test equipment is required to measure the performance of the LNA.

- Spectrum Analyzer
- Network Analyzer
- 5 volt DC Power Supply
- Power Meter

7.2 Turn On Procedure

Extreme caution should be used so as to prevent an excess of drain voltage and current from entering the circuit. The required voltage is +3 V DC and the required current is 30 mA for the LNA. Setting the correct limits on the DC supply is a must.

7.3 RF Measurements

The test equipment should be calibrated prior to performing any test on the LNA MMIC. Calibrate the analyzer from 1 – 10 GHz. The noise figure meter should be calibrated as well.

7.4 S-Parameters Measurements

After calibration of the test equipment, probes should be connected to the LNA and measurement of current and S11, S12, S21, S22 can be made and recorded.

7.5 Noise Figure Measurements

After calibrating the noise figure meter, position the probes on the VD pad and IN input pads and record the noise figure over the band of frequencies.

8 Summary & Conclusion

This report describes the design of a C-Band LNA MMIC designed to operate at 5.5 MHz using the TriQuint process. The design was simulated using Agilent Advanced Design System. The simulated model produced an LNA with gain of 15 dB or greater in the required frequency band and noise figure of less than 2 dB on a 300mm ANACHIP footprint. This designed was produced as part of the MMIC Design course taught at Johns Hopkins University of the Fall 2005 semester.