

C Band Low Noise Amplifier

Final Report

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Abstract

The design described in this document is a C-band, low-power low noise amplifier (LNA). It has a DC power consumption of 6.34mW at 1.7V and 3.73mA drain bias. It is layed-out to use dual supplies to aid in-lab tweaking of the bias of the 140um depletion-mode FET. The LNA has an operating band of approximately 5.15GHz to 5.875GHz. Within this band the noise figure is less than 2.35dB. Gain is better than 8.5dB across the band with port match better than -15dB. The amplifier is unconditionally stable from near-DC to 10GHz. The amplifier layout is inserted into a 60 mil by 60 mil Anachip for ease of fabrication.

Introduction

This LNA is designed the TriQuint TQPED process with vias. The LNA is part of the MMIC design class' duplex transceiver utilizing a receive array for the C-band HiperLAN wireless local area network (WLAN). It is one of nine unique MMIC designs which make up the C-band transceiver. Each design was to be contained on a 60 mil square die.

Circuit Description

The LNA circuit design selected was a single-stage amplifier using a 35um x 4 (140um) depletion mode FET. A drain-gate resistor-capacitor feedback network was used to stabilize the amplifier and flatten the gain but restrict DC current flow from gate to drain. Dual sources are used to bias the amplifier. The DC sources are isolated from the RF network using on-chip inductors and filtering is provided by on-chip bypass capacitors.

Design Philosophy and Design Tradeoffs

A single depletion mode FET was chosen because of the desire for an ultra-low-power amplifier with low noise figure. The goal was lower than 10mW of total DC power consumed with a secondary goal of 5mW. Better than 2.5dB noise figure was desired. The first cut design aimed for 5mW of total DC power while achieving 10dB of gain and an unconditionally stable circuit from DC to 10GHz.

The decision was made early on to not adopt a single-supply self-biased amplifier. The main reason for this is we suspected the design would be very sensitive to bias and process shifts and wanted the ability to tune in-lab to achieve best performance. Further iterations of this design could implement a self-bias scheme with a single supply to simplify integration.

The amplifier was designed to have a low noise figure and low DC power consumption. This dictates a very small device, which inherently will have low, narrow-band gain and be difficult to match (high VSWR). We mitigated this later in the design by bumping DC power slightly (by up-sizing the FET slightly) to improve VSWR. Initial designs showed high gain but very poor VSWR when using a drain-only resistive stabilization. A small series inductor on the FET source combined with an RC feedback stabilization network flattened gain (at the expense of peak gain) and achieved an unconditionally stable design.

The LNA is matched for optimum noise figure on the input side using an LC network. The output is matched for VSWR at 50 ohms using an LC network. Both networks are entirely on-chip and neither includes any DC paths to ground, maintaining a low-power operation.

Because this design was somewhat new, no hard specifications were provided so reasonable goals were set by the design team.

Table 1 – Specification Matrix

Spec	Specification Goal	Layout Schematic
Frequency Bandwidth	5150-5875	5150-5875
Gain	> 8dB	8.5dB minimum
Gain Ripple	+/- .5dB max	1.2dB
VSWR, 50 ohm	<1.5:1	<1.5:1, output < 1.78:1, input
Supply Voltage	None specified	Dual supplies
Noise Figure	< 2.5dB	< 2.32 dB
DC Power	<10 mW	6.34mW

Predicted RF Performance

The following plots show the predicted performance of the amplifier as layed-out including interconnect, bond pads and bond wires to connect to external supplies. Performance is expected to be slightly better if the RF pads are probed using G-S-G probes and efforts are made to keep inductance to a minimum.

Figure 1 – Noise Figure

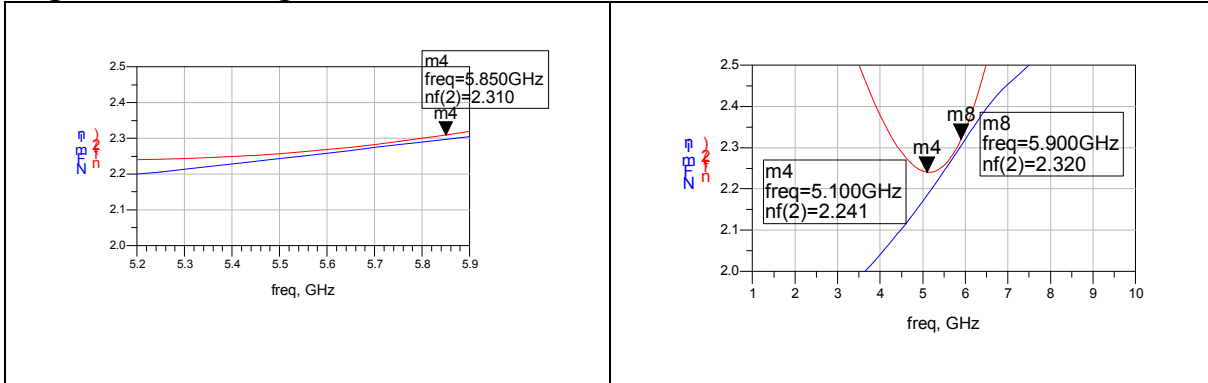


Figure 2a – S-parameters

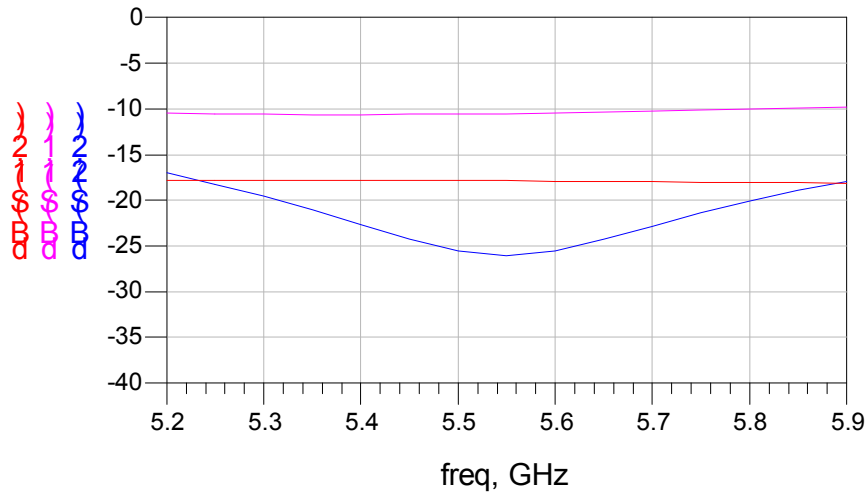


Figure 2b – S-parameters expanded

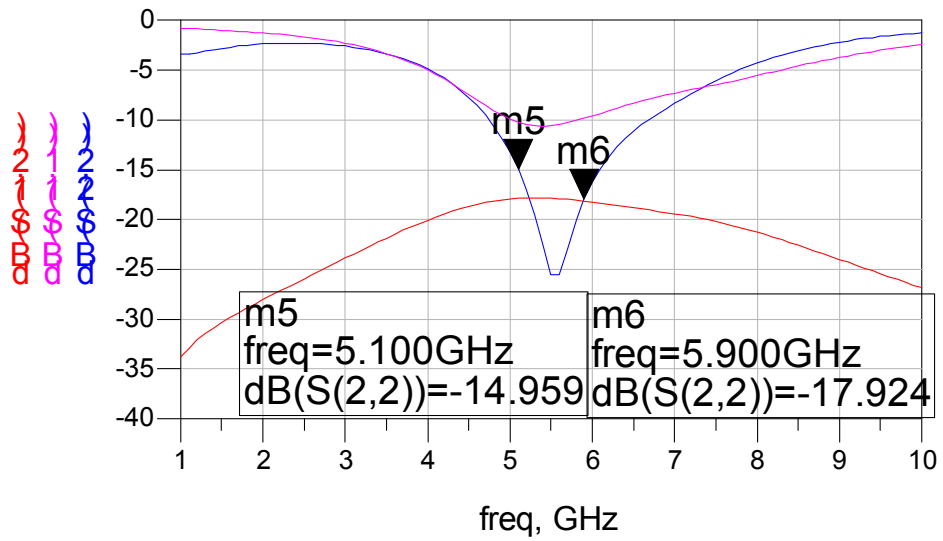


Figure 3a – In-band Gain

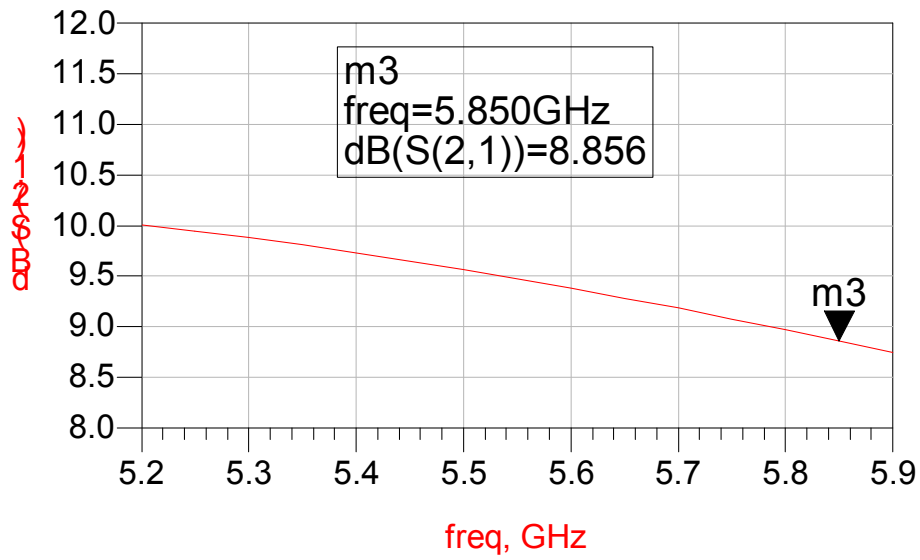


Figure 3b – Gain expanded

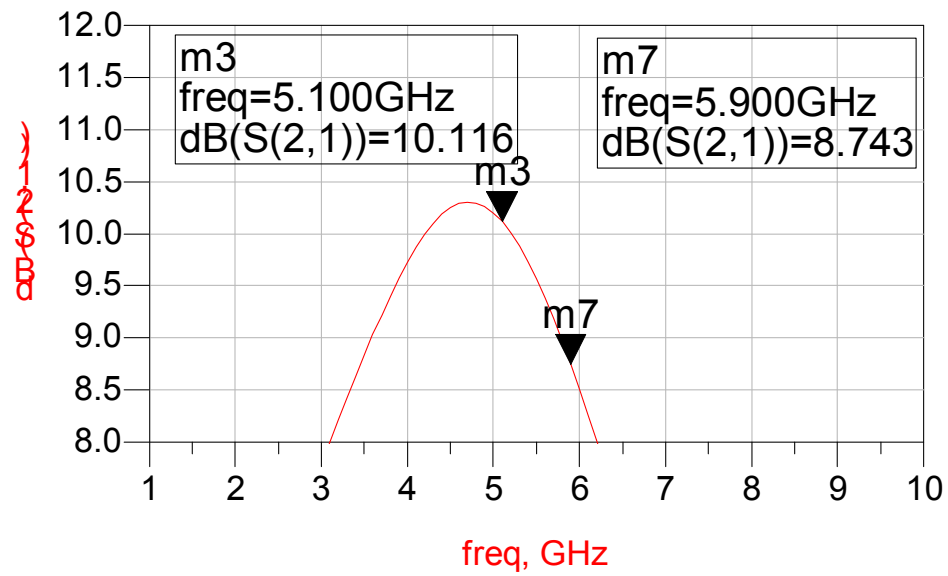


Figure 4a – In-band Stability

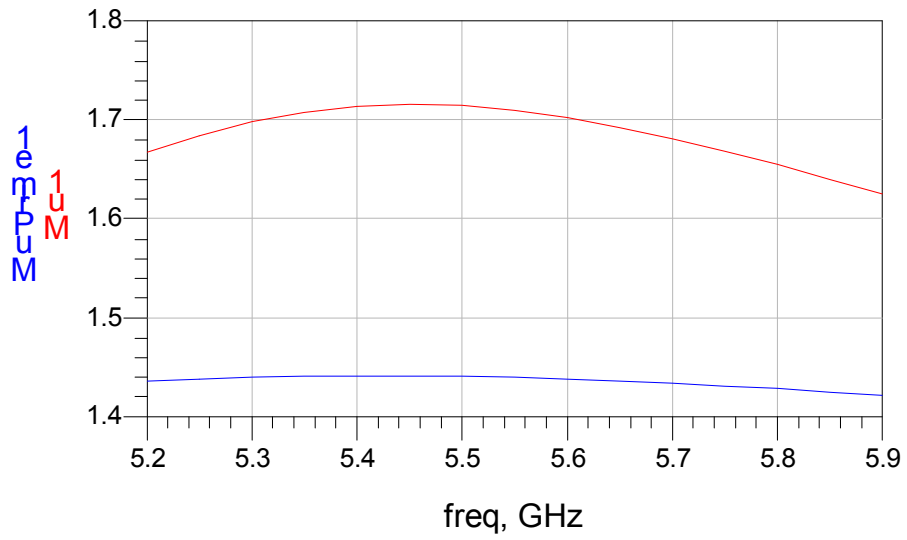
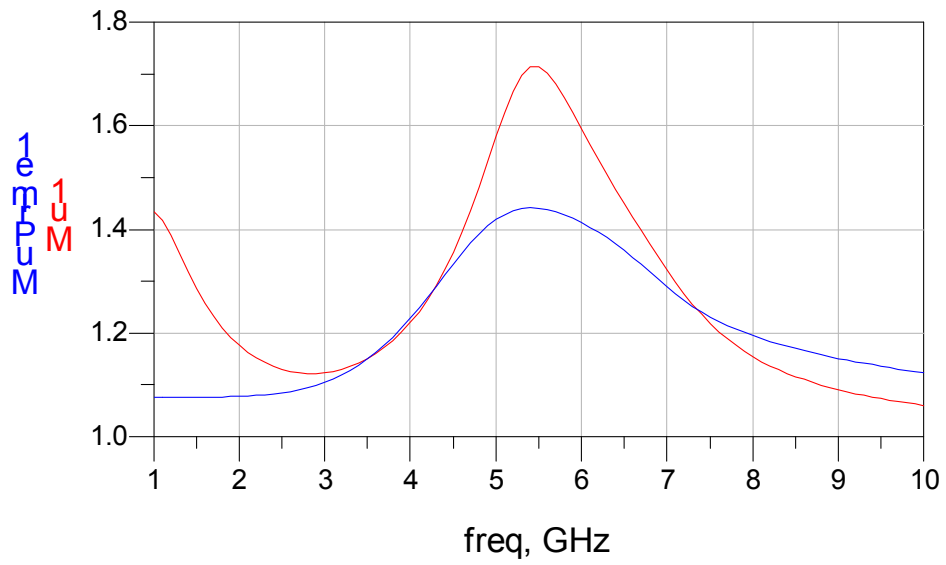
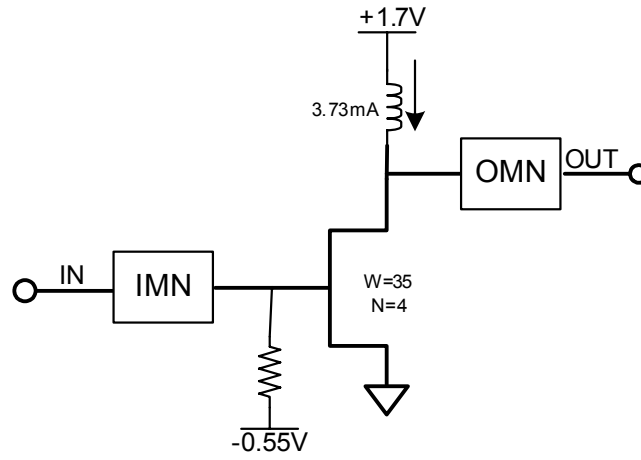


Figure 4b – Stability expanded



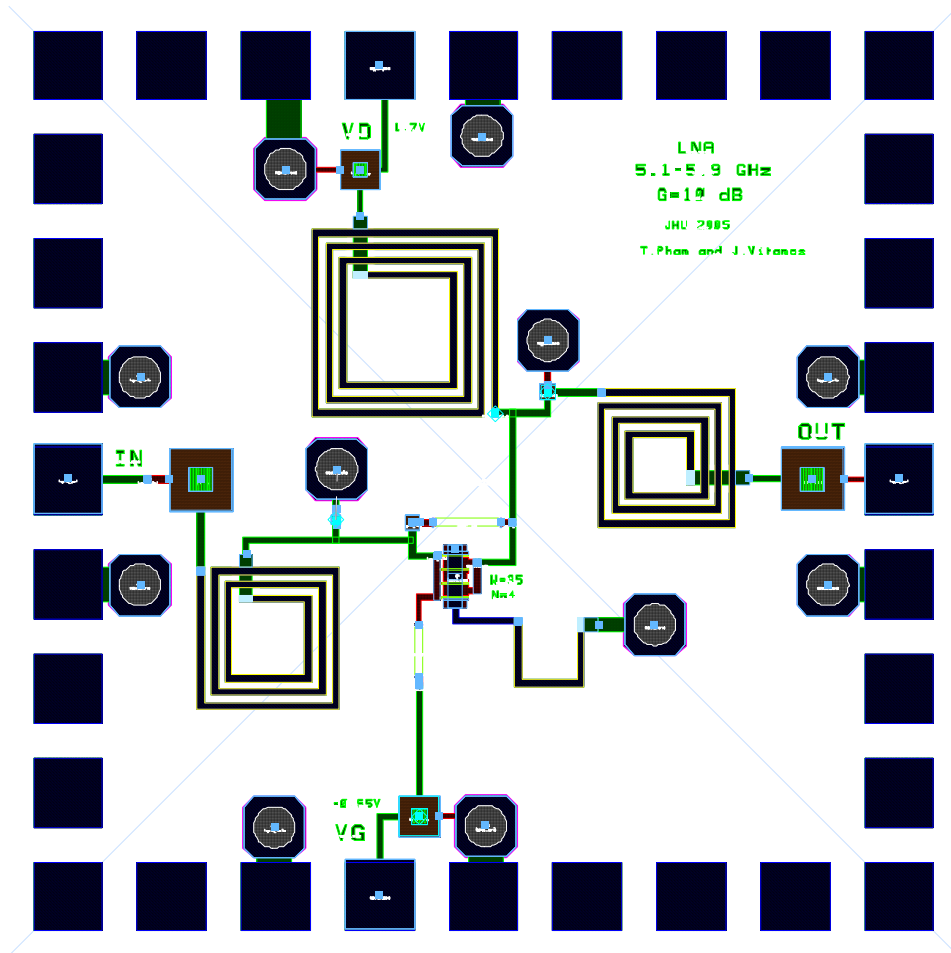
Schematic Diagrams

The following pages illustrate the simplified design schematics used for this LNA. They do not include interconnect for simplicity's sake.



Final Layout

Final layout of the LNA was fixed perfect into Anachip and using TriQuint components.



Test Plan

- Ground procedure: The signal ground, test equipment and DC ground shall be electrically connected in the test station.
- Voltage Requirement: All test voltages shall be measured with respect to signal ground unless otherwise specified.
- Test equipment: The following test equipment will be needed to fully characterize the LNA design.
 - Agilent Network Analyzer (or comparable 2-port VNA)
 - Signal Generators
 - Digital DC Power Supply (two)
 - Spectrum Analyzer
 - Agilent Power Meter
- Turn On Procedure:
 - Set Gate power supply to -2VDC.
 - Set Drain power supply to 1.7VDC.
 - While measuring drain current, bring gate voltage more positive.
 - Desired drive current is 3.83mA which should correspond to a gate voltage of approximately -0.55VDC.
 - Apply RF power to the device
- SS measurement:
 - Perform a full calibration on the network analyzer from 1 to 10GHz
 - Apply the DC power supply and record the DC current of device.
 - Measure S11, S22 and S21 of the LNA and store the data. Set frequency from 1GHz to 10GHz Step of 0.4GHz; input power -10dBm
 - Turn off power supply when finished
- Noise Figure Measurement:
 - Perform a calibration on the noise figure meter at 5.5 GHz.
 - Connect the input probe to the RF IN pad.
 - Connect the output probe to the RF OUT pad.
 - Apply bias and
 - Perform the Turn On Procedure.
 - Measure the noise figure of the LNA and store the measurement data.
 - Turn off power supply.

Compare the result with simulation data and record it.

Summary and conclusion

We have completed the design, simulation and layout of a C-Band low-power LNA. Power consumption is 6.34mW. Expected noise figure is less than 2.32dB across the band of operation. Output VSWR is better than 1.5:1. Gain is better than 8.5dB across the band. The design has passed layout versus schematic (LVS) checks and passes a design rule check (DRC). Our primary compromise was trading VSWR and small-signal gain for low power operation while still maintaining a low noise figure.