

C-BAND POWER AMPLIFIER

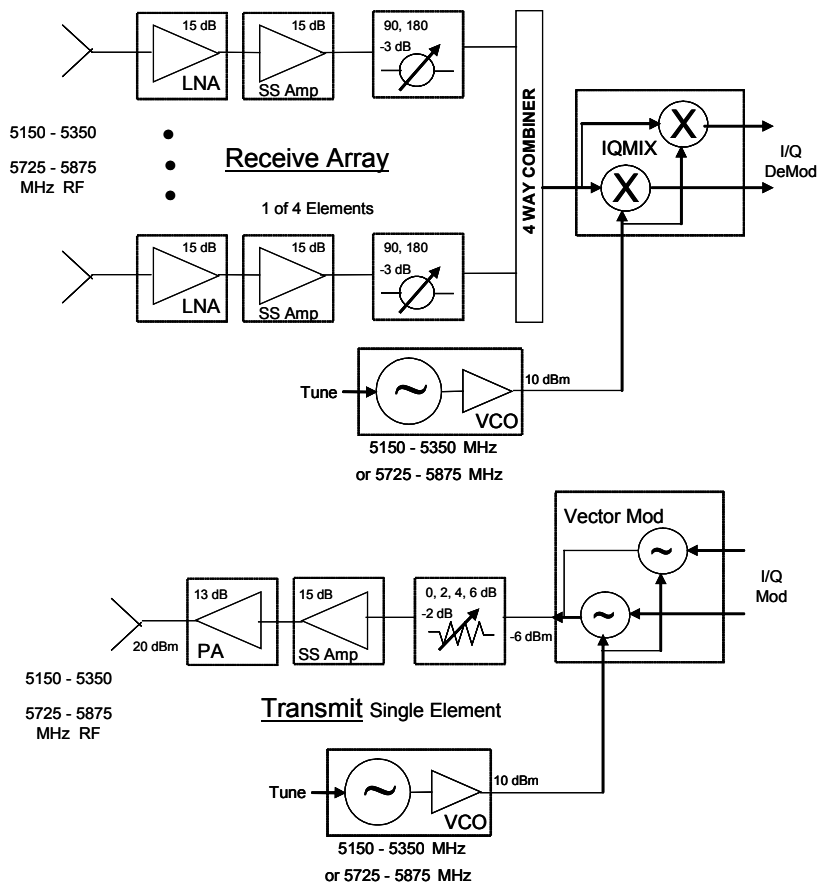
525.787 Microwave Monolithic Integrated Circuits (MMIC) Design

Abstract

The design of class AB MMIC Power Amplifier is described in this paper. This design is a part of a duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies. The designed was implemented using TriQuint TQPED 0.5-um pHEMT process. Good performance in the frequency band of 5.15 to 5.875 GHz, center frequency 5.5125 GHz, was achieved. The PA results achieved are as follows: small- signal gain of 12.4 dB across the band; output power $> +20$ dBm and PAE of $>30\%$ at the 1dB compression point; VSWR of $<1.5:1$ input and $>1.5:1$ output was achieved.

Introduction

The Power Amplifier designed in this project is part of duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies shown in Figure below. The PA is in the transmit chain and therefore requires to be highly efficient and linear as well. Class AB bias was chosen because it gives a good tradeoff between the 2 requirements: efficiency and linearity. The most important specification to meet is the output power level and power added efficiency.



Chip Set for the 5150 - 5350 MHz WLAN and
5725 - 5875 MHz ISM Bands

Fig.1: C-Band duplex transceiver

Design Approach

Based on the specification given for this design as shown in table 1 below, the device size, topology, and bias was chosen. The chip size to be used was 60 X 60 Mil, which posed a challenge on layout of 2 stage amplifier. The first design approach was to design a single stage PA biased at class AB using Cripps design method [1]. The drain voltage was chosen based on the power supply limitation to 5 Volts. A previous PA design done in class using TriQuint 6X50 0.5 μm Dmode PHEMT showed good results and therefore the same device size employed in this design.

	SPECS	Pre-Layout	Post-Layout
Frequency	5150 – 5875 MHz	Yes	Yes
Bandwidth	> 800 MHz	Yes	Yes
Gain (Small Signal)	>13 dB; goal 15 dB	13.36dB	12.4dB
Gain Ripple	± 0.5 dB max.	Yes	Yes
Output Power@ 1 dB compression point	>+20 dBm	21.003 dBm	20.226 dBm
Power Added Efficiency	>20 %; 25% goal	36.4 %	31.44 %
VSWR (50 Ω)	<1.5:1 input & output	1.309:1 input; 2.45:1 output	1.249:1 input; 2.379:1 output
Power Supply	+ 5 and – 5 V	Yes	Yes
Chip size	60 X 60 mil ANACHIP	Yes	Yes

Table 1: Design specifications and goals for the PA

The figure below shows the I-V Characteristics of the TOM3 model and a marker indicating the biasing for this device. The Gate Voltage, V_{gs} , is equal to -0.1 V at 56 mA and V_{ds} of 5 V.

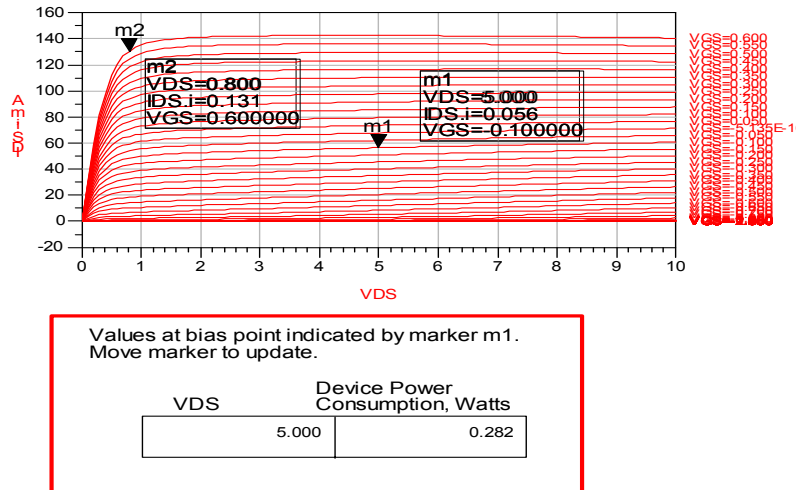


Fig.2: I-V Characteristics of the pHEMT model

The design of the PA was first done using ideal lumped elements. Those ideal elements were replaced using the corresponding models from the TQPED design kit. Resistors and capacitors were easy to synthesize, but inductors had to be carefully modeled using an iterative tuning process. Final layout was done using microstrip connections. The final design was then simulated to give the results shown in table 1.

Trade-off

The trade-off for this design was directly associated with the design specifications that were the most important. In the case of PA design these specifications are output power and power added efficiency (PAE). Since PA consume most of DC power in a RF chain, hence require the PAE to be high. The higher this value is the better DC power consumption design is. The specification was >20 % and 25% goal. The final design was able to achieve 31.4 %. The output power goal of >20 dBm (20.2 dBm) was achieved. The small signal gain of 13 dB across the band was compromised to a final of 12.4 dB. The gain would have been achieved by either increasing device size or using a second stage but since output power and PAE goals were met the extra mile was not taken due to complexity of network for the 2 stage layout. The input VSWR was met because the input match is conjugately done to give the best match at the input, while the output VSWR was not met due to the nature of output match, which is done for the best power as supposed to the best match.

Schematics

The figure below shows the final PA design using Triquint elements without the microstrip interconnections. The DC bias is also displayed. The intended bias of 56 mA I_{ds} and V_{ds} of 5 V was slightly changed by the use of real elements to 67 mA and 4.72 V respectively, which can be lived with. The design includes input matching network, L22, stabilizing resistor, R3, output matching network, L21 and C16, blocking capacitors, C11 and C13, DC feeds, L20 and R4, at the drain and gate respectively. The ideal inductors L10 and L19 represents bond wires to the DC power supplies. The capacitors C15 and C12 provide RF ground to avoid the RF interference with the DC supply.

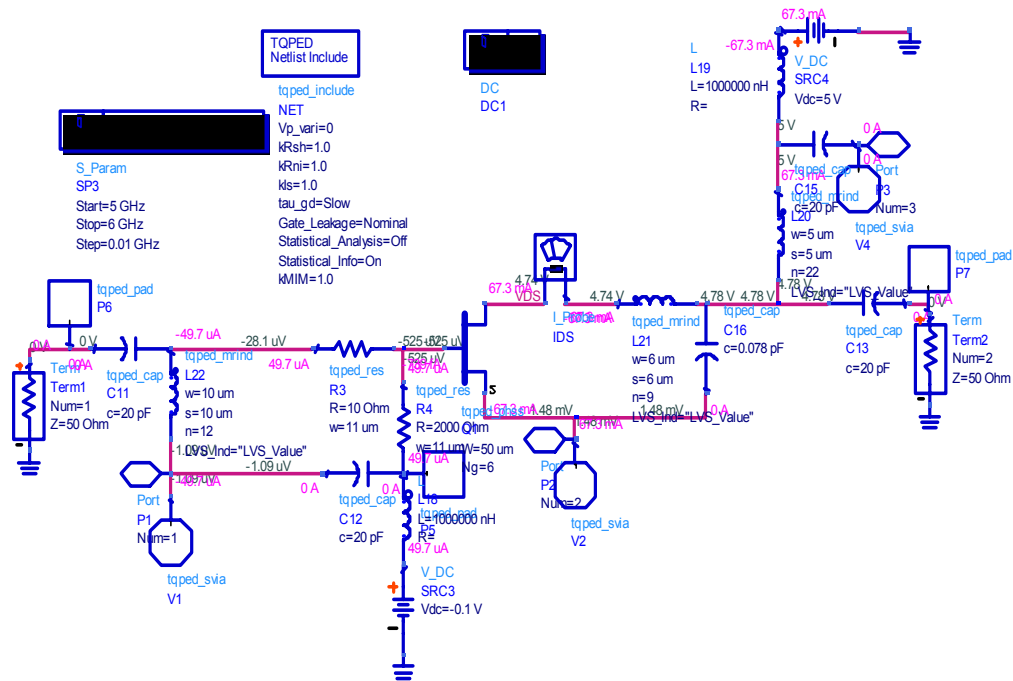


Fig.3: Schematic showing bias of the device.

Output Matching Network (OMN) using Cripps Method

Output matching network is the first network to be done in the PA design. The Cripps method [1] is employed. R_{cripps} was determined from the DC load line (load line dictated by markers m1 and m2 in the Figure 2 plot). R_{cripps} was calculated to be 67.8 Ω . An RC network was then tuned to model S22 from which Cds could be determined. The final load used according to Cripps is $R_{cripps} || C_{ds}$. Figure below shows the model for S22 of device (Term1 network) and Cripps load (Term2 network).

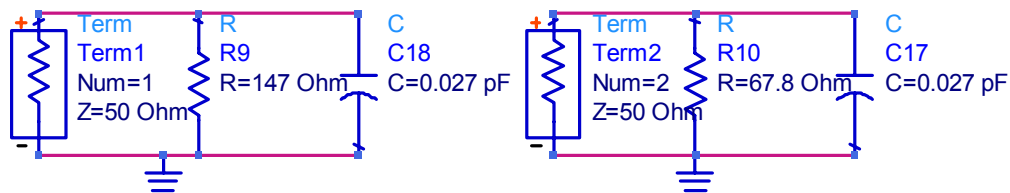


Fig. 4: RC network for Power match

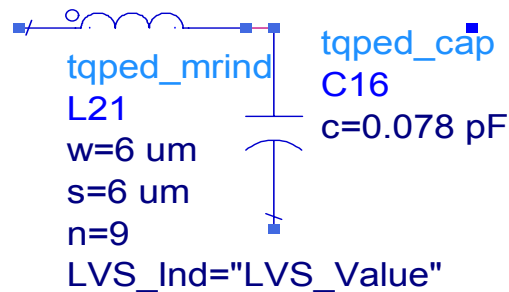


Fig. 5: Final Triquint Element OMN

Input Matching Network (IMN)

The input matching network was a conjugate match to avoid the loss of any more gain within the design. The network determined was made up of 2 elements as shown below, but it produced a very narrow band. A compromise of one element (L22 in figure 3 above) was done and the value was optimized to give a broader frequency response.

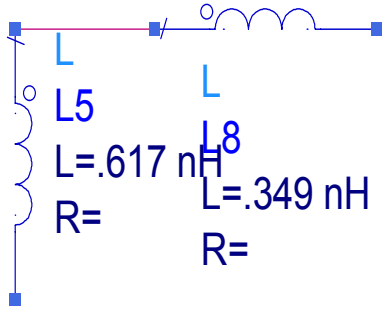


Fig. 6: original Ideal IMN

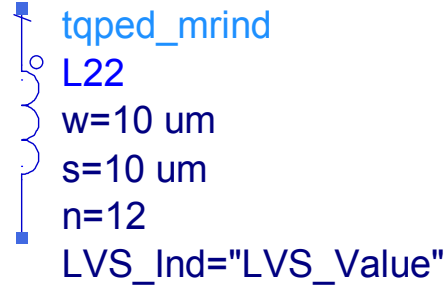


Fig. 7: Final Triquint Element IMN

Final PA design

Once all the networks are put together, the final design requires the microstrip interconnections for a fair comparison between the schematic and layout. The figure below shows the final schematic with interconnects and matching networks tuned to compensate for the microstrip interconnects losses. The schematic also includes the Ground-Signal-Ground (G-S-G) pads and DC supply pads.

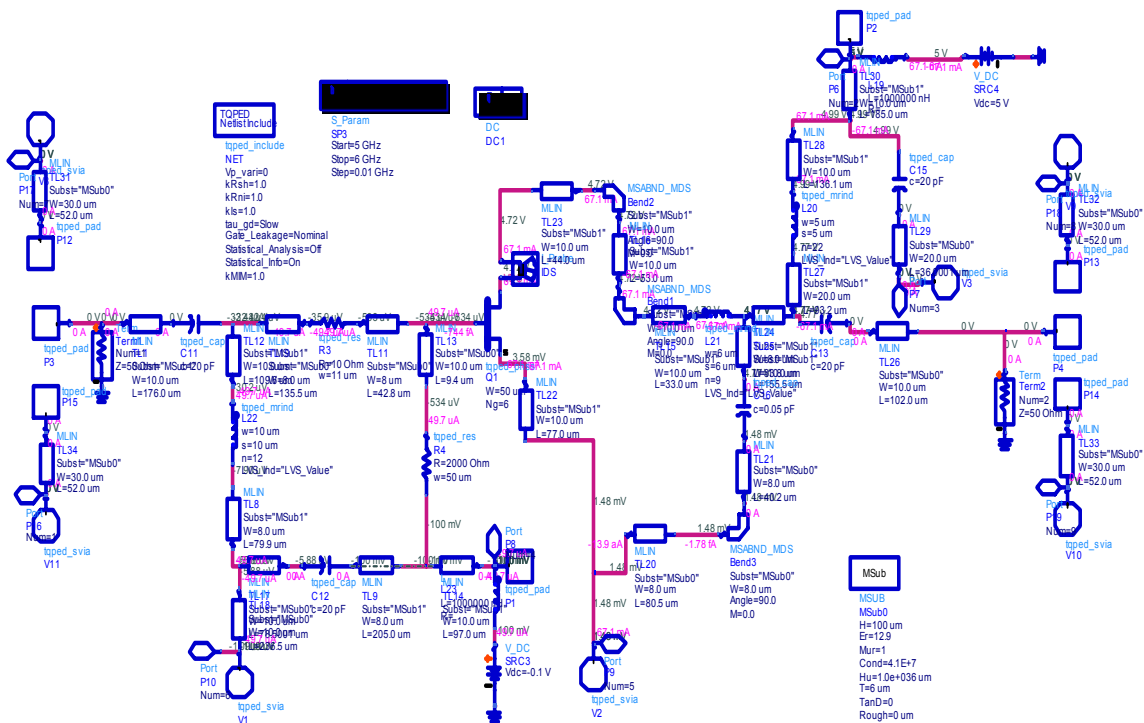


Fig. 8: Final Schematic with Microstrip interconnections

Simulations

Linear simulations were done across 0.5 – 10 GHz. The stability plot below shows stability across the whole band. The Linear simulation results were done both before and after microstrip interconnections. The displayed linear results include S21, S11, S22 and VSWR (with a closer look at the frequency band of interest).

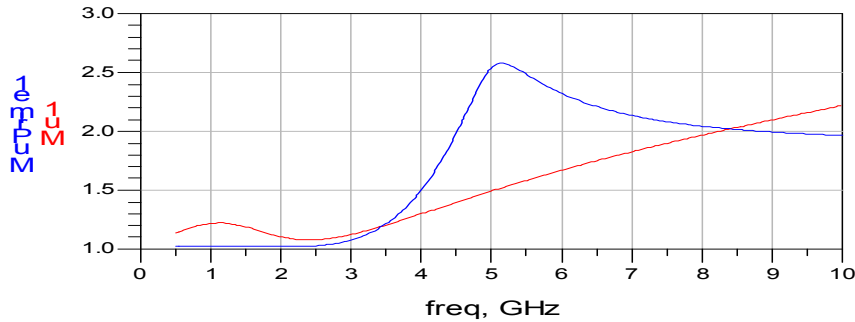


Fig.9: Stability factor plot

Pre-Layout results (Before microstrip interconnections)

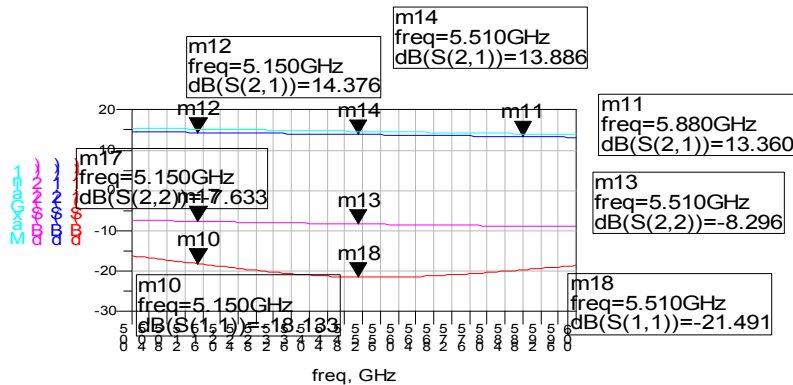


Fig.10: S-parameter simulations

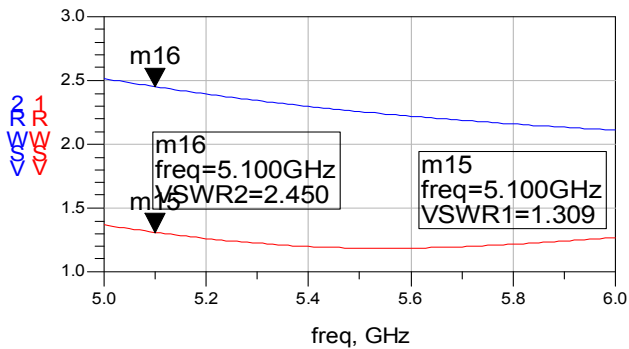


Fig.11: VSWR (blue=output; Red=input)

Post-Layout results (after microstrip interconnections)

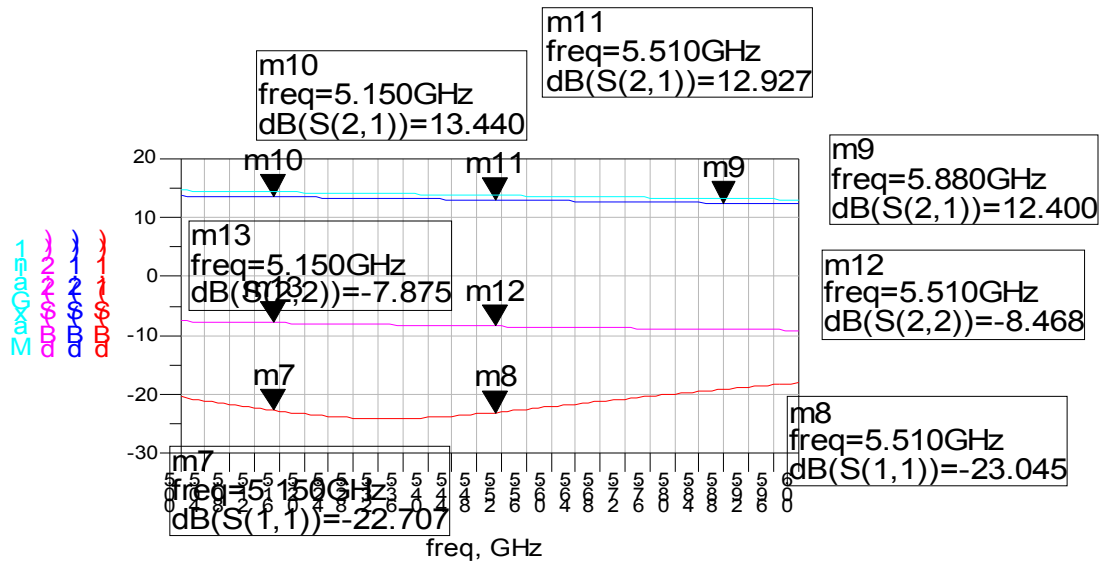


Fig.12: S-parameter simulations

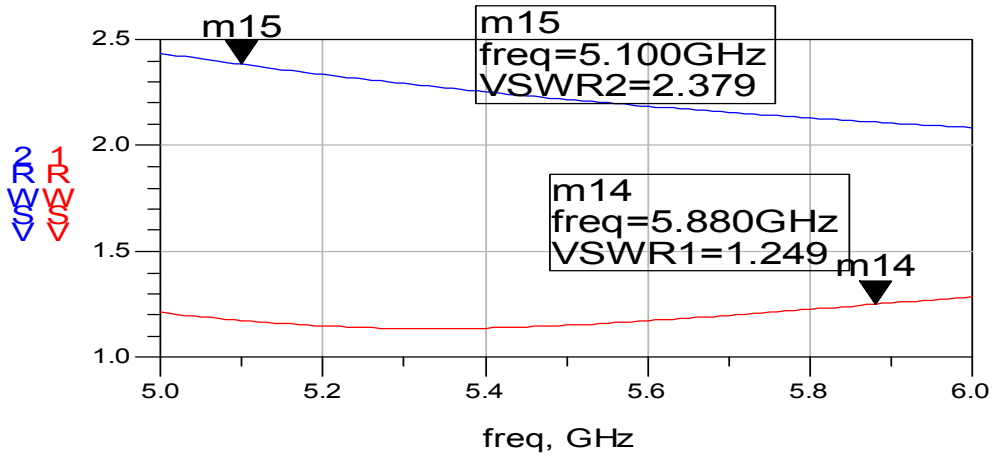


Fig.13: VSWR (blue=output; Red=input)

It can be noted that before the microstrip interconnections, figure 10, that the gain requirement had been met, but slightly changed with the interconnections added, figure 12. The VSWR improved with interconnections.

Non-Linear Simulations

Harmonic balance simulation was done to display non linear results, Output power and Power Added Efficiency. The results are also displayed for pre- and post- layout. These plots also include a gain plot, and a linear plot for determining 1 dB compression point given as 8.2 dBm input power. The left y-axis scale is for Output power, gain and linear plot, while the right y-axis shows the Power Added Efficiency scale.

Pre-Layout results (Before microstrip interconnections)

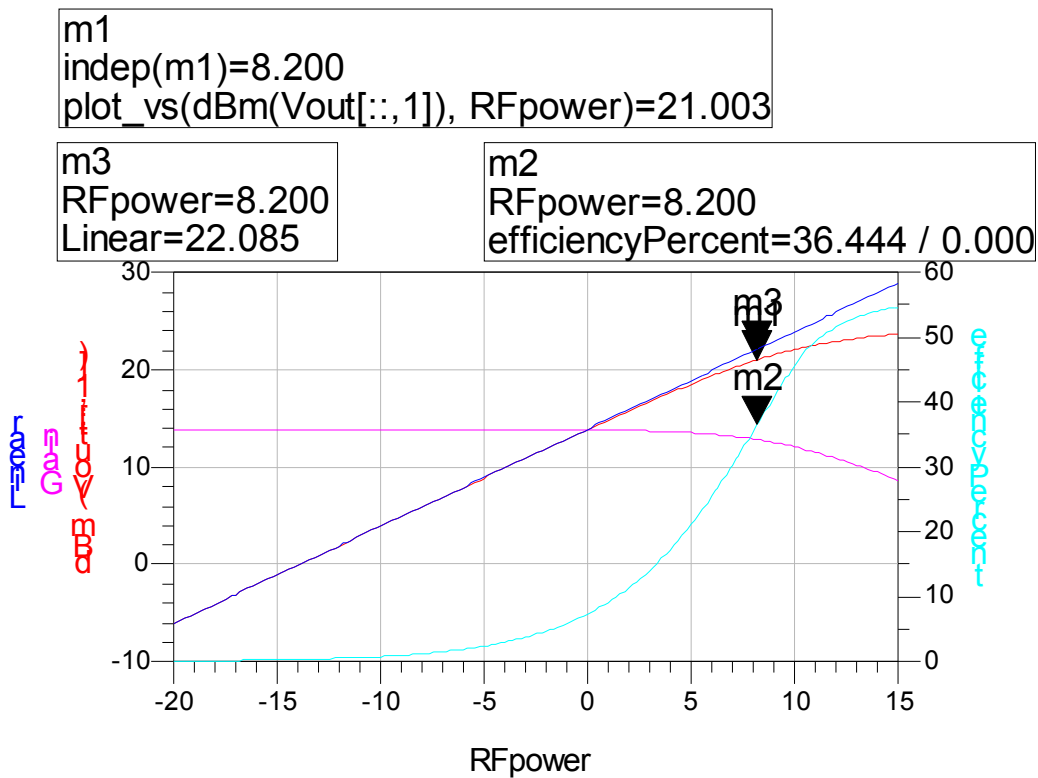


Fig.14: non-linear simulations

Post-Layout results (Before microstrip interconnections)

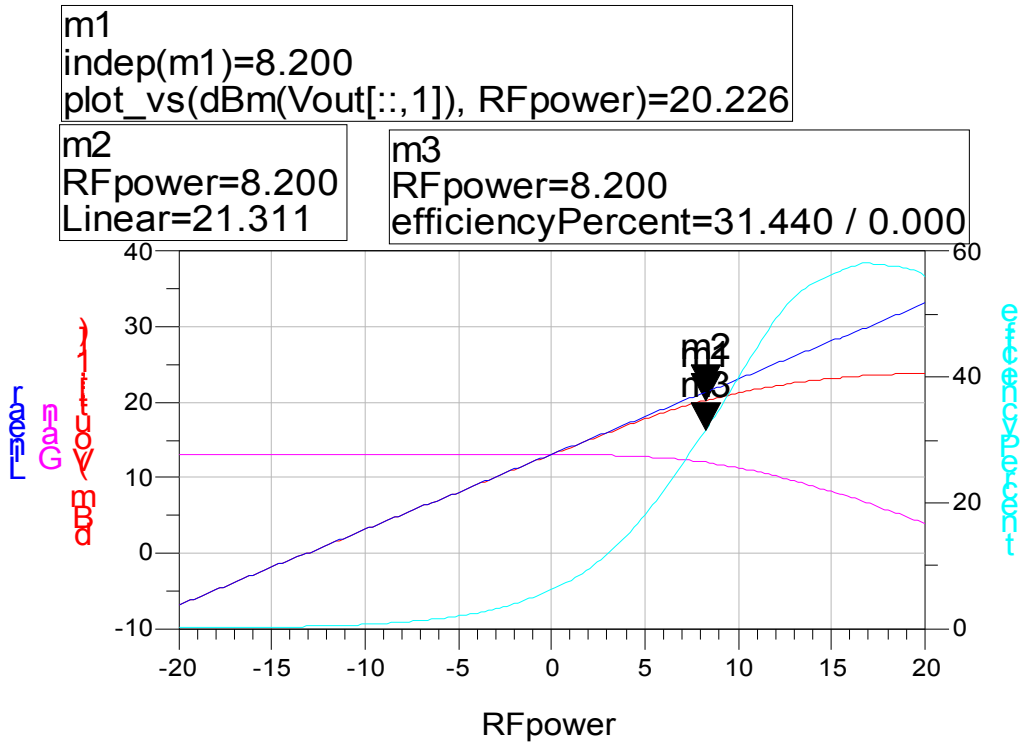


Fig.15: non-linear simulations

Finally dynamic load line is displayed in the figure below.

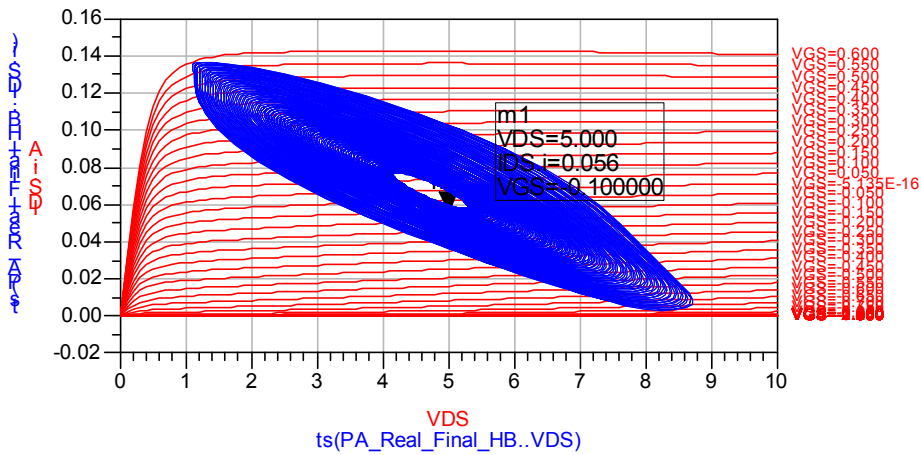
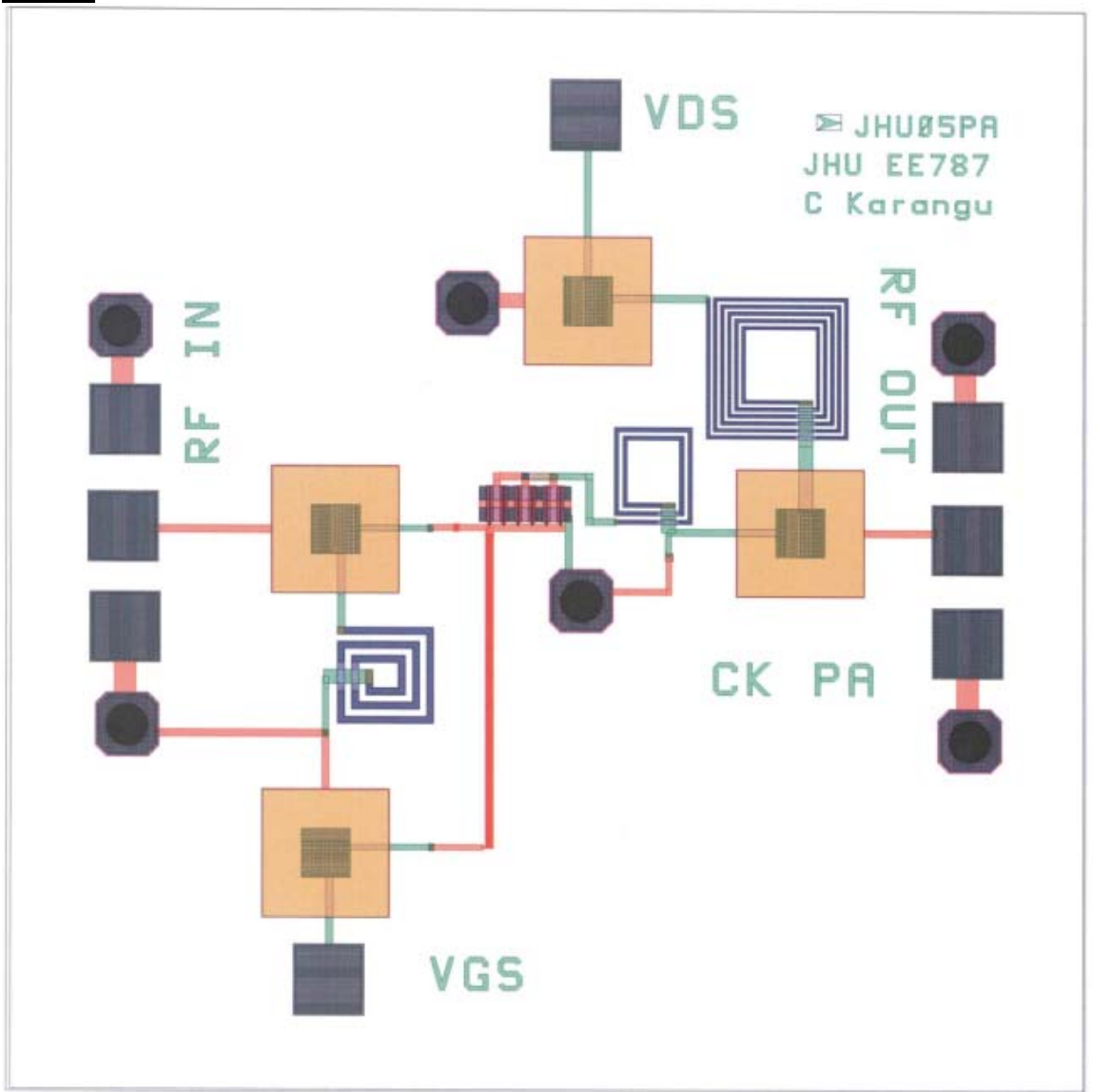


Fig.16: Dynamic Load Line

Layout



Test plan

Ground-Signal-Ground (G-S-G) pads are required in order to perform RF measurements using the HP 8510 Vector Network Analyzer and Cascade probe station. These pads are shown in the Final Layout figure above and are labeled RFIN and RFOUT for the RF input and output respectively. RF probes will come in from the left and right of the chip for input and output, respectively as shown in the layout.

For the DC bias, pads are put on top and bottom of the chip for VDS and VGS bias respectively. 5 and -0.1 volts supplies will be connected to the VDS and VGS pads respectively.

The VNA 8510 will be used to measure all linear measurements while the spectrum analyzer will be used to perform non linear measurements.

Below is a list of all equipment to be used.

Test Equipment:

- Agilent 8510 VNA (45 MHz to 26 GHz)
- Cascade Model 43 wafer probe station with up to 4 RF probes & 4 DC needle probes
- Synthesized signal generators to 26 GHz
- Spectrum analyzer to 18 GHz

Conclusion

The design of PA for the C-Band Transceiver was successfully done. All the goals were not met but the most important ones were met, namely Power Added Efficiency and Output power of, 31.4 % and 20.226 dBm respectively. The input VSWR of 1.2 was achieved meeting the requirement of <1.5 . The specifications that were not met were not far off, hence the settling of the final design. One of these specifications was the small signal gain. It was supposed to be 13 dB across the band but the design yielded 12.4 dB gain across the band. A difference of 0.6 dB was not that critical to make the decision to do a 2 stage design. Output VSWR achieved was 2.37 but this was expected to be off due to the nature of the output matching design. The design and layout were both done using ADS circuit simulator. This exercise was very informative and enabled tremendous growth towards becoming RF MMIC designer.

References

1. Steven C. Cripps, "RF Power Amplifiers for Wireless Communications," Artech House, 1999, chapters 3, 5, 8.
2. Penn, John and Reece, Michel. *Class Handouts*. JHU/APL. 2005.