

Phase Shifter Final Report

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Abstract

A MMIC 2-bit phase shifter for the 5.8 GHz ISM band was designed using the Triquint Semiconductor TQPED process. Simulation and layout were performed with Agilent ADS. The phase shifter is one component of a duplex transceiver being built as a class exercise at Johns Hopkins University.

Introduction

A phase shifter is a two-port microwave device whose phase response changes according to an external input. The phase shifter designed here accepts logical inputs to select from four phase states. This will be used in the signal path of each element of an antenna array. By changing the phase of the signals, the antenna array beam can be steered without physically moving the antenna.

The specifications for this phase shifter are as follows:

Frequency:	5150 to 5875 MHz
Bandwidth:	> 800 MHz
Insertion Loss:	< 4 dB (3dB Goal)
Insertion Loss Balance:	+/- 1 dB
Phase Shift:	Steps of 45 (Goal), 90, 180 Degrees
VSWR to 50 Ohms:	<1.5:1 on Input and Output
Supply Voltage:	+/- 5 Volts
Control:	TTL (Goal) or 0/-5 Volt
Size:	60 by 60 mil

Design Approach

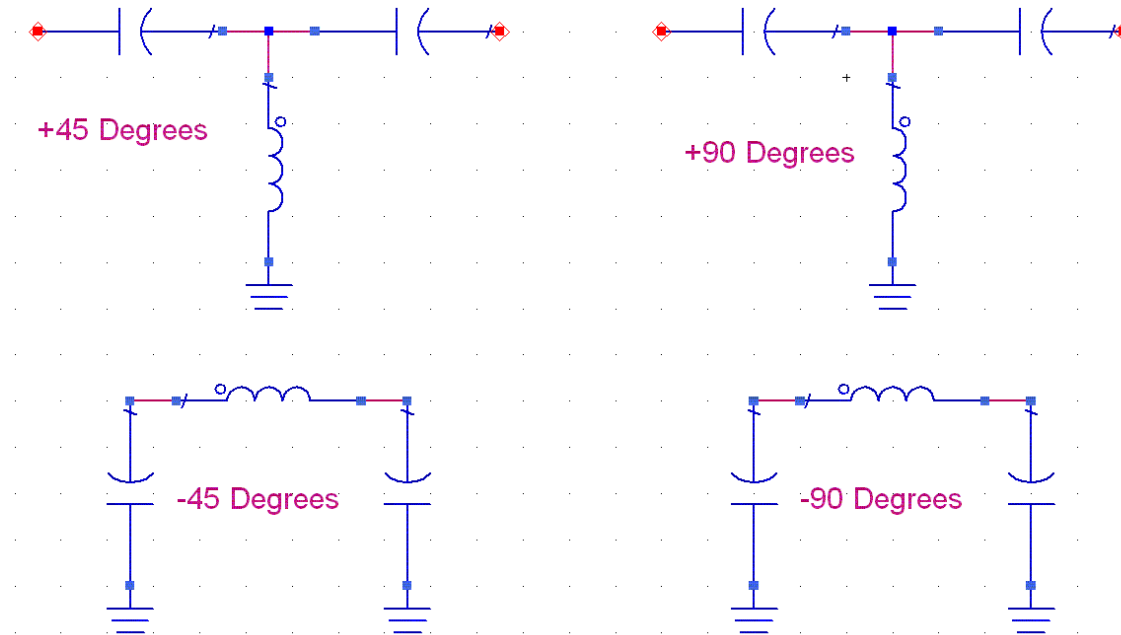
A straightforward topology was chosen to implement the phase shifter. The topology is a parallel combination of two phase filters in series with a second parallel combination of two phase filters. One filter from each parallel combination is selected with FET switches.

The first parallel combination is of filters with +45 degree and -45 degree phase shifts. The second parallel combination is of filters with +90 degree and -90 degree phase shifts. By selecting either +45 or -45 degrees and +90 or -90 degrees, the following relative phase shifts can be realized:

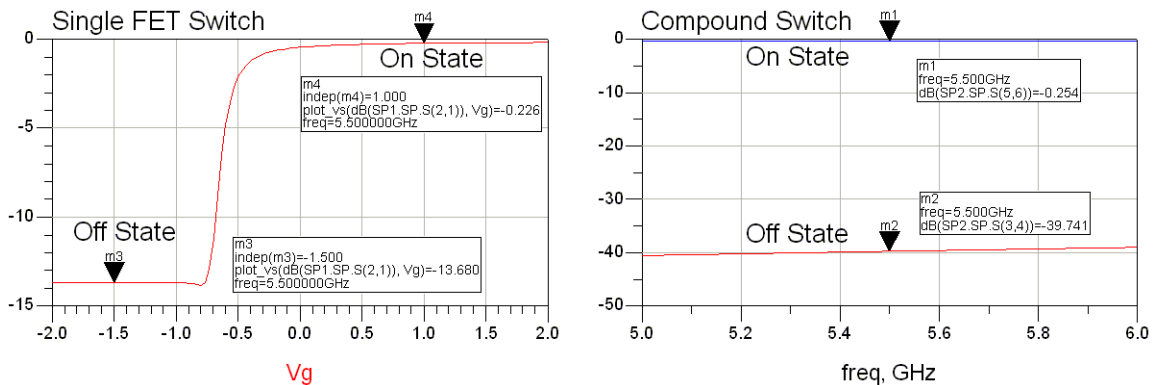
First Filter	Second Filter	Absolute Shift	Relative Shift (Subtract 45)
+45	+90	+135	+90
-45	+90	+45	0
+45	-90	-45	-90
-45	-90	-135	180

Once the general topology is chosen, the four individual filters and the switches had to be designed. For the filters, lumped elements were used to generate the required phase shift. The +90 and -90 degree filters implemented as lumped element quarter wavelength transformers. Copies of these were tuned to generate the +45 and -45 degree filters. The topology of each filter was

chosen to minimize die space usage. As can be seen in the figure below, the appropriate TEE or PI, high-pass or low-pass, topology was chosen to require only one inductor per filter.



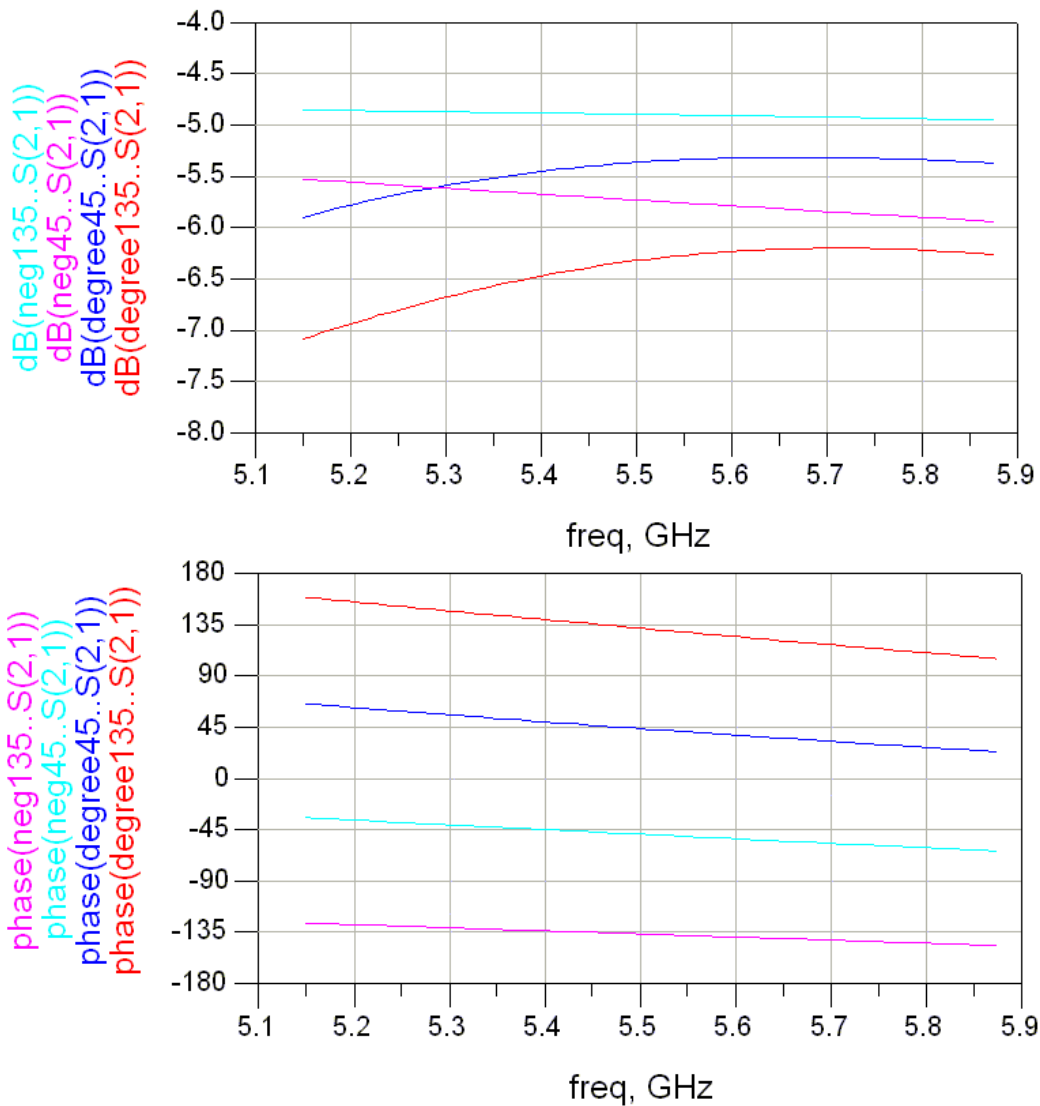
For the switches, an initial simulation of a single series FET and of a series-shunt combination was performed. Both configurations had similar insertion loss of 0.25dB. The off state of the single series FET provided 13dB of isolation while the series-shunt combination provided 40dB. For this application, the single series FET switch was chosen. It is smaller, easier to route the control voltages, and for this design the effects of the lower isolation can be absorbed into the filters. The following figure shows the on and off state performance of each configuration.

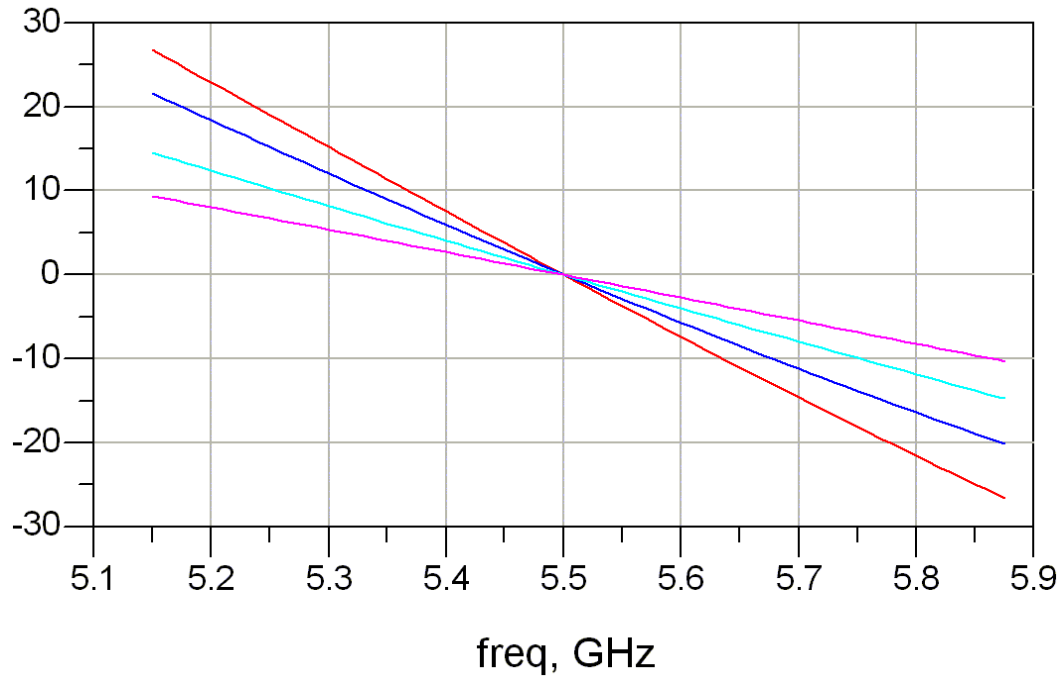


Simulations

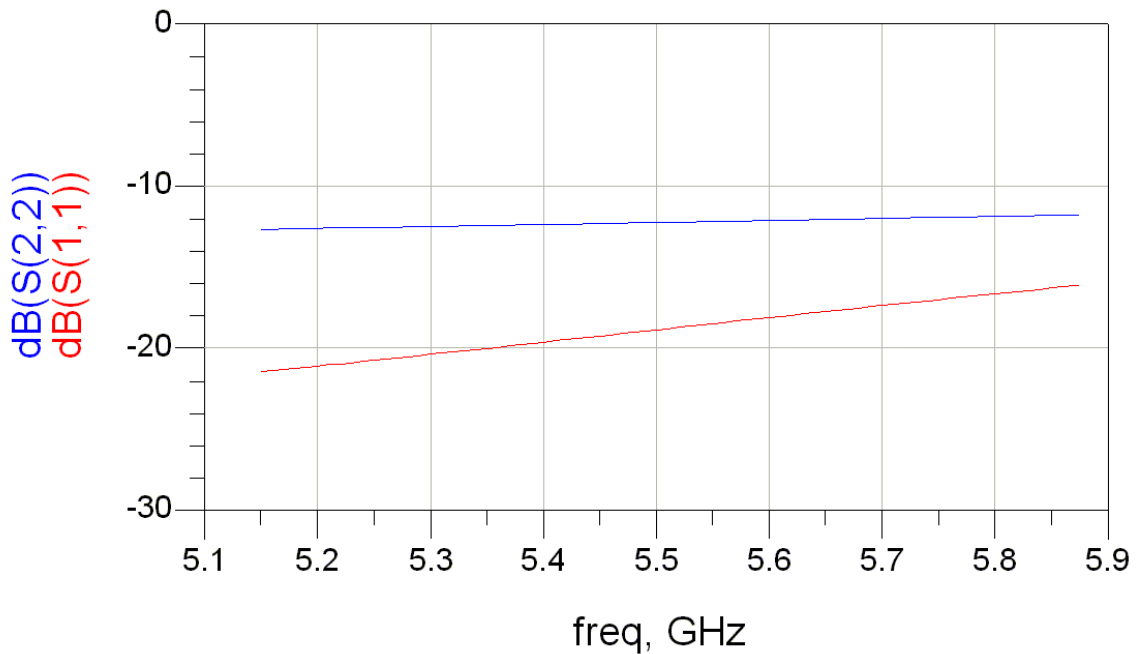
The following simulations are of the entire circuit including interconnecting lines generated in the layout. As seen in the first plot below, neither the insertion loss nor the insertion loss balance specifications were met. The mid-band insertion loss varies from -4.8 to -6.4 dB.

The phase of the four states are shown in the second figure below. The mid-band values show the expected absolute phase shift of -135 , -45 , $+45$, $+135$ degrees, as expected. However, the states with larger phase shift diverge from the desired value more quickly than the lower phase shifts. This is illustrated in the third figure below. In this figure the phases are normalized to zero at the center frequency. The divergence from the intended phase shift versus frequency is clearly more for the larger phase shift states. The result of this is undesired relative phase shifts at the band edges. A correction for this was not attempted in this design.



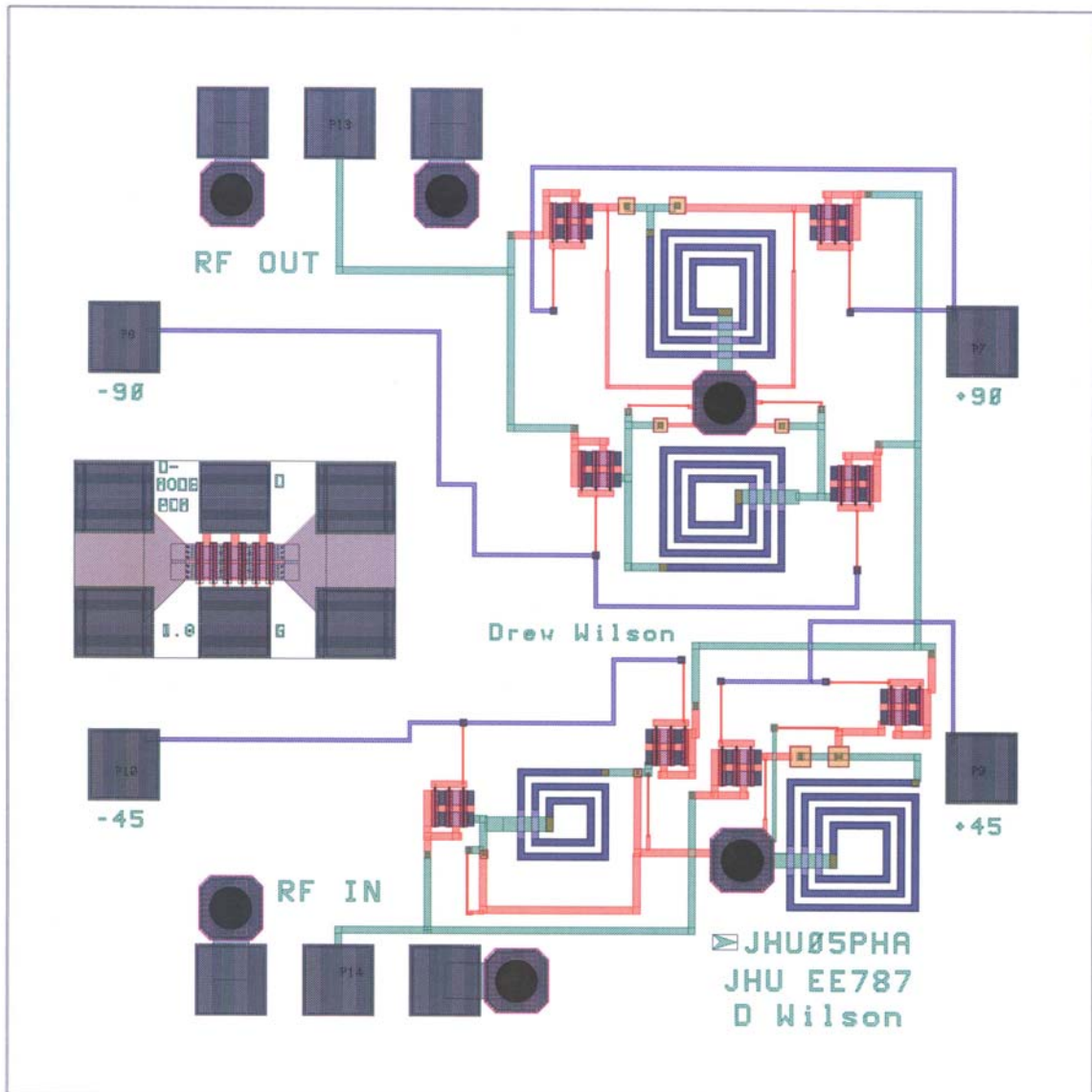


The input and output impedance match specification is VSWR of 1.5:1 on input and output. This corresponds to a return loss of -14dB . A plot of input and output port return loss is below. The impedance match specification was met on the input, but not the output. During the design only the input impedance match was monitored.



Layout Plot

A plot of the layout follows. In this plot, the two RF ports are labeled RF IN and RF OUT. Each of these has ground-signal-ground pads on opposite sides of the die for testing on a wafer probe station. There are four DC connections to be made to the die. These are toward to four corners of the chip and spaced away from the RF connections. This is to simplify needle probe connections. These four ports are labeled -90, -45, +90, +45.



Test Plan

Connections

The die requires two RF connections. These are labeled RF IN and RF OUT on the die and in the layout plot above. Both ports are 50 Ohm.

Four DC connections are required for testing. DC levels are 0 and -5 Volts. Simulations show current draw for the entire die to be 1.6pA. The DC ports are 0/-5 Volt complementary pairs. One pair is labeled +45 and -45. The other pair is labeled +90 and -90. Select phase states by reading across the table below.

“-90”	“+90”	“-45”	“+45”	Absolute Phase
0 V	-5 V	0 V	-5 V	-135 Degrees
-5 V	0 V	0 V	-5 V	+45 Degrees
0 V	-5 V	-5 V	0 V	-45 Degrees
-5 V	0 V	-5 V	0 V	+135 Degrees

Tests

S11 and S22 can be measure with any phase state. Phase and Amplitude (dB) of S21 for each of the four phase states should be measured and recorded. Measurements should be compared to the plots in the Simulations section of this paper.

Summary and Conclusions

A 2-bit MMIC phase shifter was designed using the Triquint Semiconductor TQPED process and Agilent ADS. Specifications were given for the project. Simulations show the circuit meets some, but not all, of those specifications. The phase shifter did not meet the insertion loss or insertion loss balance specifications. The variation in insertion loss of any one filter is not more than 1dB. Therefore, attenuators could have been used to achieve the insertion loss balance specification. However, the insertion loss specification would not be satisfied. To achieve the insertion loss specification, more attention needed to be paid to impedance matching in the phase shifter. For instance, the parasitics of the switches and of the neighboring filter through the low-isolation switch need to be explicitly incorporated into the design. The method used here was to tune the filter components after the interconnecting lines were added in layout. The low switch isolation made this a difficult process because when one filter was tuned, it detuned the others. One solution to this would be to use compound FET switches, therefore better isolating the filters form one another.