

Making Microwaves MMIC VCO Design Via Impedance Matching

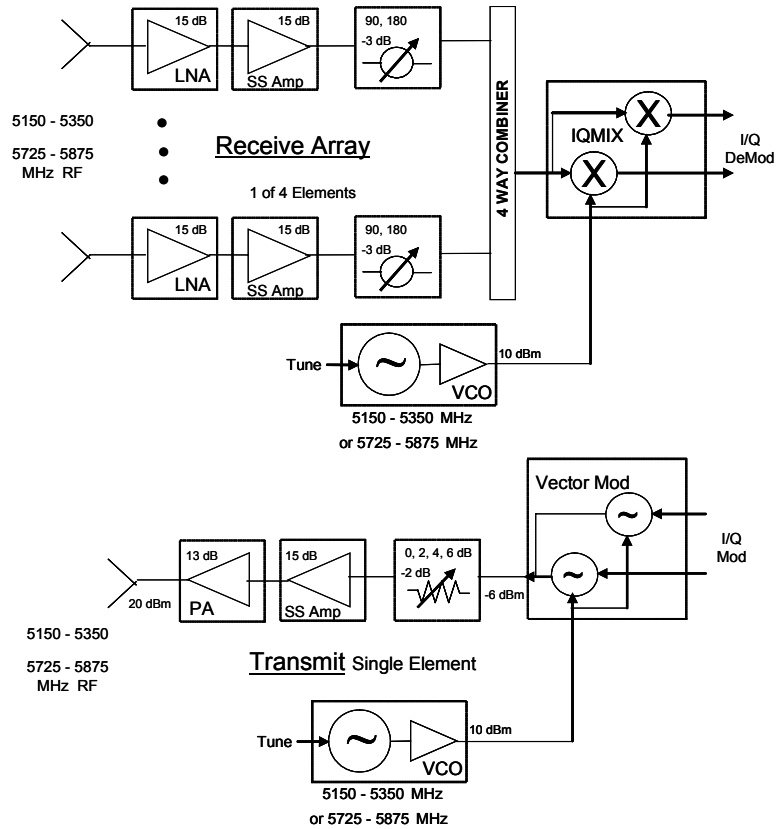
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Abstract

This final design report for the John Hopkins University Fall 2005 MMIC Design course details the design of an MMIC VCO. The MMIC VCO is designed on the TRI-Quint TQPED process. The VCO design goals are a tuning range of 5150 to 5350 MHz or 5725 to 5875 MHz, maximum 5 volt supply, 0 to 0.6 volts for control, lowest phase noise and an output power greater than +7 dBm. The emphasis of this report is on making the VCO cover both tuning ranges and choosing the varactor. An on chip Emode PHEMT device is used for the varactor. Microwave Office is used for the simulation and layout.

1. Introduction

The design project for the Fall 2005 MMIC Design class at The Johns Hopkins University is a duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies. For transmission, a direct vector modulator is used to transmit data onto the carrier. For downlink, an I/Q down converter is used to derive modulated data. The frequency carrier consists of a VCO. The VCO operates from 5150 to 5350 MHz, or



Chip Set for the 5150 - 5350 MHz WLAN and 5725 - 5875 MHz ISM Bands

Figure 1 Project block diagram

5725 to 5875 MHz, to cover the WLAN and ISM frequencies. A phase shifter chip implements a 2 bit phase for the receive array. Transmit level control is implemented with the MMIC attenuator chip. Each element of the receive chain array consists of an LNA and a driver amplifier in cascade, followed by a phase shifter. The transmit path employs a driver amplifier feeding a 100 milliwatt power amplifier. Nine unique MMIC designs make up the S-band transceiver. Each design is to be contained on a 60 mil square die in the TQPED process. The proposed block diagram is shown in Figure 1.

The emphasis of this report is on the VCO design and test procedure. The VCO is designed on the Tri-Quint TQPED process. Microwave Office is used for the simulation and layout. Utilizing the device's small signal parameters, the oscillator is designed using the reflection method. A non-linear simulation was ran to check the output power and phase noise. No optimization is done based on the non-linear simulation. The drain and source of an Emode PHEMT is grounded to make varactor using the TQPED process. The design chronicles the design process. Using the available 60x60 mil die area the circuit is laid out. A test procedure is detail in the test section and the expected results are summarized in the conclusion section

2. Design

The VCO is designed using the reflection method (often called negative impedance method) of oscillator design. The essence of this method is to reduce a non-linear three terminal device to a linear two port equivalent circuit and match the two ports appropriately. In this instance the PHEMT (3 terminal device) gate is taken as one port and the drain is taken as the other port. It is accepted that if the device is oscillating in one port, it must also be oscillating in the other port. The output can be taken at either the drain or the gate. To achieve maximum output power the drain is chosen for the output. This leaves the gate for the resonant circuit. Now that the function of each port is identified, like most other microwave designs, the linearized circuit is now an impedance matching task. Unlike other microwave designs, choosing the proper terminating impedance is not a strait forward task and requires iteration. The details of the VCO impedance matching are chronicled below.

The operating point was chosen to meet the power requirement ($V_d=3.0$ volt, $I_d=15$ mA) and reduce the noise.

2.1. Examine FET to determine topology

The gain and stability factor of the non-linear PHEMT model is plotted in Figure 2. The PHEMT's measured s-parameter data is also plotted to increase confidence in the non-linear model. The non-linear and linear model agree up to ~14 GHz. This is sufficient for this design.

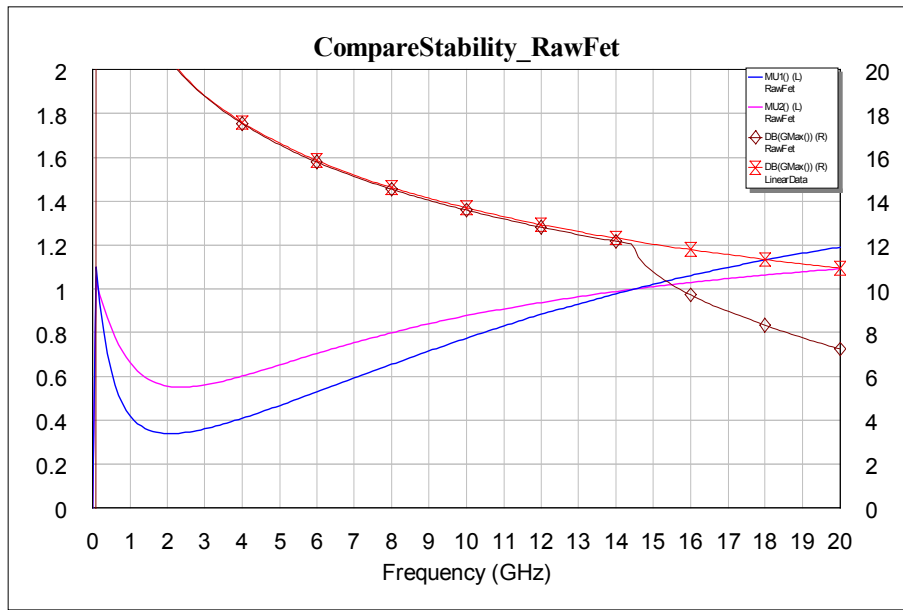


Figure 2 Gain and stability of PHEMT. Gain and stability shown for linear and no-linear model.

The device has a lot of gain at the lower frequencies and is conditionally stable. Compensation must be added to the device to reduce the lower frequency gain and stabilize the device outside the desired oscillation frequency range. This must

be done to insure the oscillation occurs at the desired frequency. The compensated device and its response is shown in Fig. 3. The device is compensated in the source. This works out splendidly because a bias resistor must be added to utilize a single supply bias.

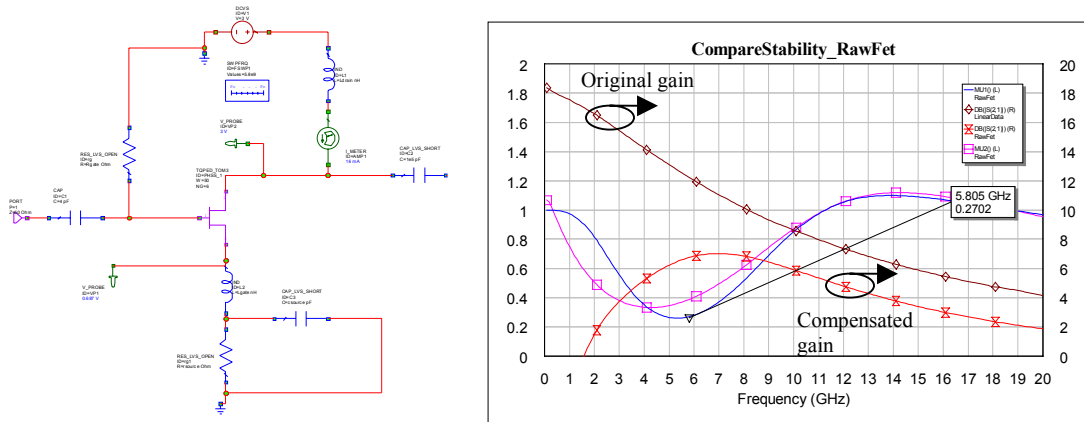


Figure 3 On left the compensated device. Plotted on right is the compensated device's response

Referring to Fig. 3, notice the stability factor is 0.27 at 5.8 GHz. The stability factor relates to the magnitude of the reflection coefficient. As a rule of thumb this should be ~ 0.33 (the smaller the coefficient the less stable the device.) Because of the varactor loading effects, the device is made slightly more unstable than usual.

2.2. Choosing the gate load for oscillation

Now that the device is compensated and biased the gate matching requirement can be determined using the 2 port circuit response. Figure 3 will be used extensively to determine the proper gate matching requirement.

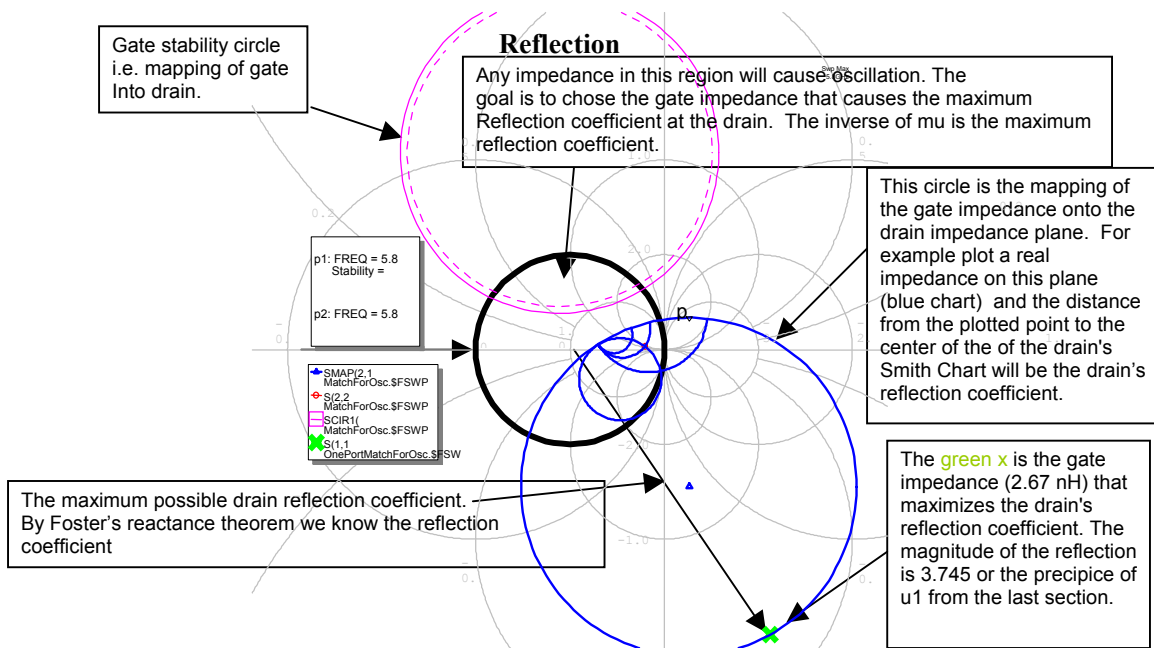


Figure 4 Plot showing the drain's reflection coefficient.

Figure 3 is a plot of the drain's (output) reflection coefficient at 5.8 GHz. The heavy black circle is the boundary of the unit Smith chart. The pinkish circle is a stability circle mapping the gate's impedance. Choosing a gate impedance in the overlapping region can cause the drain reflection coefficient to be greater than unity i.e. oscillate. The problem is choosing the best gate impedance. A reasonable criterion is to select the impedance which maximizes the drain's reflection coefficient. Recall we know the maximum drain reflection from the last step, $1/u_1=3.745$. A convenient way to determine the gate impedance is to map all possible gate impedance's onto the drain's reflection coefficient's plane. The blue circle is this mapping (very nice feature of Microwave Office). The green X on the mapping (blue circle) represents the maximum drain reflection coefficient. This is verified by replacing the gate with the requisite gate impedance (2.67 nH) and plotting the drain reflection coefficient. As expected

the drain reflection coefficient is 3.7. The gate impedance should be 2.67 nH for a maximum drain reflection coefficient.

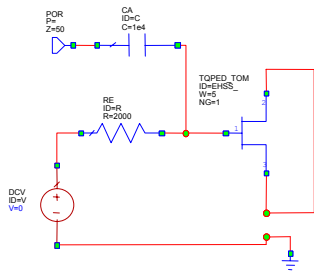
2.3. Designing the varactor

The source and drain of a PHEMT is grounded to a make varactor. The critical parameters are the available tuning range and the Q. Two varactor configurations were considered, a 6 finger device or a 10 finger device. The equivalent circuit model for each device is determined and used for comparison.

The equivalent circuit model and the matching between the model and the actual device are shown in Figure 4. Notice the model accurately matches the device over .1 to 20 GHz. This indicates the model is good.

Table 1 shows the capacitance and ESR for a 6 finger and a 10 finger device over the tuning voltage. The 10 finger device has a lower ESR. The 10 finger device will be used in this design.

Varactor test circuit



Varactor equivalent

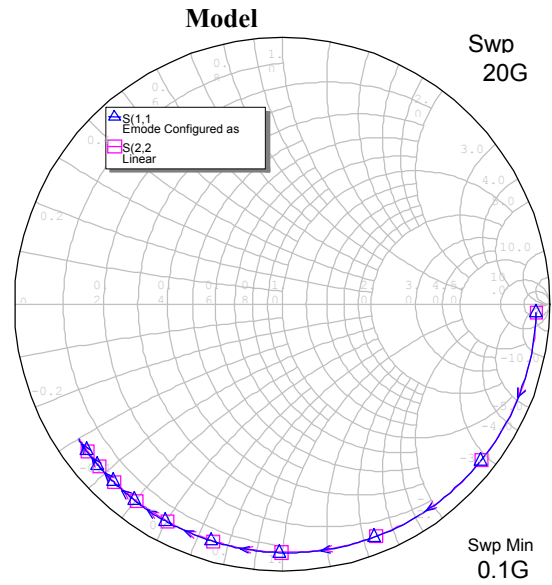
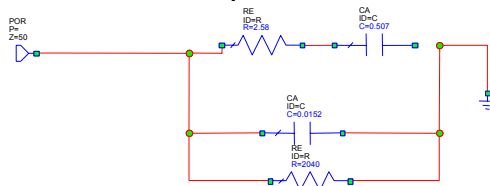


Figure 4 Varactor model

Table 1 Table of varactor capacitance and ESR for a 6 finger and 10 finger device.

Vtune	6 Finger (pF)	6 Finger (ohms)	10 finger (pF)	10 finger (ohms)
0	0.249	6.9	0.507	2.58
0.2	0.381	5.8	0.78	2.58
0.4	0.7	4.9	1.29	2.58
0.6	1.32	4.3	2.3	2.25

2.4. Design the gate matching network.

Now that the varactor model and the desired gate match has been determined, the gate matching network can be designed. The gate circuit is shown in Figure 5.

The ideal gate match was an inductor. The limited Q of the inductor and varactor

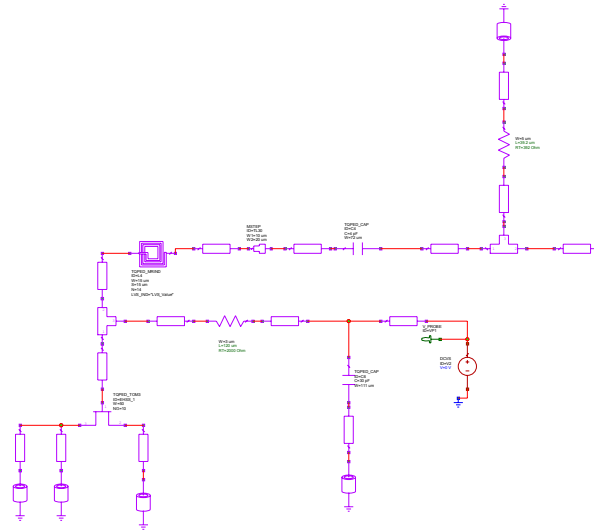


Figure 5 The gate circuit with varactor.

make realizing this match over a wide frequency range difficult.

2.5. Drain/load matching

The load circuit should present the correct phase rotation and loading as determined in Figure 3. The correct phase is 180 degrees i.e. rotating the reflection coefficient to resonance. The resonance type can be read off the Smith chart. The resonance is series. Note the gate match from the previous step is used to determine actual matching values. A rule of thumb is to make the loading impedance one third the negative impedance.

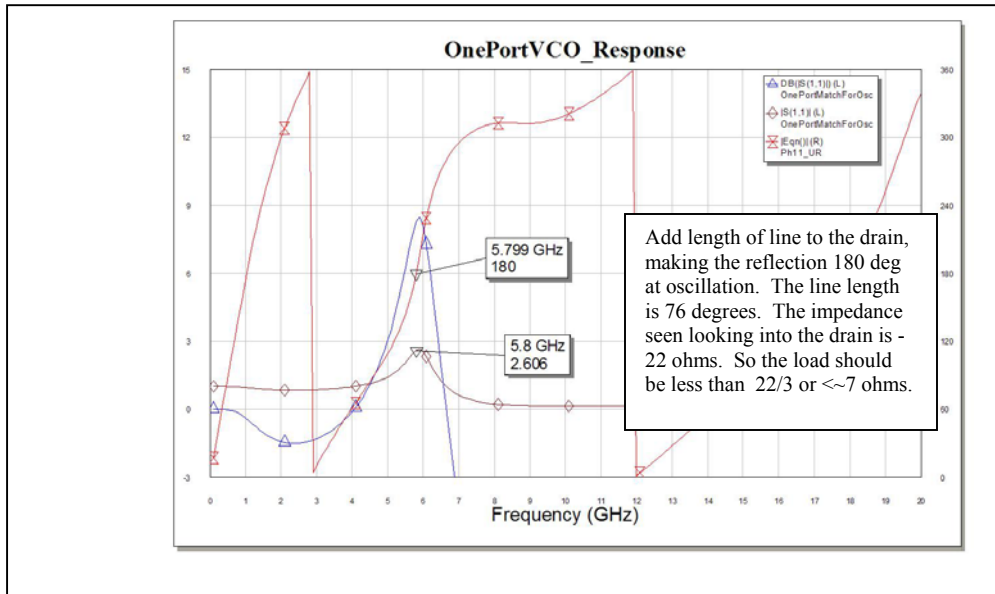


Figure 6. Drain reflection with gate and source match. The output is and ideal match.

The ideal match was converted to a 2 element match at a single frequency. This simple matching circuit may not be sufficient, because the reactance slope has not been matched. At this point in the design the circuit was laid out and design rule checked. A more complex output matching circuit was designed. The more complex matching circuit had trouble fitting into the available space. Due to time requirements the decision was made to go with the simple output matching circuit that had passed the design rule check. The circuit passed design rule checking and no further iterations were performed.

2.6. The VCO response

The completed matched circuit is shown in

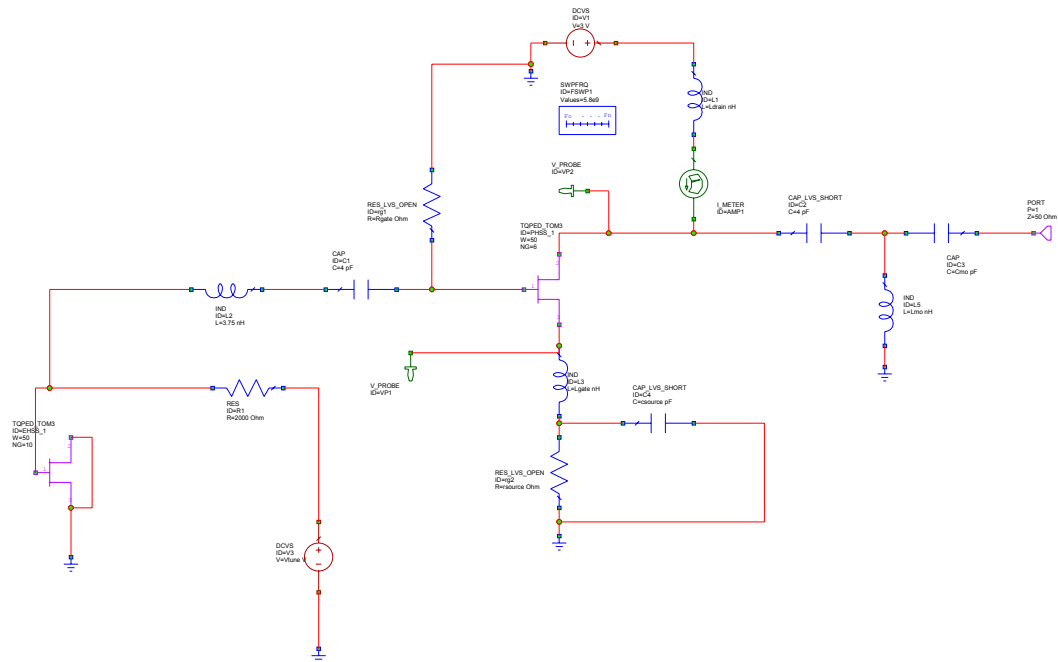


Figure 7. The VCO

The output reflection coefficient for $v_{tune}=1$ and 0 volt is shown in Figure 9 and Figure 8. The VCO should operate over the full range. The reflection coefficient is small at the lower end on the range and may not oscillate.

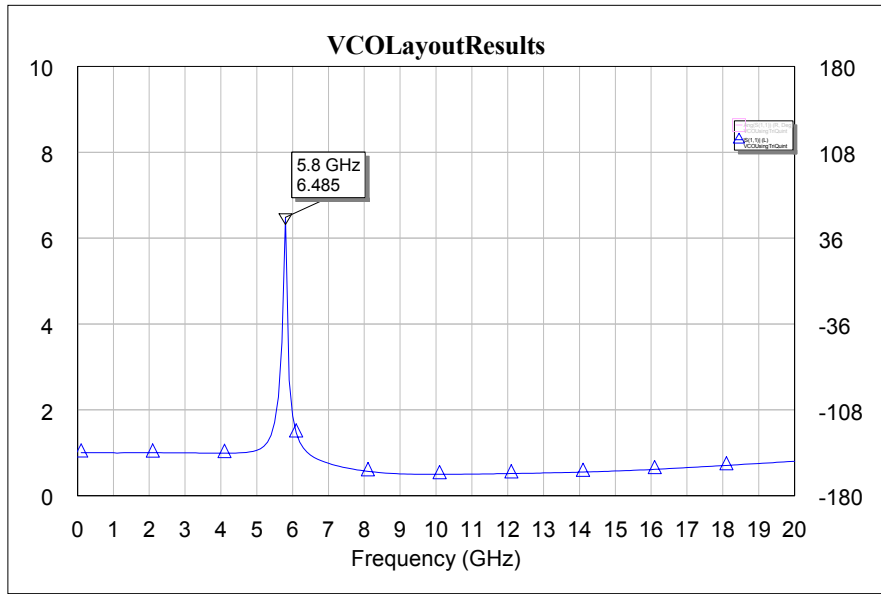
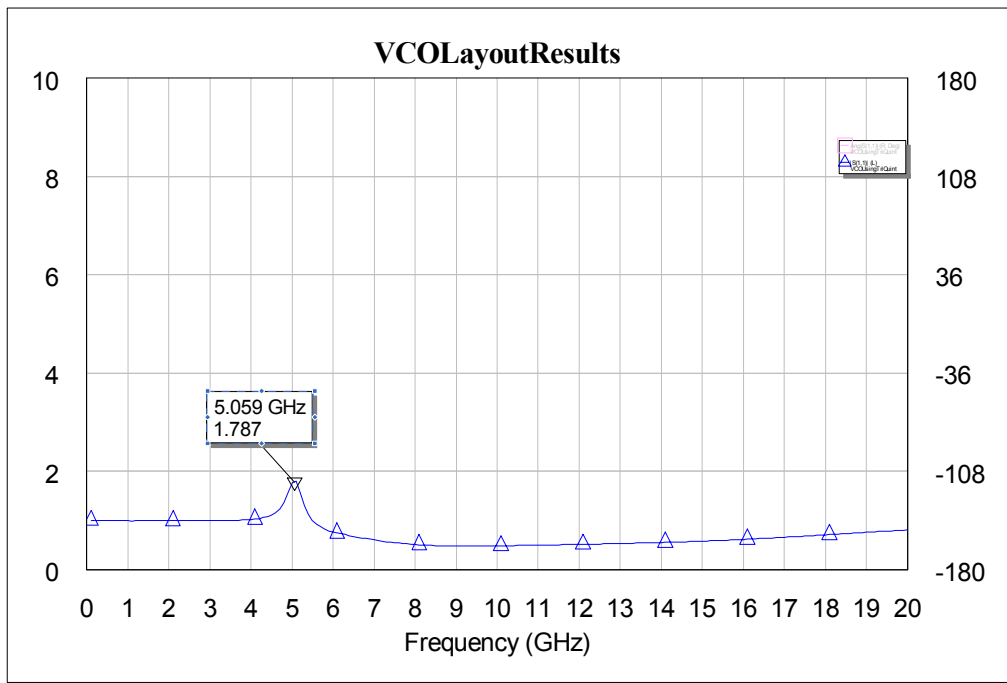


Figure 8. Drain reflection of VCO vtune=0 volts



Notice the reflection coefficient in Figure 9 is only 1.7. The rule of thumb was to have a reflection coefficient of ~3. In Figure 8 the reflection coefficient is 6.4, much greater than the desired 3. The phase is not 180 for either response. In

the middle of the tuning range the phase aligns and the reflection is 3. The phase across the tuning range and the magnitude of the reflection coefficient was comprised to increase the tuning range of the VCO. The output matching requires more optimization. When the layout passed the rule checking the next iteration of optimization was halted. The thought being these are rules of thumb and the non-linear response of the oscillator will compensate the phase.

Using the oscillator probe in MWO, a harmonic balance simulation was run. The predicted spectrum and phase noise is shown in Figure 10 and Figure 11.

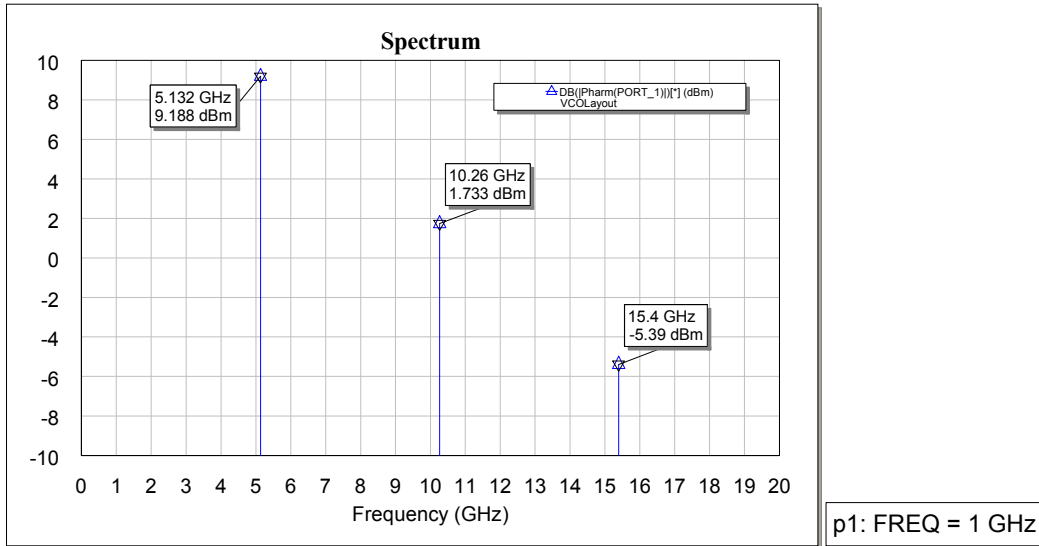


Figure 11

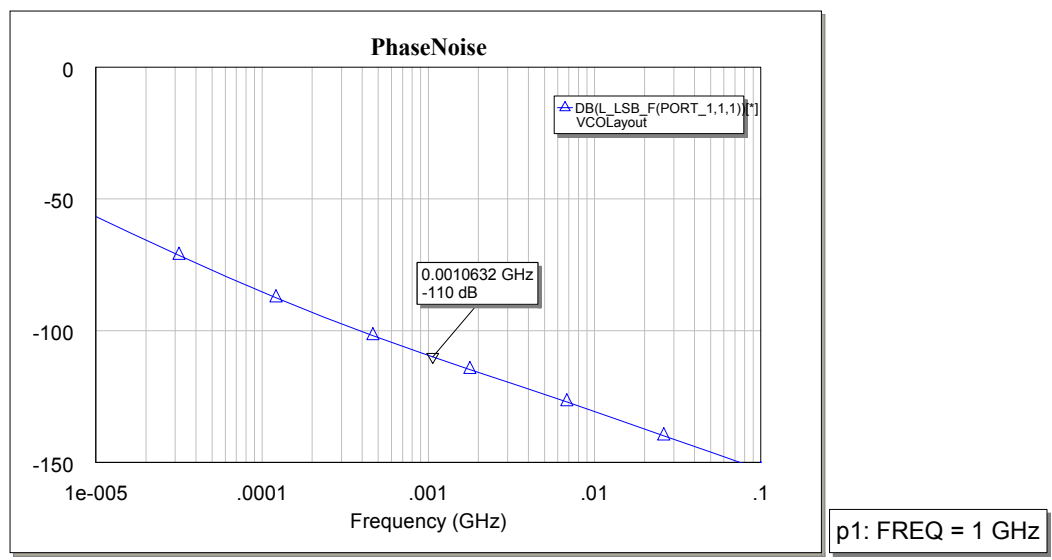
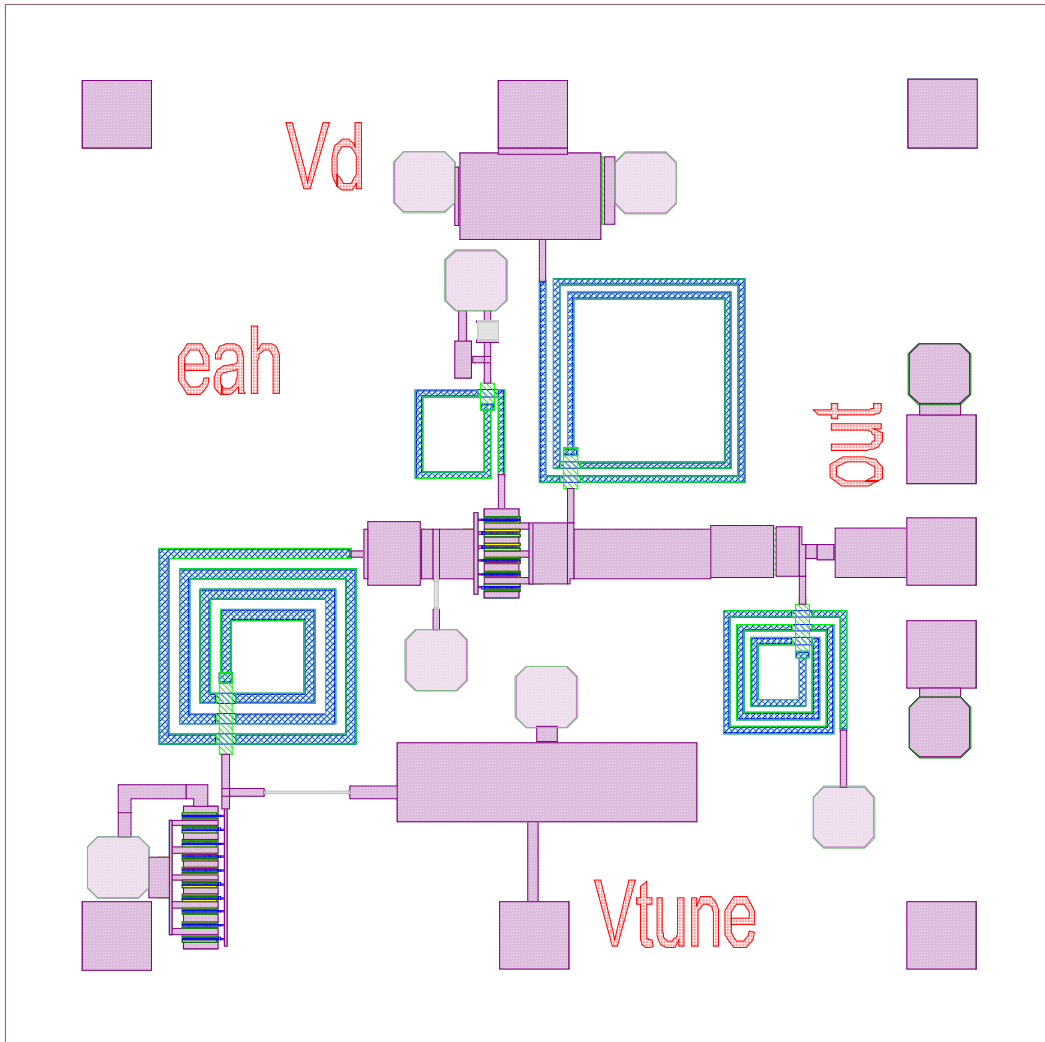


Figure 11. Predicted phase noise of the VCO using the MWO oscillator port, vtune=0.25 volts.

The non-linear simulation indicates the VCO will be low in frequency (4.9 to 5.3 GHz). The non-linear simulation oscillation frequency depends on the probe placement and the initial start and stop values. Measurements will indicate the truth.

3. VCO Layout

The layout is shown below.



4. Test Plan

Place the circuit in the probe station. Apply the bias voltage of 3 volts to the terminal labeled Vd. Verify the circuit is drawing ~15 mA. Apply a second DC probe to the terminal labeled Vt. This port should control the oscillation frequency. Apply a third RF probe to the labeled RFout. This port should be connected to a spectrum analyzer similar to the HP 5668E. With the spectrum analyzer on full span verify the oscillation is present. If present swing the tune voltage between 0 and 1 volt and verify the oscillation movement is continuous. Fill out the table below.

Vtune	fo (GHz)	Power @ fo (dBm)	2xfo (dBc)	@ 100 kHz (dBc/HZ)	@1M (dBc/HZ)
1.0					
0.8					
0.6					
0.4					
0.3					
0.2					
0.1					
0.0					

5. Conclusion

An MMIC VCO was designed using the Tri-Quint TQPED process. Microwave office was the tool used to simulate and layout out the circuit. The reflection method (negative impedance) method as used to design VCO. The VCO is expected oscillate. According non-linear simulation the oscillation will be low and have a reduced tuning range. Linear simulation also indicates a sluggish VCO response due to excessive loading in the output circuit. The output loading was not reduced in an effort to increase the VCO tuning range. Another iteration of output matching could possibly improve the oscillator performance.

According to the linear simulation the oscillator should oscillate from 5.0 GHz to 5.8 GHz. Using the linear simulation and the load line the output power should be $\sim +7$ dBm. The expected results from the non-linear simulation are summarized

Vtune	Fo	dBm	dBc/Hz
1.0	4.908	4.9	-112
0.8	4.952	4.9	-112
0.6	4.971	8.4	-112
0.4	5.063	8.9	-111
0.3	5.123	9.2	-110
0.2	5.161	9.2	-109
0.1	5.22	9.5	-109
0	5.284	9.6	-109