C-Band Vector Modulator and I/Q Demodulator

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Abstract – This paper details a C-Band .5um pHEMT Vector Modulator and I/Q Demodulator with an I/Q frequency of 50 MHz. The design was simulated using Agilent's Advanced Design Systems along with models supplied by TriQuint. The simulations predict the Vector Modulator to have a minimum insertion loss of ~5dB and the I/Q Demodulator has a conversion loss of ~3dB.

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1. Introduction

1.1 Circuit Description – Vector Modulator

The vector modulator design consists of a 90-degree hybrid to split the RF input into I/Q components, two attenuators to control the amplitude and sign of the I and Q components, and a combiner to sum the two signals. Because of the limited amount of space, the 90-degree hybrid was realized using a lumped element equivalent circuit. Reflective attenuators were designed using the same 90-degree hybrid along with two transistors biased as variable resistors by the I and Q inputs. The combiner is a simple lumped element Wilkinson design.

1.2 Circuit Description – I/Q Demodulator

The I/Q Demodulator uses the same architecture except for the replacement of the variable resistors with diode connected FET's. The RF and LO signals are fed into the two RF pads (they can be interchanged), and the 50 MHz I/Q outputs will vary in amplitude depending on the relative phase of the RF signal with respect to the LO signal. The diodes are driven on by the LO input, which was simulated at an input level of +12 dBm to the entire chip.

2. Design

2.1 Lumped Element 90 degree hybrid

The 90 degree hybrids used in both circuits are a simple lumped element design optimized at a center frequency of 5.5 GHz. For this frequency, a distributed network was unrealizable in the given area. The ideal hybrid was converted to a lumped element circuit by replacing the quarter wavelength sections with equivalent low pass networks.

2.2 Wilkinson Divider

Similarly to the 90 degree hybrid, the Wilkinson divider/combiner was realized with equivalent lumped elements at C-band due to size constraints.

2.3 Transistor Sizing for Vector Modulator

For the Vector Modulator, the range of the variable resistors is the determining factor in the range of the reflective attenuators. Ideally, a perfect short and a perfect open would yield an attenuation range of +1 to -1. A large resistance is easy to obtain by putting a large enough negative bias on the gate of the FET. Creating a good short requires a larfe FET, but a large FET also adds parasitic capacitance that can skew the constellation of the vector modulator. A 105 um FET turned out to be a good compromise. With a gate bias of +.5 volts, the FET had a series resistance of about 10 ohms. The capacitance of the FET was negligible at the frequency of interest. Assuming I/Q inputs of -.7 to +.5 volts, our total range of resistance is approximately 10 to 250 ohms.

2.4 Diode Sizing for I/Q Demodulator

For the I/Q Demodulator, we used diodes sized to be approximately 50 ohm loads. This was done to minimize the effects of the diodes on the 90 degree hybrid. With a 12 dBm input, the diodes should be operating near the threshold voltage, so the diodes were sized based on a bias of .7 volts. Diode connected FETs with a single finger of 50 um turned out to be about 50 ohms at this bias level.

2.5 Layout Design

The layout of the 90 degree hybrid circuits was done to minimize the interaction of the two reflective attenuators and any possible cross-talk between the I and Q components. The 90 degree hybrids and the Wilkinson were then re-optimized to compensate for the interconnect within the individual components. The next step was to interconnect the hybrid circuits and Wilkinson and then add in the FETs. Another iteration of tuning was necessary to compensate for this lengthy interconnect. See figures 1 and 2.

3. Simulations

3.1 Vector Modulator

The vector modulator was simulated with swept DC inputs for the I and Q signals. Careful considerations were made to ensure that this circuit would work at the specified 50 MHz as well.

Figure 1 shows a polar plot of the output constellation with gate biases swept from -.7 to +.5 volts. As you can see, it has a usable range out to an amplitude of .3, or just over 5 dB of loss. This complies with the specified loss goal of no more than 7 dB. It should be noted that the output is highly nonlinear with respect to the I/Q voltages. It is assumed that this will be compensated by the back end of the system.

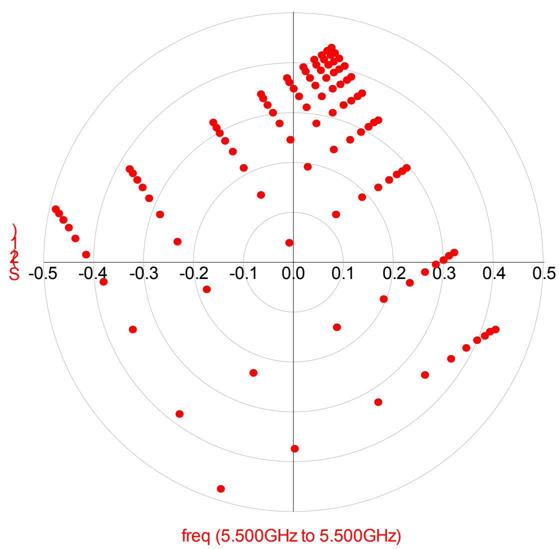


Fig 1 – Vector modulator output constellation

Figure 2 shows the RF input and output vswr, both of which meet the spec of 2.5:1. The output vswr comes close, but does not meet the goal of 1.5:1 at the upper edge of the band. The I/Q input vswr is nearly perfect due to the 50 ohm shunt resistor at these inputs.

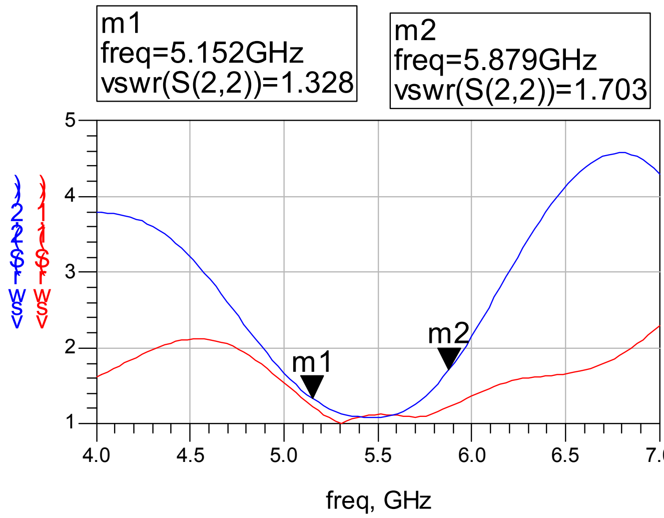


Fig 2 – Input and Output vswr

To evaluate the power handling capabilities of this circuit, the input power and the I/Q inputs were all swept together. It was determined that this circuit has the lowest 1 dB compression point when all of the FET's are biased to look like 50 ohm loads (approximately -.4 volts). The plot in figure 3 shows the compression of the circuit at this bias level.

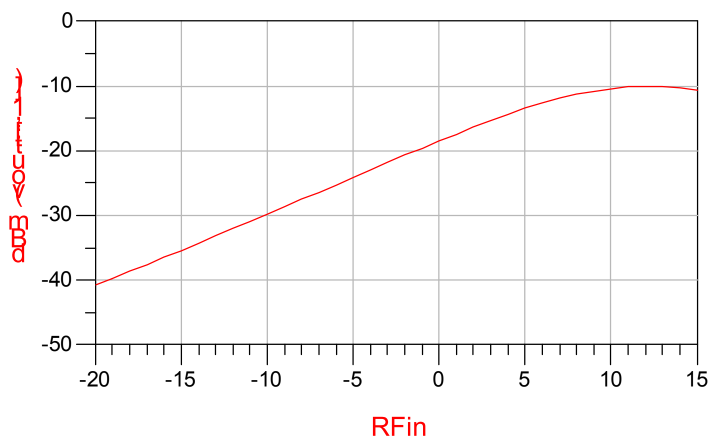


Fig 3 – Vector Modulator compression

3.2 I/Q Demodulator

The I/Q Demodulator was simulated using the ADS harmonic balance simulation tool. To vary the I/Q input, an ideal phase-shifter was placed at the RF input, and the phase was swept from 0 to 360 degrees. As figure 4 shows, the I and Q outputs (50 MHz) each have two peaks and are offset by close to 90 degrees. The simulation was done with an LO input power of +12 dBm to drive the diodes, and an RF input power of 0 dBm. These simulations show that there is only ~2dB of insertion loss in the circuit.

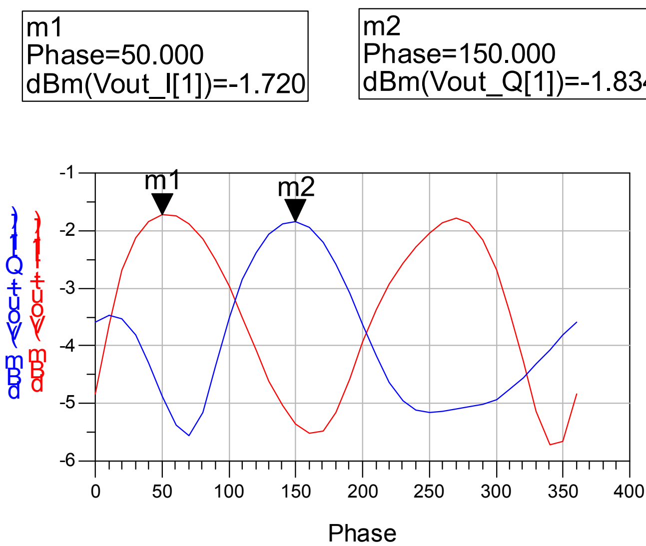


Fig 4 – I/Q Demodulator output vs. RF input phase

Similar to the vector modulator, the I/Q demodulator has good vswr, but it does not quite meet the goal of 1.5 at the upper edge of the band.

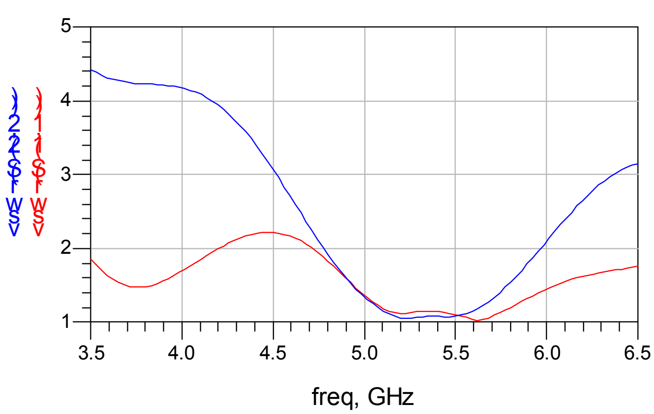
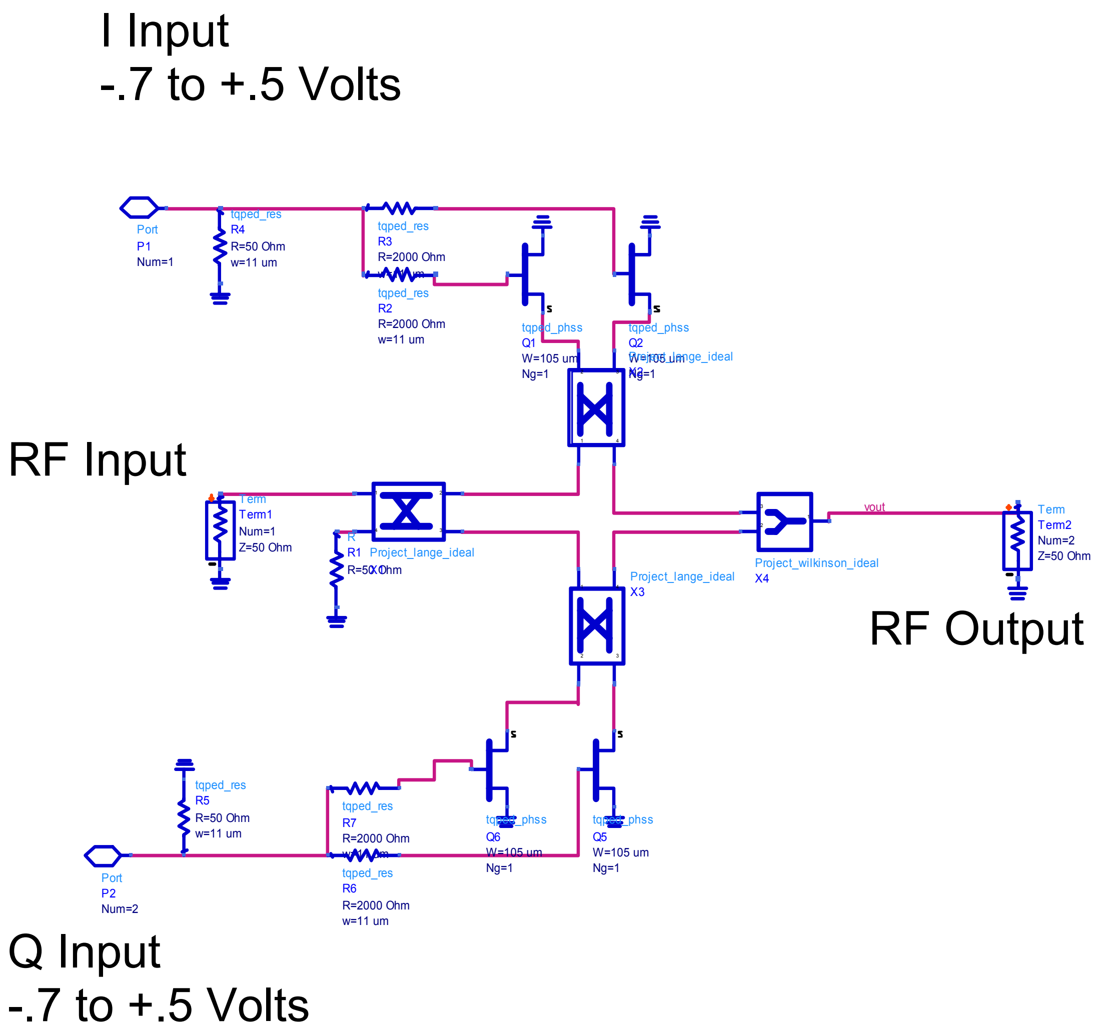


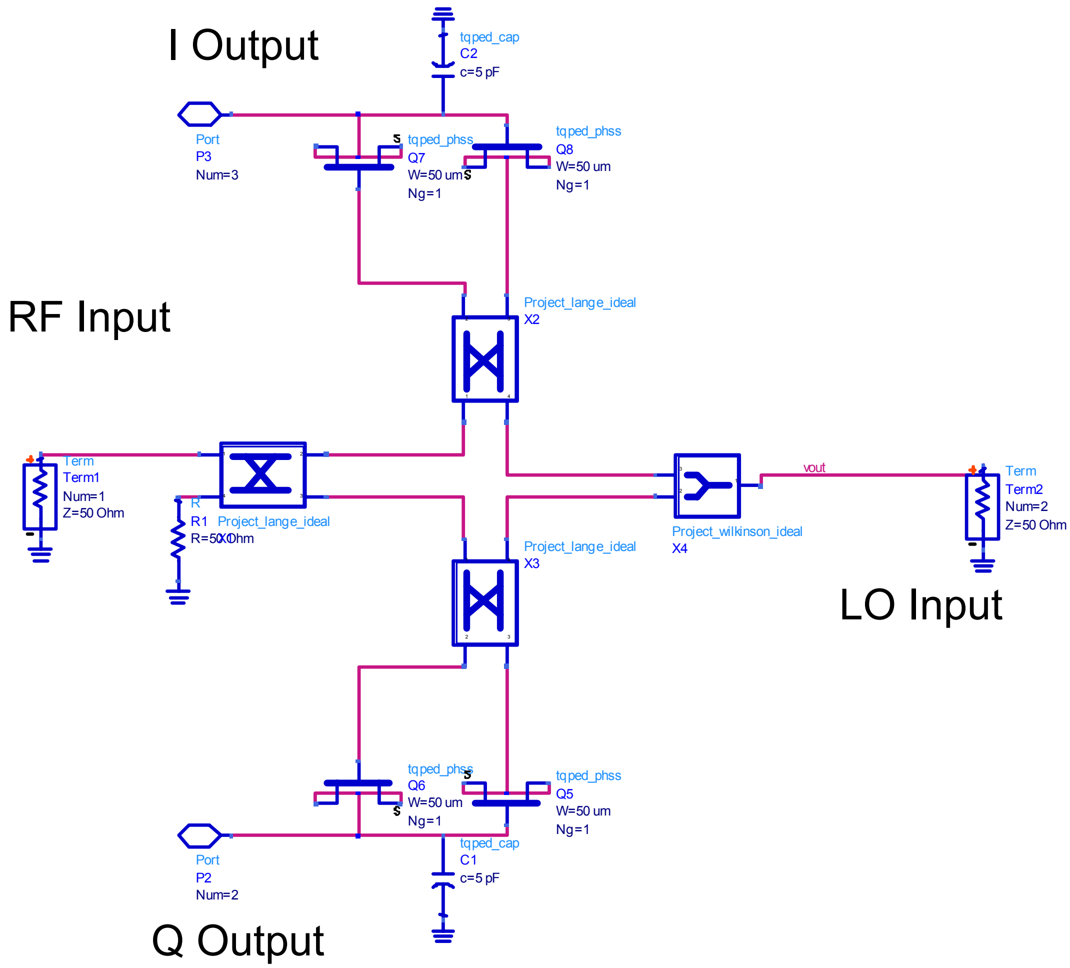
Fig 5 – I/Q Demodulator RF and LO vswr

4. Schematics

4.1 Vector Modulator Schematic

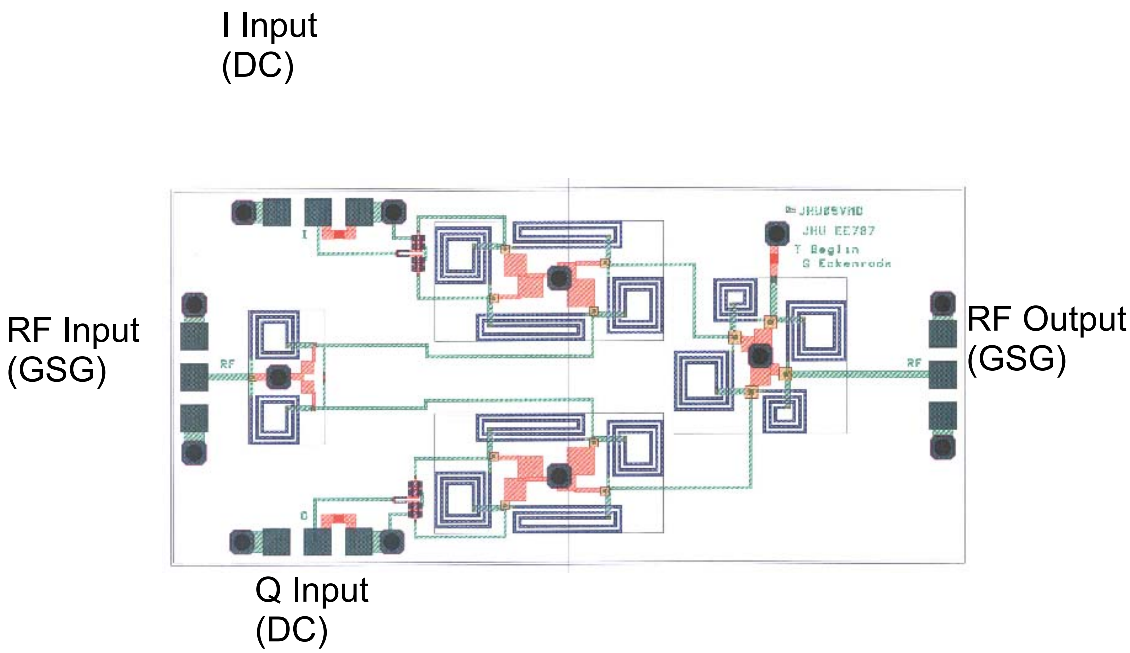


4.2 I/Q Demodulator Schematic

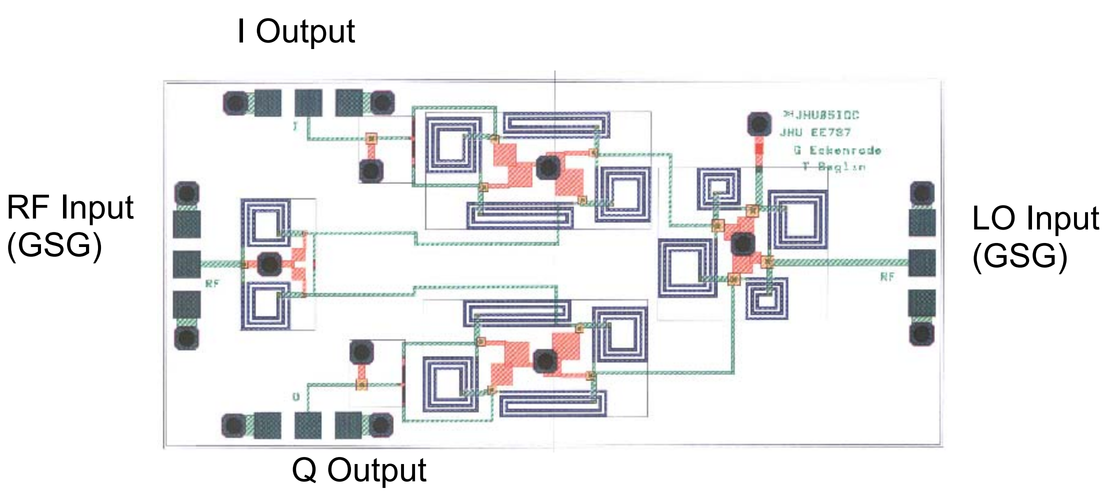


5. Layout

5.1 Vector Modulator Layout



5.2 I/Q Demodulator Layout



6. Test Plan

6.1 Test Equipment

- Agilent 8510 Network Analyzer
- DC power supply
- Two signal generators with phase-locking capability
- Spectrum anlayzer

6.2 Test Procedure

6.2.1 Vector Modulator Test Procedure

The Vector Modulator can be easily tested by measuring the RF input to RF output on a network analyzer. First, a calibration from 5 to 6 GHz should be performed on the network analyzer. Measurements of the device should then be taken with each of the bias settings listed in the table below. After the data has been taken, single frequency points can be plotted on a polar chart across bias settings to verify a good constellation of RF output magnitudes and phases.

Input Voltages	
I	Q
-.7	-.7
-.7	-.3
-.7	.1
-.7	.5
-.3	-.7
-.3	-.3
-.3	.1
-.3	.5
.1	-.7
.1	-.3
.1	.1
.1	.5
.5	-.7
.5	-.3
.5	.1
.5	.5

6.2.1 I/Q Demodulator Test Procedure

The I/Q Demodulator will require two RF sources phase locked together with an offset of 50 MHz. These signals should be input into the RF and LO GSG pads on the device, and the I/Q outputs should be observed on a spectrum analyzer. The input power should be 0 dBm on the RF input and 12 dBm on the LO input. To test that the I and Q components are being separated out of the RF signal, a relative phase shift will have to be inserted between the RF source and the device.

This can be realized by lengthening the cable between the RF source and the device in small increments (possibly with several RF connectors in a row). The relative changes in phase of this cable should be measured on a network analyzer prior to beginning this test. The amplitude of the 50 MHz I/Q outputs should then be measured and plotted versus the relative phase shift (see simulation plot in section 3.2).

7. Conclusion

The design of a C-Band Vector Modulator and I/Q Demodulator have been described. The simulations were performed using ADS and they showed that the vector modulator will have an insertion loss of ~5 dB while the I/Q demodulator will have a conversion loss of ~2 dB. The designs will be fabricated at TriQuint using the .5um pHEMT process.

8. References

1. Penn, John E. "A Balanced Ka-Band Vector Modulator MMIC." *Microwave Journal,* June 2005.