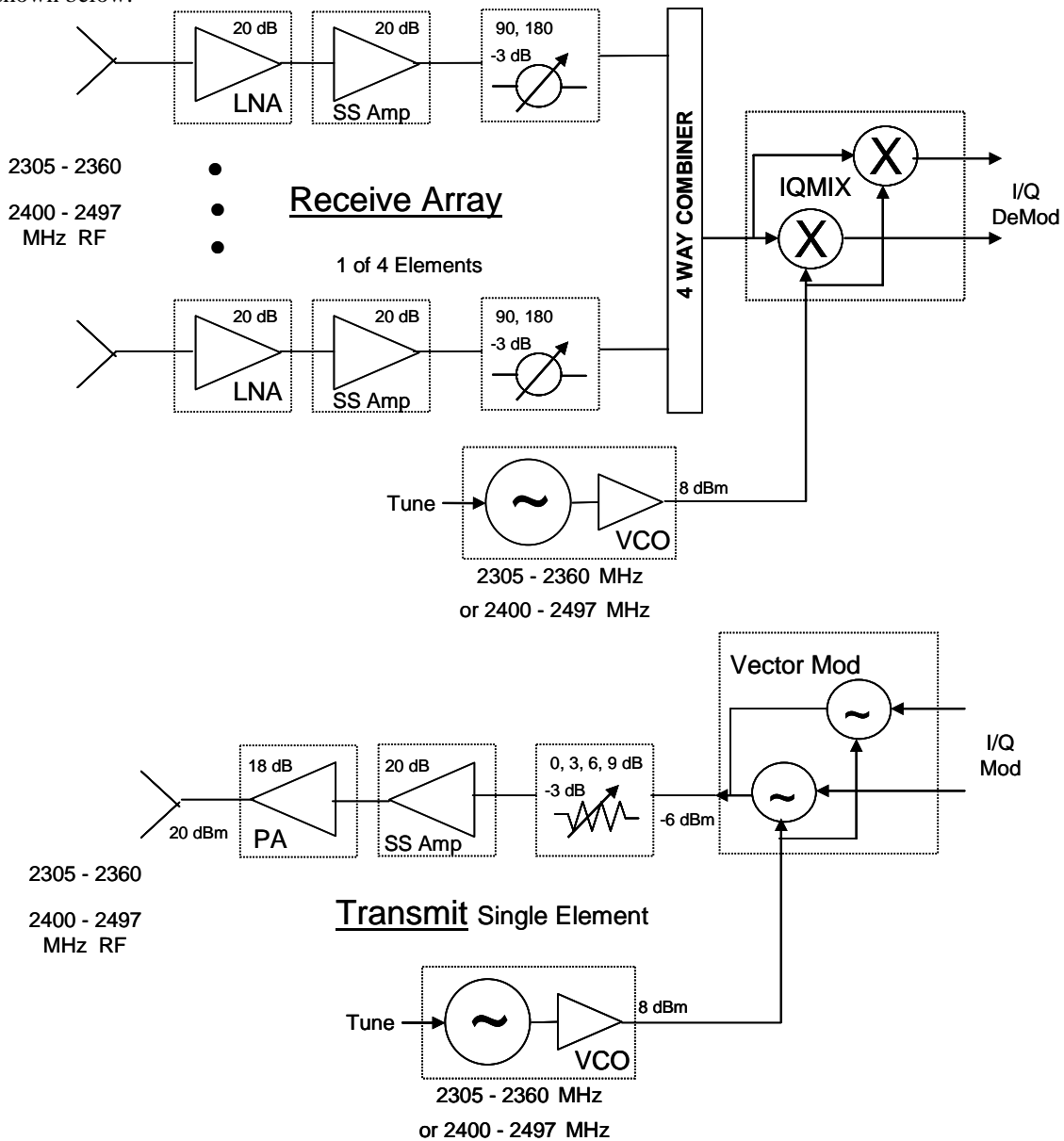


MMIC DESIGN EE 525.787 FALL 2006

STUDENT PROJECTS

This year's project for the MMIC Design class at The Johns Hopkins University is a duplex transceiver employing a receive array for the S-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies. For transmission, a direct vector modulator is used to transmit data onto the carrier. For downlink, an I/Q down converter is used to derive modulated data. The frequency carrier consists of a VCO. The VCO operates from 2305 to 2497 MHz to cover the WCS and ISM frequencies. A phase shifter chip implements a 2 bit phase for the receive array. Transmit level control is implemented with the MMIC attenuator chip. Each element of the receive chain array consists of an LNA and a driver amplifier in cascade, followed by a phase shifter. The transmit path employs a driver amplifier feeding a 100 milliwatt power amplifier. Nine unique MMIC designs make up the S-band transceiver. Each design is to be contained on a 60 mil square die (TBD) in the TQPED process. The proposed block diagram is shown below.



Chip Set for the 2305 - 2360 MHz WCS and
2400 - 2497 MHz ISM Bands

PROJECTS

Low Noise Amplifier - 20 dB gain, 2 dB NF

Low Noise Amp 2 - 15 dB gain, 3 dB NF, 10 mW DC-PMODE (small devices!)

D. Sokol (LNA)

N. Hughes/L. Majecka (Low power LNA)

SS Amplifier – 20 dB Gain, +20 dBm IP3

C. Wedderburn (Small Signal Amp)

Vector Modulator – 2305 to 2497 MHz, 7-10 dB conversion loss

J. Egan (Vector Modulator)

I/Q Down Converter – 2305 to 2497 MHz, 7-10 dB conversion loss

Attenuator – goal 3 dB IL, 3 dB steps, 2 bit control

Power Amplifier – 100 milliwatt, 18 dB gain, high efficiency

Medium Power High Efficiency Amplifier – 25% PAE, 18 dB gain

B. Myers/ N. Patel (PA)

P. Smith (Med. Power PA)

Voltage Controlled Osc. - 2305 to 2497 MHz tuning range

D. Loizos (VCO)

2 bit Phase Shifter – goal 3 dB insertion loss, 1/2 LS bit accuracy

D. Wendland (Phase Shifter)

GENERAL CONDITIONS

TriQuint:

TQPED Process, with vias

4 mil (100 micron) thick wafer

60 x 60 mil die (ANACHIP) (60 x 120? For VM and IQ Demod)

TOM3 FET model in ADS

Testing:

Agilent 8510 VNA (45 MHz to 26 GHz)

Cascade Model 43 wafer probe station with

up to 4 RF probes & 4 DC needle probes

Synthesized signal generators to 26 GHz

Spectrum analyzer to 18 GHz

SPECIFICATIONS FOR S BAND LOW NOISE AMPLIFIER

*On chip high Q matching networks, source inductance
and FET size tuned for low noise with good input VSWR*

FREQUENCY:	2305 to 2497 MHz
BANDWIDTH:	> 800 MHz
GAIN:	> 20 dB
GAIN RIPPLE:	± 0.5 dB goal.
NOISE FIGURE:	< 3 dB; 2 dB, goal
INPUT IP3:	> +5 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	± 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR S BAND LOW DC POWER LOW NOISE AMPLIFIER

Similar specs but an additional 1 dB higher NF, more gain ripple, and no IP3 spec. Use 60 um (4x15) Dmode or Emode PHEMTs for one or two stage design. Emode is preferred since it has higher gain with slightly less noise figure than the Dmode. Single supply voltage at 3.3 V for battery power (3-3.6V range)..

GAIN RIPPLE:	± 1 dB goal.
NOISE FIGURE:	< 4 dB; 3 dB, goal
INPUT IP3:	NA
SUPPLY VOLTAGE :	+ 3.3 Volts only, goal (3 to 3.6V range)

SPECIFICATIONS FOR SMALL SIGNAL AMPLIFIER

Two stage amplifier with on chip bias network and FET size tuned for efficient Class A power operation with good input & output VSWR

FREQUENCY:	2305 to 2497 MHz
BANDWIDTH:	> 800 MHz
GAIN small signal:	> 20 dB goal
GAIN RIPPLE:	± 0.5 dB goal
OUTPUT IP3:	> +20 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	± 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR S BAND VECTOR MODULATOR

switch attenuators with lumped element match for RF..

FREQUENCY:	RF = 2305 to 2497 MHz, I/Q to 50 MHz
ISOLATION:	I/Q to RF 10 dB min.; 16 dB goal
CONVERSION LOSS:	10 dB max.; 7 dB goal
RF POWER:	up to +7dBm max 0 dBm goal
VSWR, 50 Ohm:	2.5:1 max.; 1.5:1 goal
SUPPLY VOLTAGE:	Variable, 0 to 5 Volts TBD
SIZE:	60 x 120 mil ANACHIP

SPECIFICATIONS FOR S BAND I/Q DE-MODULATOR

diode mixers with lumped element match for RF..

FREQUENCY: RF = 2305 to 2497 MHz, I/Q to 50 MHz

ISOLATION: I/Q to RF 10 dB min.; 16 dB goal

CONVERSION LOSS: 10 dB max.; 7 dB goal

RF POWER: up to +7dBm max 0 dBm goal

VSWR, 50 Ohm: 2.5:1 max.; 1.5:1 goal

SUPPLY VOLTAGE: Variable, 0 to 5 Volts TBD

SIZE: 60 x 120 mil ANACHIP

SPECIFICATIONS FOR S BAND POWER AMPLIFIER

*On chip drain and gate bias network, output matching network,
and FET size tuned for efficient power operation with
good input & output VSWR*

FREQUENCY:	2305 to 2497 MHz
BANDWIDTH:	> 800 MHz
GAIN, small signal:	> 18 dB; 20 dB, goal
GAIN RIPPLE:	± 0.5 dB max.
OUTPUT POWER:	> +20 dBm @ 1 dB compression
POWER ADDED EFFIC.	> 20 % @ 1dB compression; 25 %, goal
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE:	+ 5 and -5 Volts
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR S BAND MEDIUM POWER AMPLIFIER

Similar specs but the goal is efficiency to get the most RF output power for a given DC consumption (i.e. battery life). More gain ripple, and a single supply voltage at 3.3 V for battery power (3-3.6V range). Use 60 um (4x15) Dmode or Emode PHEMTs for one or two stage design. Emode is supposed to have higher gain for a given DC power consumption than the Dmode, but be sure to simulate output power and efficiency of both devices before choosing.

GAIN RIPPLE:	± 1 dB goal.
OUTPUT POWER:	TBD @ 20-25% PAE (Power Added Efficiency)
SUPPLY VOLTAGE :	+ 3.3 Volts only, goal (3 to 3.6V range)

SPECIFICATIONS FOR S BAND VOLTAGE CONTROLLED OSCILLATOR

On chip high Q resonator and tuning varactor. One design for each band.

FREQUENCY: 2305 to 2497 MHz

OUTPUT POWER: > +7 dBm; +10 dBm goal

CONTROL VOLTAGE: 0 TO -5 Volts

SUPPLY VOLTAGE: ± 5 Volts; +5 Volts only goal

OUTPUT IMPEDANCE: 50 Ohm, nominal

SIZE: 60 x 60 mil ANACHIP

SPECIFICATIONS FOR S BAND ATTENUATOR

FET switches with on chip TTL driver

FREQUENCY:	2305 to 2497 MHz
BANDWIDTH:	> 800 MHz
INSERTION LOSS:	< 3 dB min IL (2 dB goal); steps 0, 2, 4, and 6 db
ISOLATION:	> 20 dB
POWER HANDLING:	> +10 dBm @ 1 dB compression
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	\pm 5 Volts
CONTROL:	TTL
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR 2 BIT PHASE SHIFTER

Goal: *FET switches with on chip TTL driver*

FREQUENCY:	2305 to 2497 MHz
BANDWIDTH:	> 800 MHz
INSERTION LOSS:	< 4 dB min IL (3 dB goal);
INSERTION BALANCE:	+/- 1dB min IL;
PHASE SHIFT:	steps 45 (goal), 90 and 180 degrees
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	± 5 Volts
CONTROL:	TTL (goal); or 0, -5V switch inputs
SIZE:	60 x 60 mil ANACHIP