The Johns Hopkins University
Part time Engineering Program for Professionals

525.787.91 MMIC Design
Fall 2006

MMIC VCO Design

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Abstract

This report describes the design of a MMIC VCO, meant to operate at a frequency range of 2305 to 2497 MHz, with output power higher than +7dBm, a control voltage between 0 and 0.4V and a single voltage supply of 5V. The design process used was the TQPED, offered from TriQuint and layout and simulations were done using Agilent's ADS package. The report goes through the steps required to design a VCO using the reflection method and presents simulations results that predict operation according to the design specifications. Care has been also taken to keep phase noise low.

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December 2006

1. Introduction

The MMIC VCO has been designed to be part of a duplex transceiver system meant to be used for the S-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies. A schematic of the architecture can be found in Fig. 1. More specifically, the design specifications for the VCO require that it operates between 2305 and 2497 MHz. In the transmitter part, the VCO is used to generate the carrier frequency of the transmitted signal, whereas in the receiver part it is used for demodulation. In the transmitter end the VCO drives an I/Q Vector Modulator, whereas in the receiver part an I/Q Vector Demodulator. More details about the architecture of the transceiver can be found in [1].

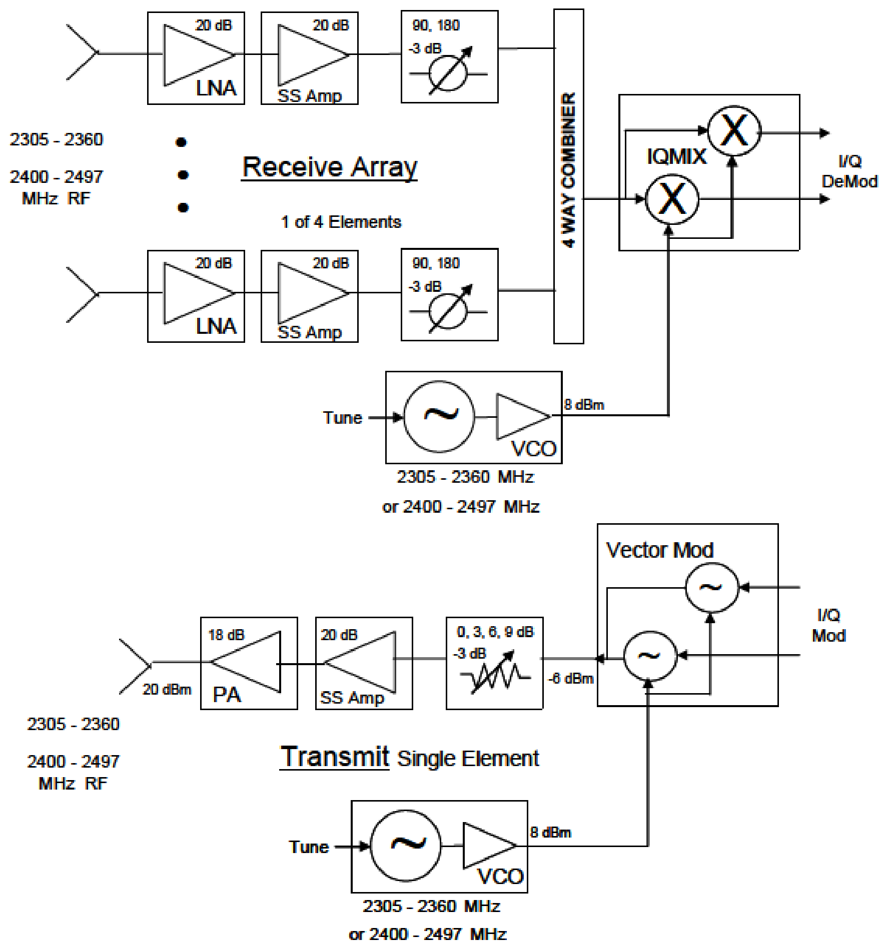

Figure 1. Architecture of the duplex transceiver system operating at WCS and ISM frequencies

Emphasis on this report is given mainly to the steps needed to design the VCO. As will be discussed in the next Section, the first step is the choice of the architecture. Then, a varactor with a widely tunable capacitance and a fairly small parasitic resistance is needed to achieve a wide frequency tuning range without deteriorating the quality factor of the resonator, parallel to which it is attached. The choice of the resonator is probably the most important part in the VCO, since it is the network that will determine the phase noise of the oscillator. Appropriate biasing is then needed to achieve the desired output power. Finally, a good output matching network is needed to provide an interface with next stages that will guarantee oscillation.

2. Design approach

Several architectures exist for designing VCOs. Based on the application and the specifications of the specific MMIC VCO, the Colpitts architecture was chosen, because of its simple design and fairly good characteristics. Moreover, the use of only one transistor in the topology was appealing in keeping the phase noise low. The Colpitts topology can be seen in Fig. 2, with two possible configurations: one with the feedback from source to gate, and the other with feedback from drain to source. Either topology can be used, however notice that the feedback needs to be positive, i.e., feedback from drain to gate will not lead to oscillations.

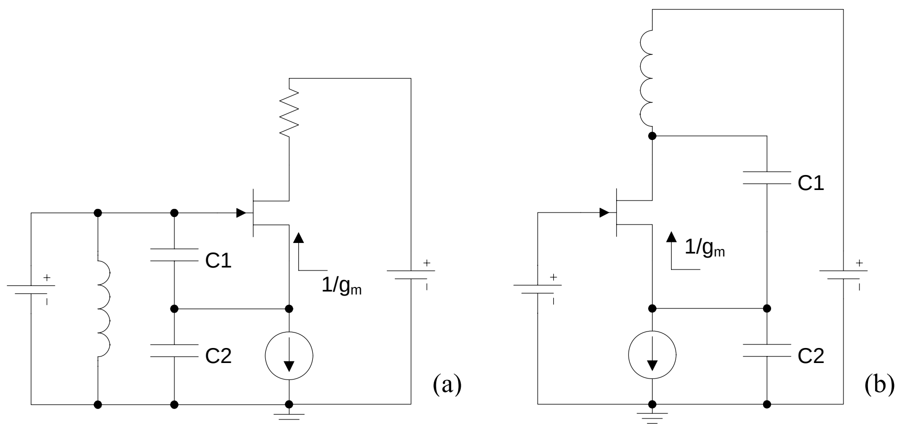

Figure 2. Basic Colpitts configurations

The FET effectively decouples the resonator from the load. In the case of feedback from source to gate the output has to be taken at the drain, whereas for drain-source feedback, the load should be connected at the gate. Since a specification of the design was to maximize the output power, the load had to be connected to the drain, and this is why the topology of Fig. 2(a) was chosen.

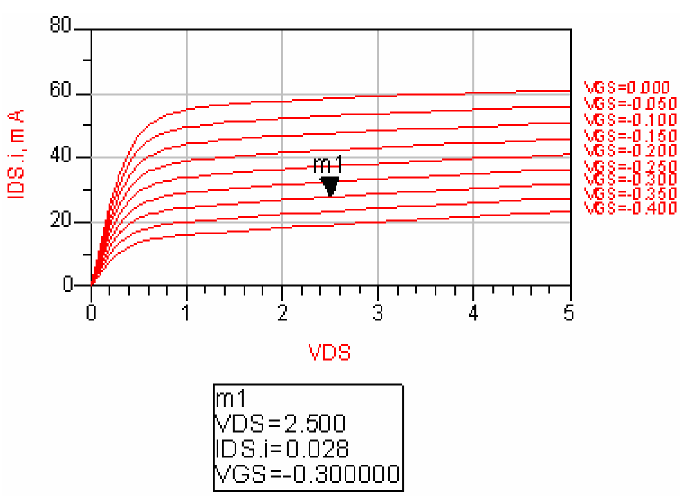

Fig.3 FET biasing

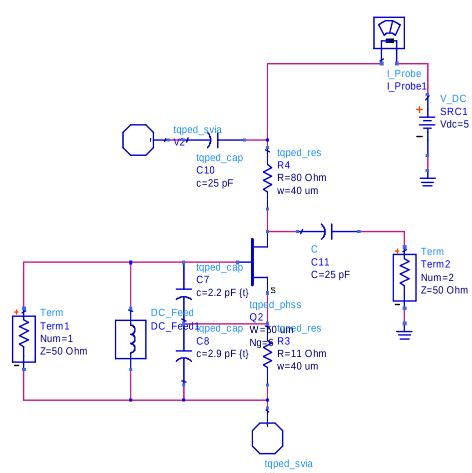

Fig. 4. Basic Colpitts topology

A D-mode pHEMT was used for the design, so as to simplify biasing; just a resistor parallel to C2 suffices. If an E-mode pHEMT were to be used, either a second voltage source would be needed, or a resistive divider at the gate had to be incorporated, increasing noise in the architecture. In order to maximize the output power while keeping noise low, the FET was chosen to operate at IDSS/2 and a VDS of 2.5 (half that of the voltage supply). In order to find the value of the resistor that had to be connected parallel to C2, a dc analysis of the FET was performed, providing the IDS vs VDS curves of the device. As shown in Fig. 3, IDSS is around 56mA (VGS=0), and for IDSS/2 and VDS=2.5V, a VGS of -0.3V is required. In order to achieve a VDS of 2.5V, an extra resistor was connected at the drain, providing the appropriate voltage drop. A schematic with the basic topology and the two biasing resistors can be seen in Fig. 4.

The inductor has not been yet added to the design and the 0V dc voltage at the gate is provided through a dc feed element. The first step in building the oscillator will be to maximize instability of the design. A figure of instability, as described in [2], is the farthest point of the output mapping circle, called MaxMP2, which is equal to μ', the load stability factor. The output mapping circle basically shows the maximum degree of instability in the circuit, assuming that an appropriate load (the load that maximizes instability) has been connected to the input port. Therefore, the first step in the design is to tune capacitors C1 and C2, so as to achieve a maximum value at the output mapping circle, for the center frequency of 2.4GHz. The initial values of these capacitors were chosen such as to provide oscillations at 2.4GHz when connected to an inductor of value around 3-4nH. Note also that the equivalent capacitance connected to the inductor is the series combination of C1 and C2.

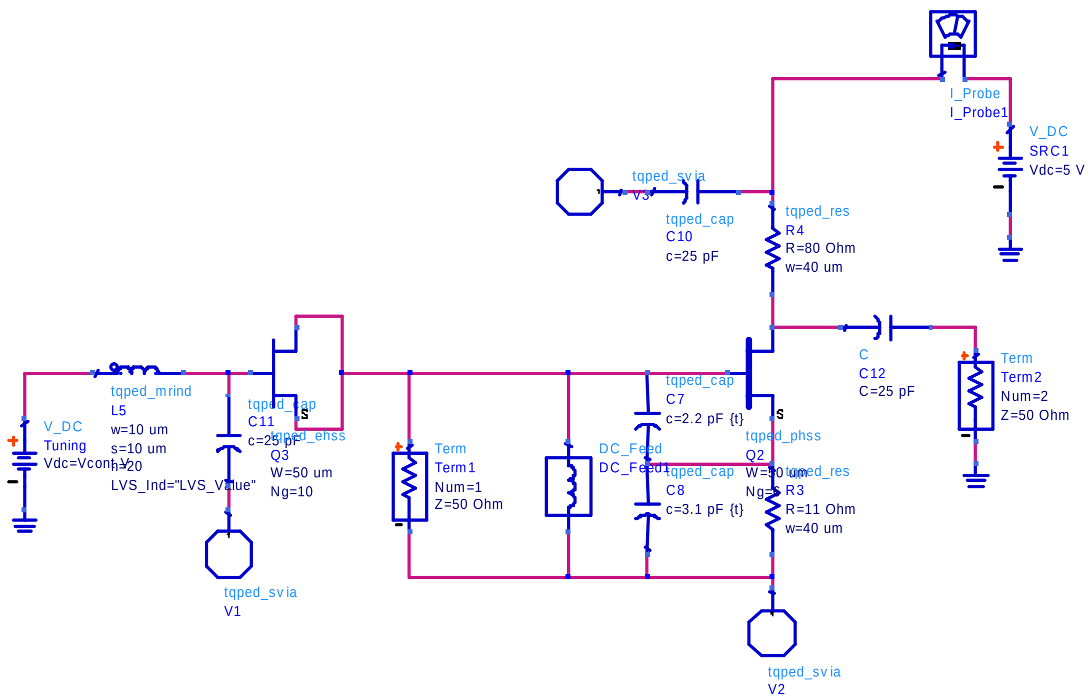

Fig. 5. Schematic with the varactor added

Next step was to add the varactor to the design, as shown in Fig. 5. The varactor had to be implemented on chip and therefore a diode connected pHEMT, reversely biased was used. As known, diodes operate as variable capacitors when reversely biased. The capacitance is nonlinearly controlled by the bias voltage. Objective here was to find an appropriate device that would have a small capacitance so that the final oscillation frequency does not divert considerably for the center frequency of 2.4GHz, but also with as low as possible losses. Ideally, the tuning voltage range has to be large, so that a small variation in the voltage does not result to a big variation in capacitance. Several devices were simulated, however, the one with the better response was found to be the E-mode pHEMT with 10 fingers of 50μm each (Fig. 6). The response of this device is shown in Fig. 7 for a frequency range of 0.5 to 2.4GHz and for a bias of 0V, along with the response of its equivalent model, that of an RC network. As can be seen from Fig. 6, the losses are fairly small. Simulations at different voltage biases (up to -1V) demonstrated even smaller losses.

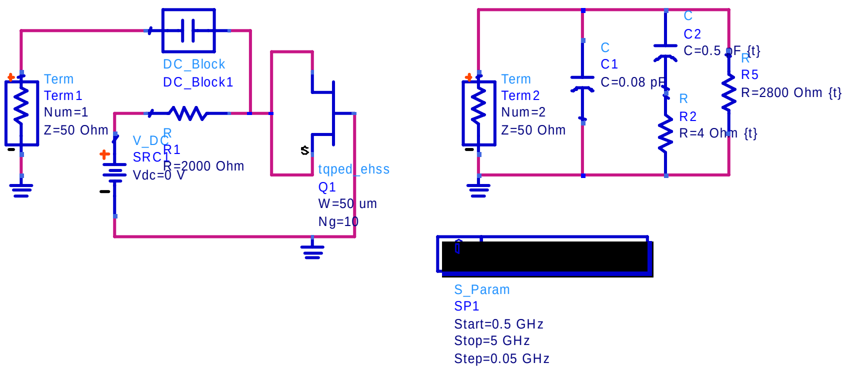

Fig. 6. E-mode varactor and equivalent model

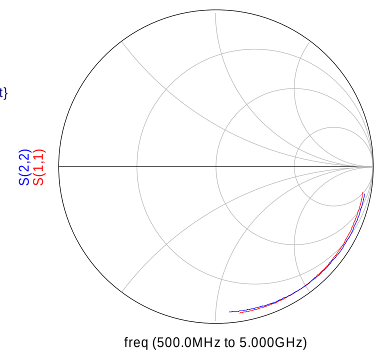

Fig. 7. Varactor frequency response

The varactor was placed parallel to the C1-C2 network and tuning of C1-C2 was done so as to achieve a maximum value for MaxMP2. The bias of the varactor was set at 0.24V (note that the varactor has been connected in a way inverse to that of Fig. 6 and that is why positive voltages are used), which was the bias at which we would like to have our center frequency. It should also be noted that the bias voltage at the gate of the varactor was applied through a big inductor instead of a resistor. This was done so as to reduce the noise introduce by the bias feed network.

Then, the inductor was added to the design in place of the dc feed (Fig. 8). The choice of the type of resonator is very important when designing a VCO, since it is the main part that affects phase noise [3-5]. Crystals and ceramic resonators have excellent phase noise; however these are devices that need to be added externally to the MMIC and therefore could not be used. For on chip implementation, two basic topologies were considered. One was the only-C network, basically a gyrator with a capacitance on one end, seen as an inductance on the other end, and connected in parallel to a capacitor, and the simple LC tank. The only-C network although smaller in size and very common in CMOS design, has the drawback of high phase noise. This is the main reason that the simple LC tank was finally implemented.

The topology was simulated as a one port element, and tuning of the C1-C2 capacitors and the inductor was performed so as to achieve the highest S11 at a frequency of 2.4GHz. Assuming a purely resistive load at the drain, we would like S11 to be purely real. This can be done by adding an output matching network at the drain that will rotate S11 to a real value. In general, oscillations will start at the point where the imaginary parts of the drain impedance and the load impedance are opposite and the real part of the negative drain impedance is absolutely greater than that of the real part of the load impedance. For our design, we chose not to add the extra matching network, knowing that oscillations will start at a frequency slightly different than where S11 has its maximum value.

Having designed the resonator part of the oscillator, we have to consider the values of its negative impedance and determine the output matching network so as to guarantee that when a 50Ω load is connected, oscillations will start and will be sustained. The output matching network was the equivalent T of a λ/4 transmission line, that would transform the 50Ω load to a lower impedance at the drain of the FET. Usually, the negative resistance needs to be at least 3 times larger than that of the load. For this case the matching network shown in Fig. 9 was employed and tuning of the L and C values was done until the condition for oscillation was met.

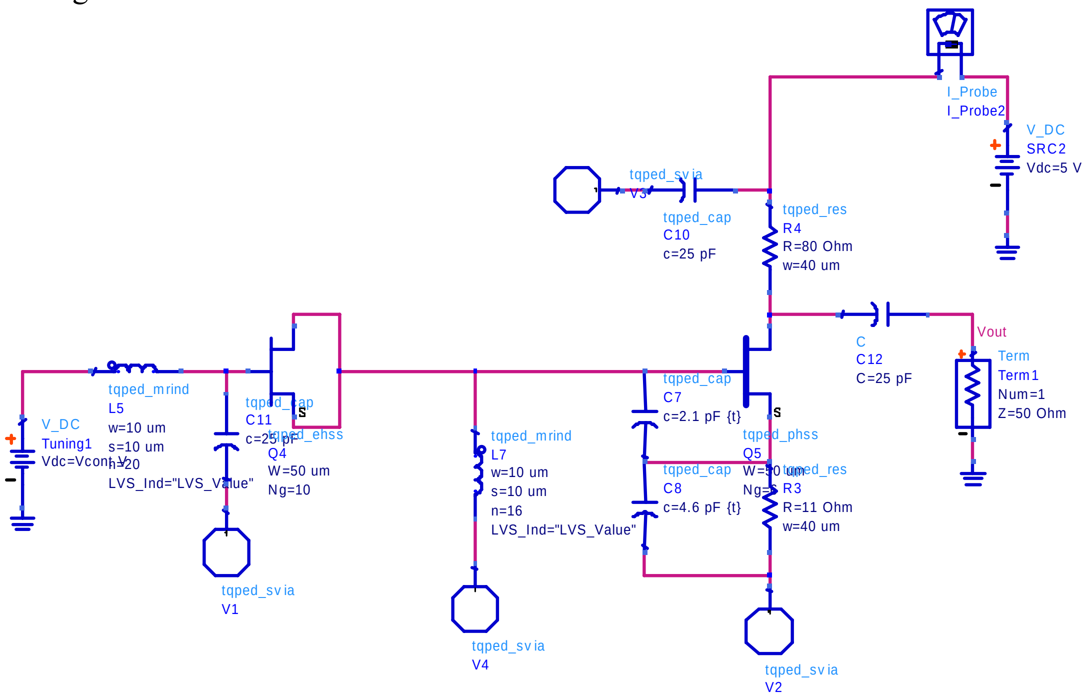

Fig. 8. Topology with the dc feed replaced by an inductor

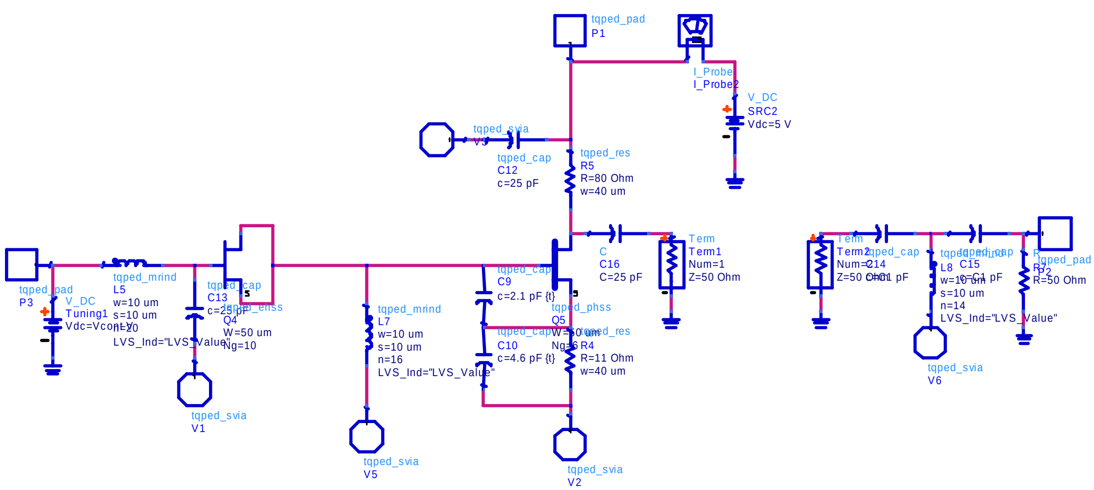

Fig. 9. Topology with output matching network

3. Simulation Results

Simulation results from several steps of the VCO design, as well as of the whole topology are provided in this section. Maximization of the output mapping circle for the frequency of 2.4GHz is shown in Fig. 10, after appropriate tuning of the values of capacitors C1 and C2, for the schematic of Fig. 5. Fig. 11 shows maximization of the value of S11 after adding the inductor to the design (Fig. 8).

In order to check that oscillations will start, at several frequencies, the schematic of Fig. 9 was simulated for different values of the biasing voltage of the varactor. Using the notation of Fig. 9 for the numbering of the ports, the objective here was that for the frequencies where imag(Z1+Z2)=0, real(Z1+Z2) had to be negative. This means that at the frequencies where the reactive part of the impedance of the load is cancelled from the impedance of the FET network, the overall resistance is negative and voltage starts to build up.

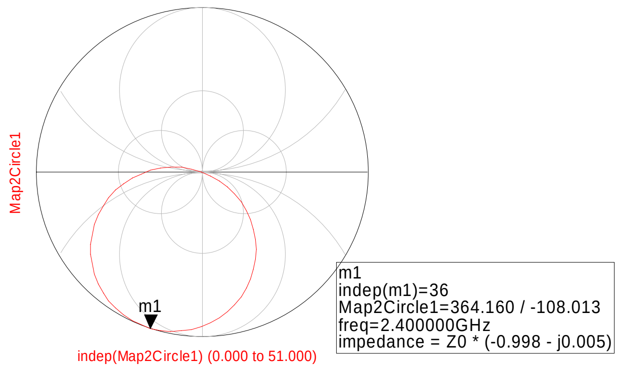

Fig. 10. Maximizing MaxMP2

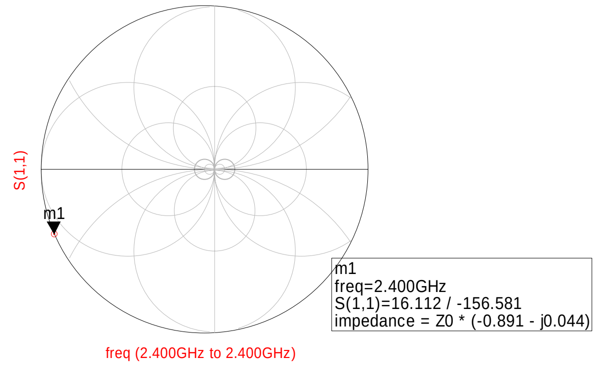

Fig. 11. Maximizing output reflection coefficient

Fig. 12(a) shows simulation results for a varactor biasing voltage of 0.28V. The sum of the imaginary parts is 0 close to 2.4GHz and at that frequency the sum of the real parts is negative; therefore, oscillations will start and will be sustained close to that frequency. Fig. 12(b) depicts simulation results for the case of a varactor biasing voltage of 0.4V and indicates that simulations will start around 2.24GHz. Finally, Fig. 12(c) corresponds to a biasing voltage of 0V and indicates oscillations around 2.56GHz. Note that in all these plots, the sum of the imaginary parts becomes zero only at one point in the range between 0.5 and 5GHz. In Fig. 12(c), the sum of the imaginary parts is very close to 0 also at 1.8GHz. However, even if it crossed the 0 point, oscillations would not start since the sum of the real parts at that point is positive.

Simulations, so far, have been performed using the nonlinear simulator built-in ADS. Another set of simulations was performed using the Harmonic Balance Simulator of ADS. The concept in that simulator is slightly different than the non-linear one. Here, oscillation at an unknown frequency ω is assumed and the nonlinear parts of the design are represented by their describing functions [6]. An `osc-port` element is introduced at some point of the closed loop and the solver finds the point at which the total phase of the loop is 360^{o} and checks if the gain is positive. If it's not, then no oscillations are sustained; if it is, then we have oscillations and the solver can provide estimates of the output power, harmonics, output waveforms, phase noise and other desired values.

An interesting point when using the Harmonic Balance solver is that the result for the oscillating frequency was different than that gotten from the nonlinear simulator. This can be due to several reasons. The first and probably the most possible is that the nonlinear simulator finds the frequency at which oscillations will start. However, the actual frequency where oscillations will be sustained is slightly different. The second reason is that in harmonic balance simulation there are several assumptions made in order to derive the describing functions, and this might hide phenomena that the nonlinear simulator is taking into account. Testing of the actual MMIC might help reveal which approach is more correct.

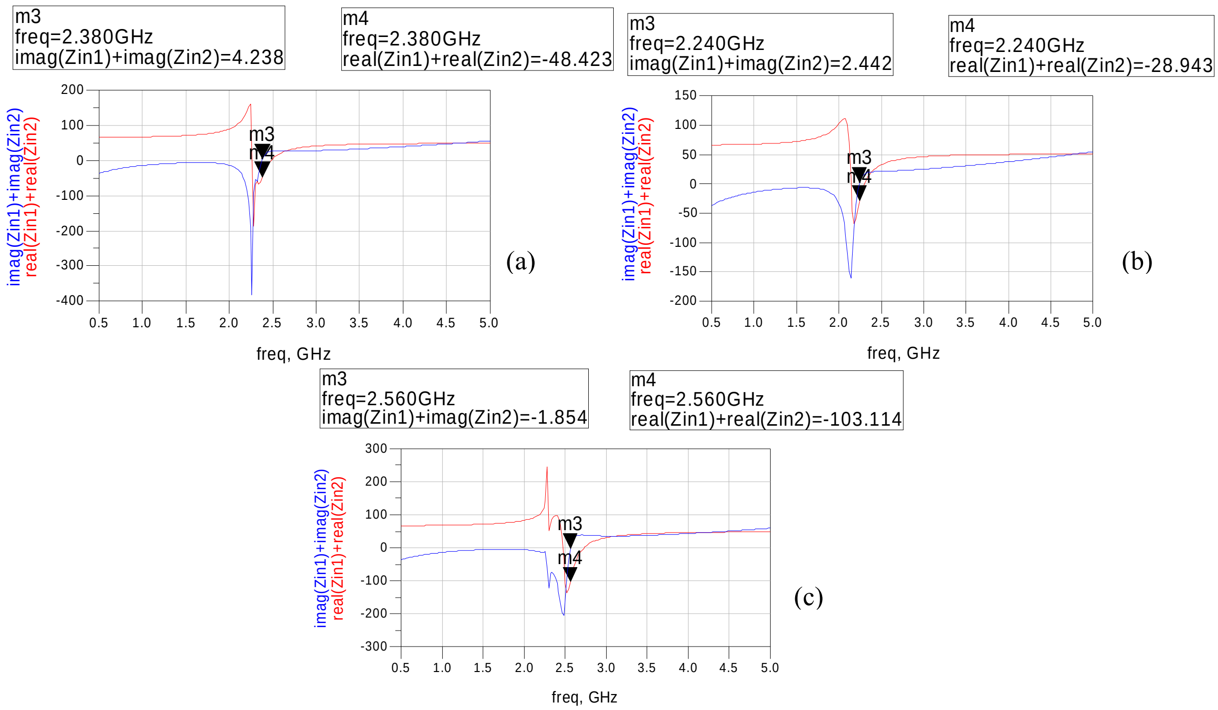

Fig. 12. Simulation results using the nonlinear solver for varactor biasing voltages of (a) 0.28V, (b) 0.4V and (c) 0V

Fig. 13(a)-(c) depicts simulation results using the harmonic balance simulator. Frequencies are shifted down by 200MHz compared to the non-linear simulator. Output power is always greater than 7dBm and for several biases greater than even 10dBm. Phase noise is also good, being less than -110dBc at 1MHz for all oscillating frequencies.

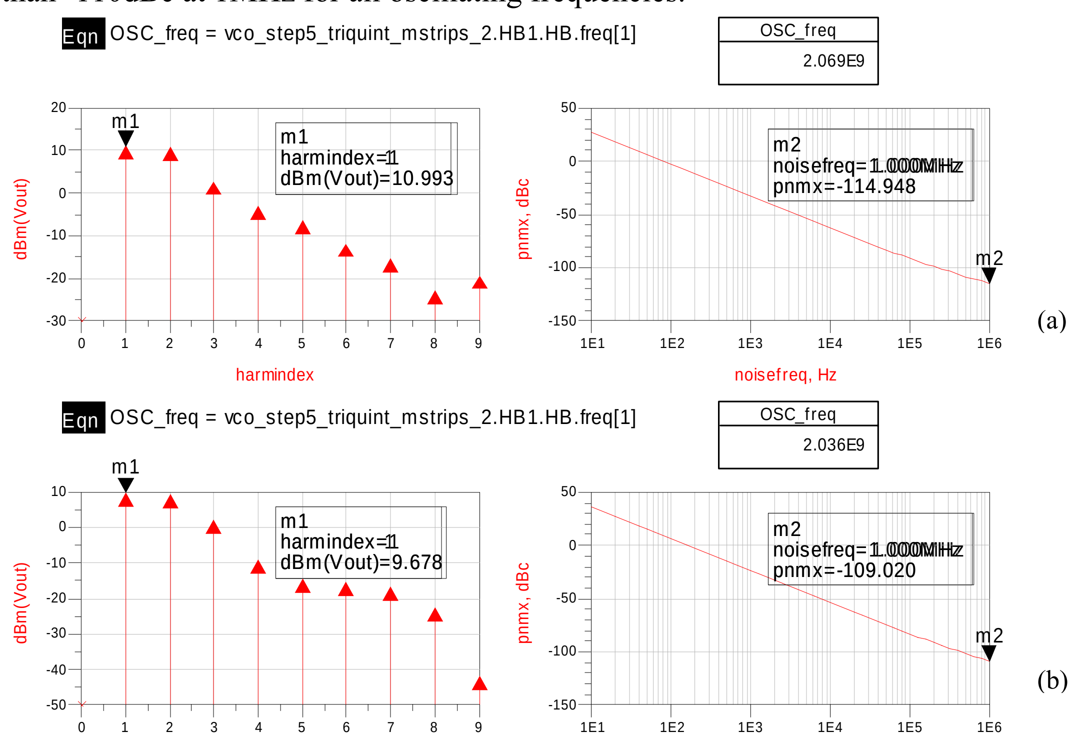

Fig. 13. Simulation results using the harmonic balance solver for varactor biasing voltages of (a) 0.28V and (b) 0.4V

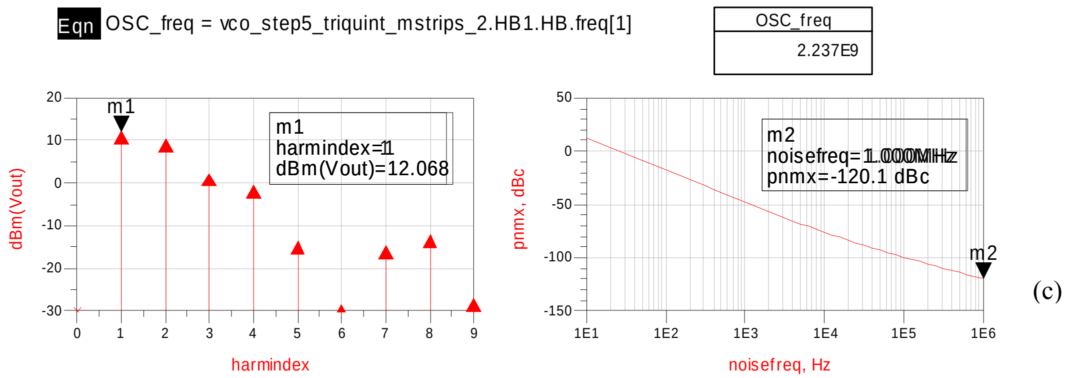

Fig. 13. Simulation results using the harmonic balance solver for varactor biasing voltage of (c) 0V

4. Schematic and Layout

The total schematic, without the `tlines` representing the interconnects, is shown in Fig. 14. The dc solution has been annotated.

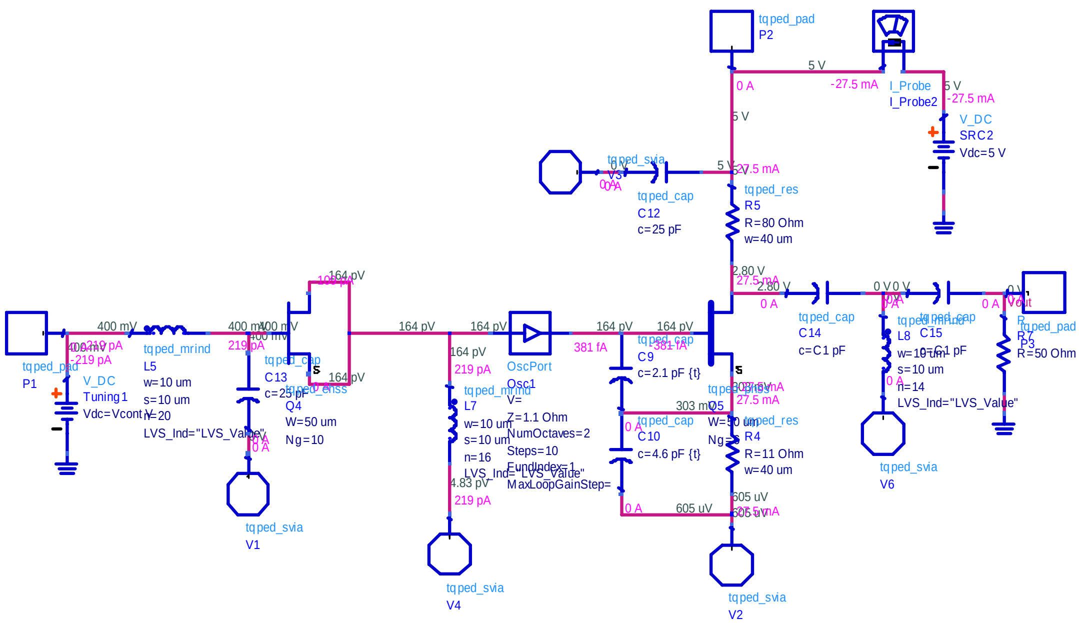

Fig. 14. Overall schematic

The layout of the circuit is shown in Fig. 15. DRC and LVS checks were performed and passed.

5. Test Plan

For testing, 2 DC probes and 1 RF probe are needed. Place, a DC probe to the terminal labeled "+5V" and apply 5V of voltage. Place a second DC probe to the terminal labeled "Vtune", and apply a voltage ranging from 0V to 0.4V. Connect an RF probe (GSG) to the terminal labeled "out" (output of the oscillator) and measure the signal on a Spectrum Analyzer. Once the center frequency has been found, limit the span to 5-10MHz and measure the power at the fundamental frequency as well as phase noise. Preset the instrument to its default settings, find the harmonics and measure the power of the 2nd and 3rd one. Fill out the table below:

V_{tune} (V)	f_o (GHz)	Power @ f_o (dBm)	Power @ $2f_o$ (dBm)	Power @ $3f_o$ (dBm)	Phase noise @ 100kHz (dBc)	Phase noise @ 1MHz (dBc)

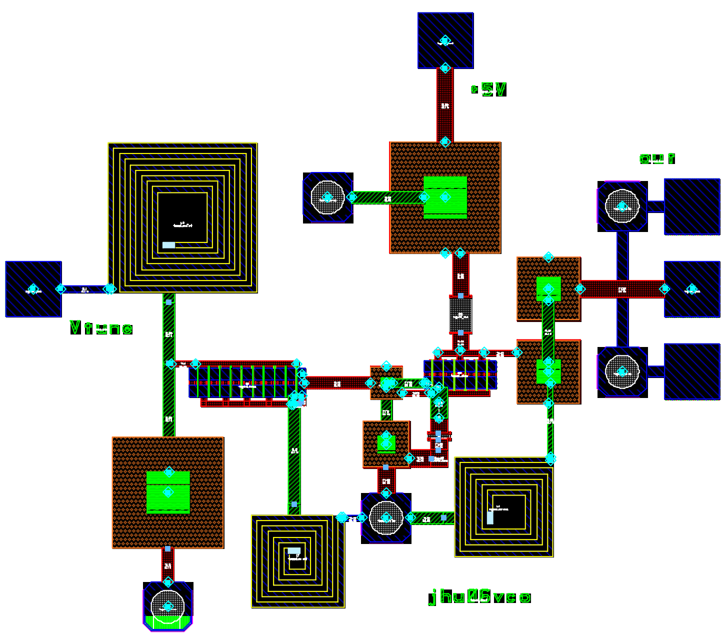

Fig. 15. Layout of the VCO

6. Conclusion

A MMIC VCO has been designed using the reflection method. The steps towards designing the VCO have been outlined starting from the architecture, then the choice of the resonator and varactor and finally the output matching network. Simulations have been performed both with the nonlinear simulator and the harmonic balance one. Differences in the results have been found and possible reasons for that have been provided. The final schematic and layout have been demonstrated as well as a plan for future testing. Testing will be critical in determining the actual oscillation frequency as well as output power and noise figure, and check the how well these figures compare to the simulation results.

References

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