Two Bit Phase Shifter

JHU MMIC Project

EE525.787 FALL 2006

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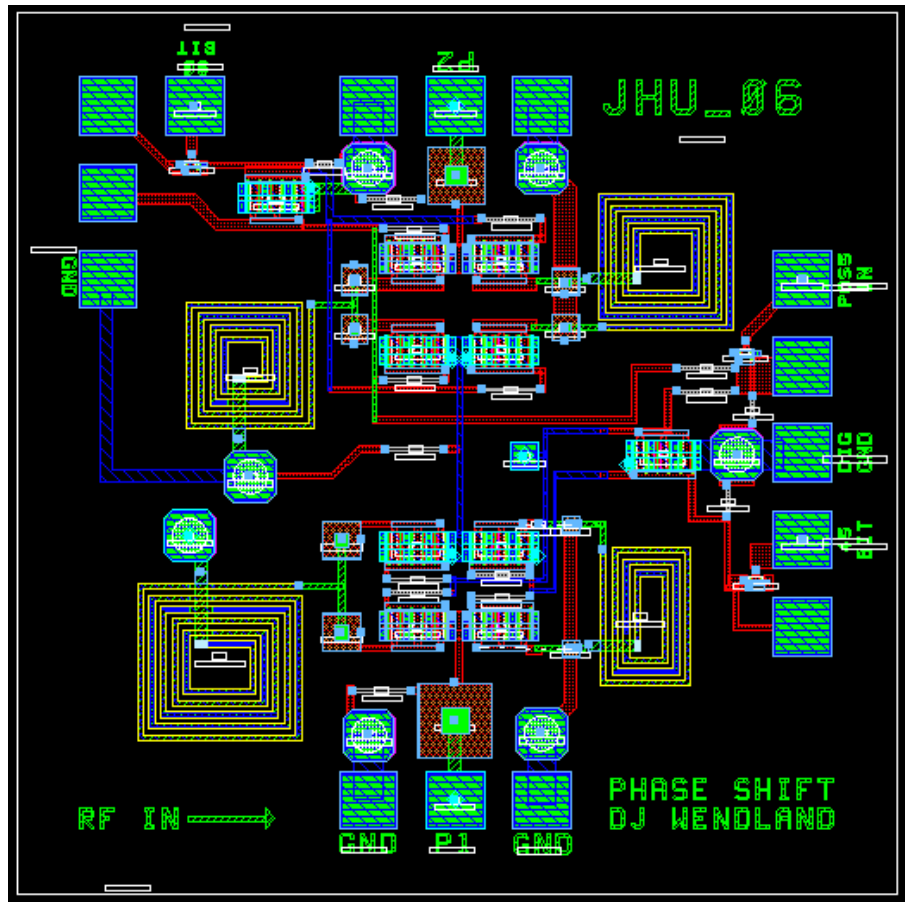
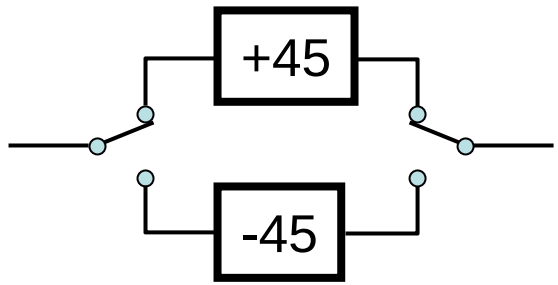
Introduction

- A MMIC two bit phase shifter was designed, simulated and laid out on a 60 mil x60 mil GaAs substrate.
- The circuit will be fabricated by TriQint.

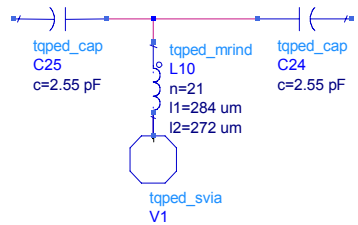


Design Philosophy

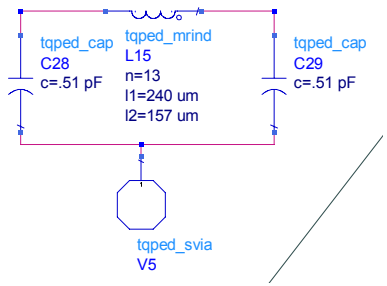
- The topology of the design was set such that there was a relative phase shift through the net work when compared to the zero or though path. The phase shifter consist of three sections.
  - Control
  - 90 degree shift
  - 180 degree shift
- The control section consist of circuitry to convert positive 5 volt control voltage to the appropriate voltages to the phase switches.
- The 90 and 180 degree shift secitions are the same except for the amount of phase shift provided by each section.
- Each phase shift section consists of a positive phase network and a negative phase network.
- The through path passes through the positive phase network of each sectin.
- Lets walk though the 90 degree phase section.
- The 90 degree phase shift section consists of a positive 45 deg. phase shift network and a negative 45 deg. phase shift network. If the through path is set through the positive phase shift network. There will be a 90 degree relative phase when the path switches, from the +45 degree network to the -45 degree network.
- With the above described topology, the phase of the through path is arbitrary and is not important for the relative phase shift.
- The 180 degree phase shift is achieved the same way but using +/-90degree networks



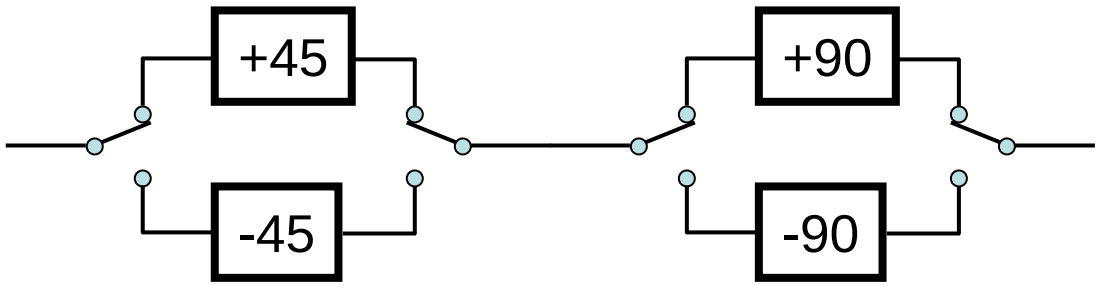
+ 45 Degree Network

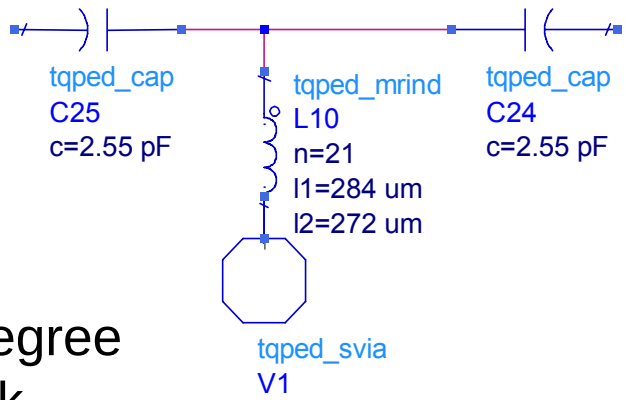


-45 Degree Network

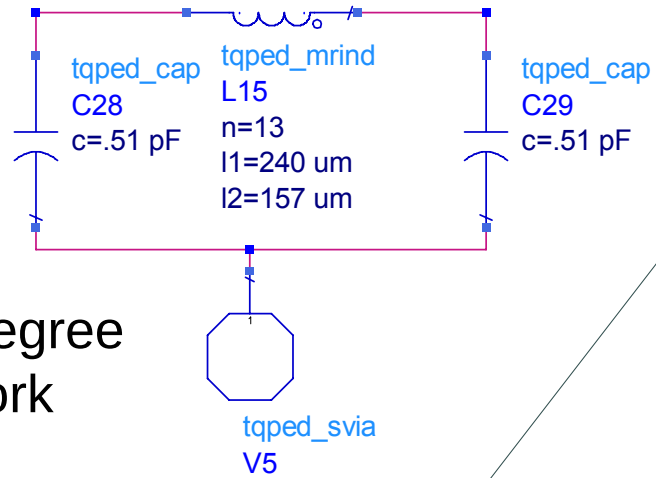


Design Philosophy





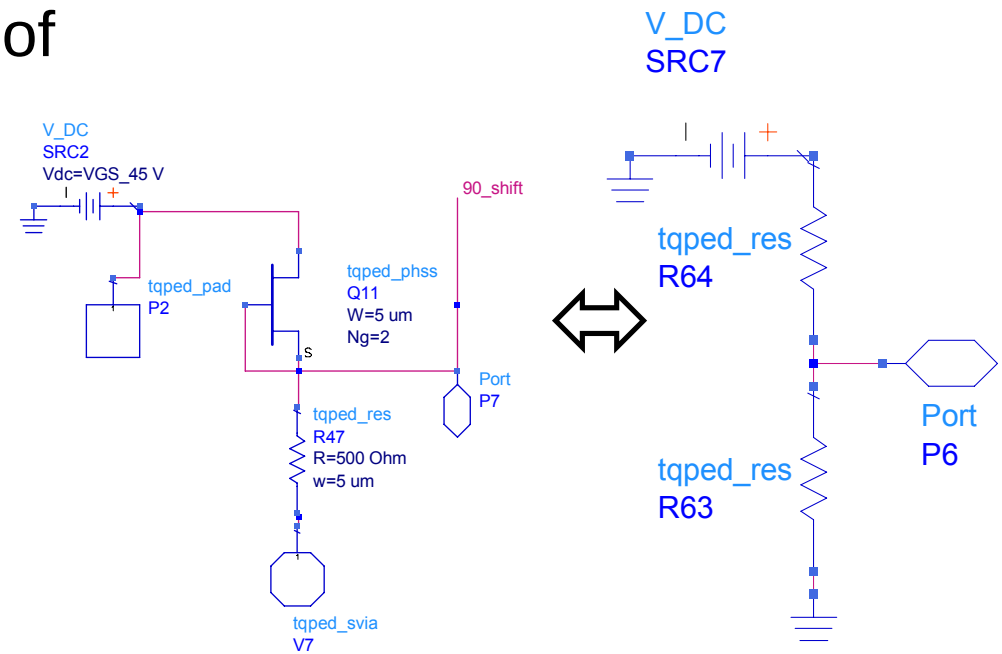
+ 45 Degree Network



-45 Degree Network

Design Philosophy

- Emode transistor were used to take advantage of the positive gate bias
  - Can use single positive supply
- Dmode transistor were used to convert +5V to the desired gate voltage
  - Smaller than resistors
  - Save space in voltage dividers.
  - FET sized to provide:
    - 2mA for 45/90 bit
    - 4mA for +5V bias



Dmode FET in voltage divider

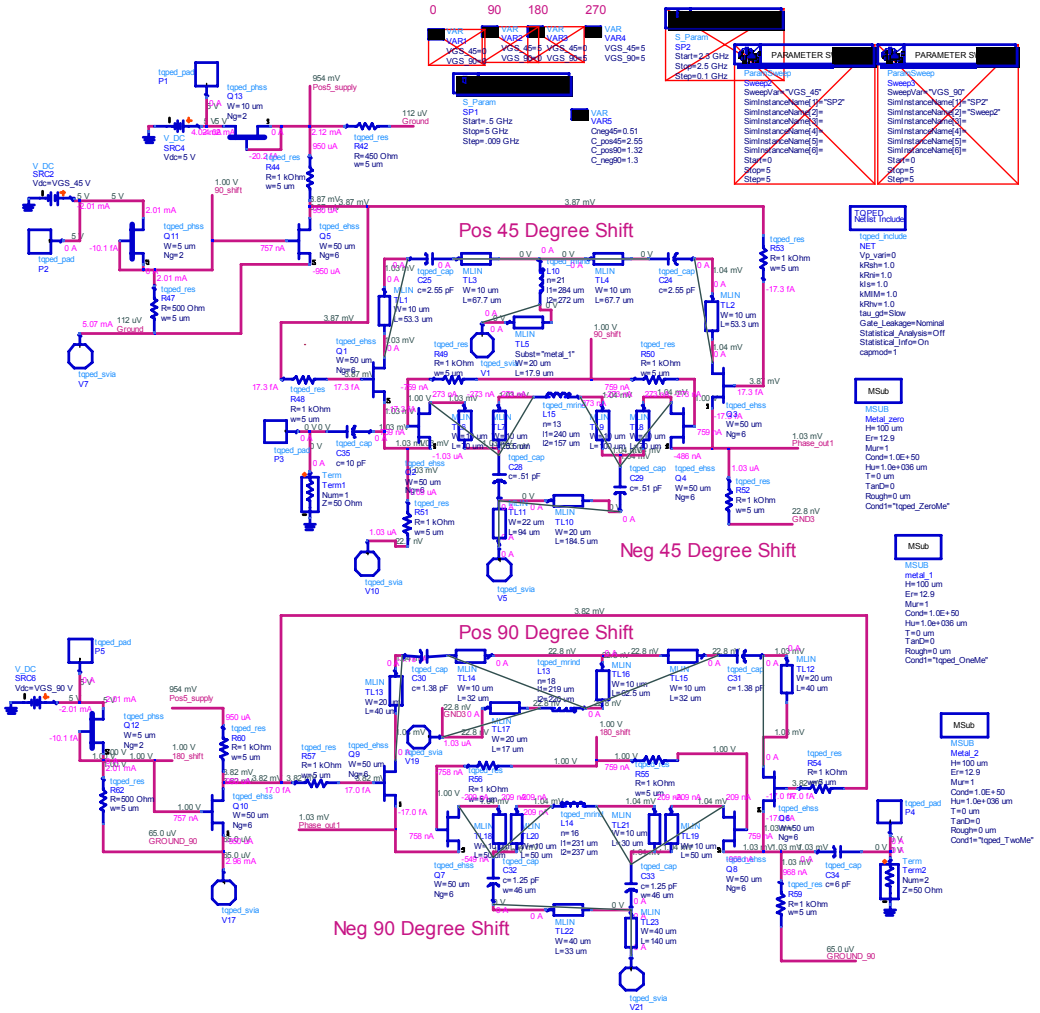
Logic Table

Phase Shift	Bit 45	Bit 90
0	0	0
90	5	0
180	0	5
270	5	5

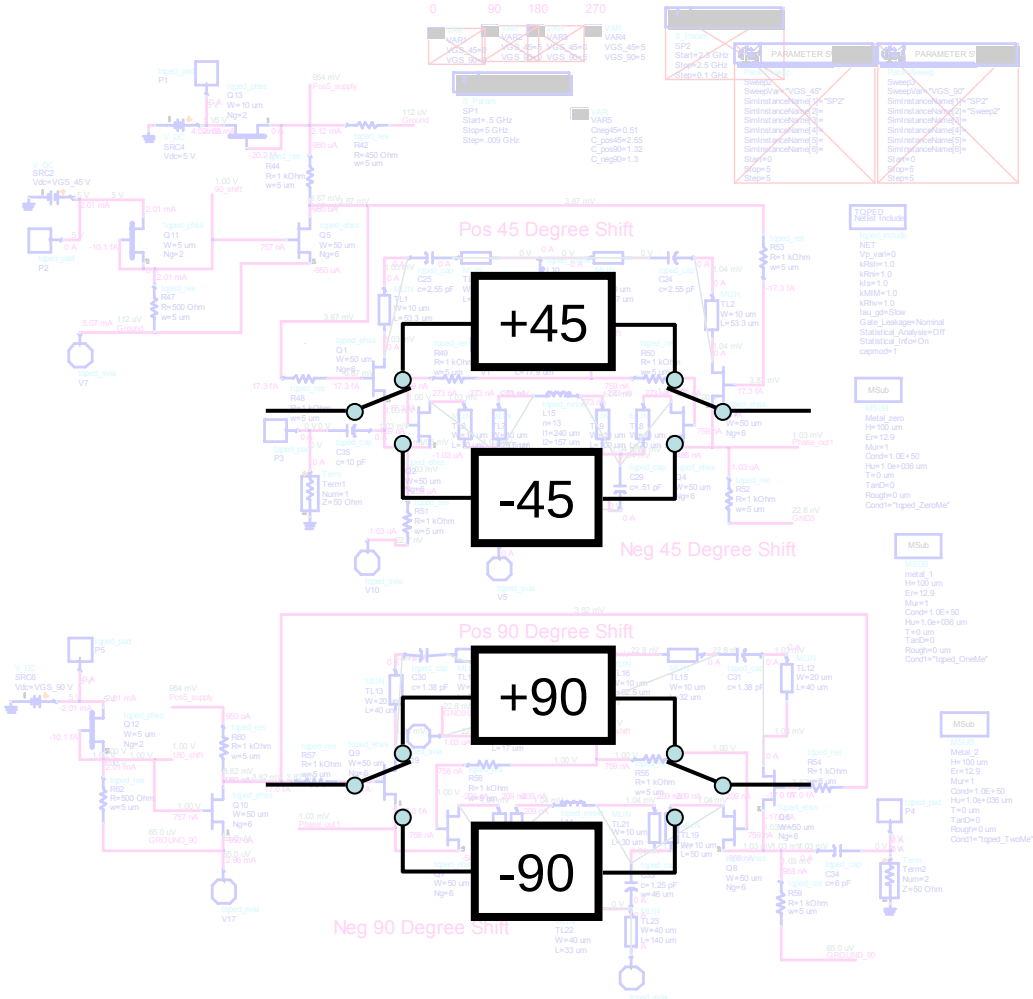
Simulation/Layout

- The phase shifter was first developed with ideal components
- TriQuint components were then substituted and retuned
- The components were then inserted into the layout, positioned and interconnects added
- The interconnects of the critical paths were simulated using microstrip elements in the schematic.
- Critical interconnects consist of:
  - Connections between switches, capacitors and inductors of the phase shift elements.
- Interconnect between the 90 degree phase shift section, 180 degree section and pads were not simulated since those paths do not affect the relative phase shift.

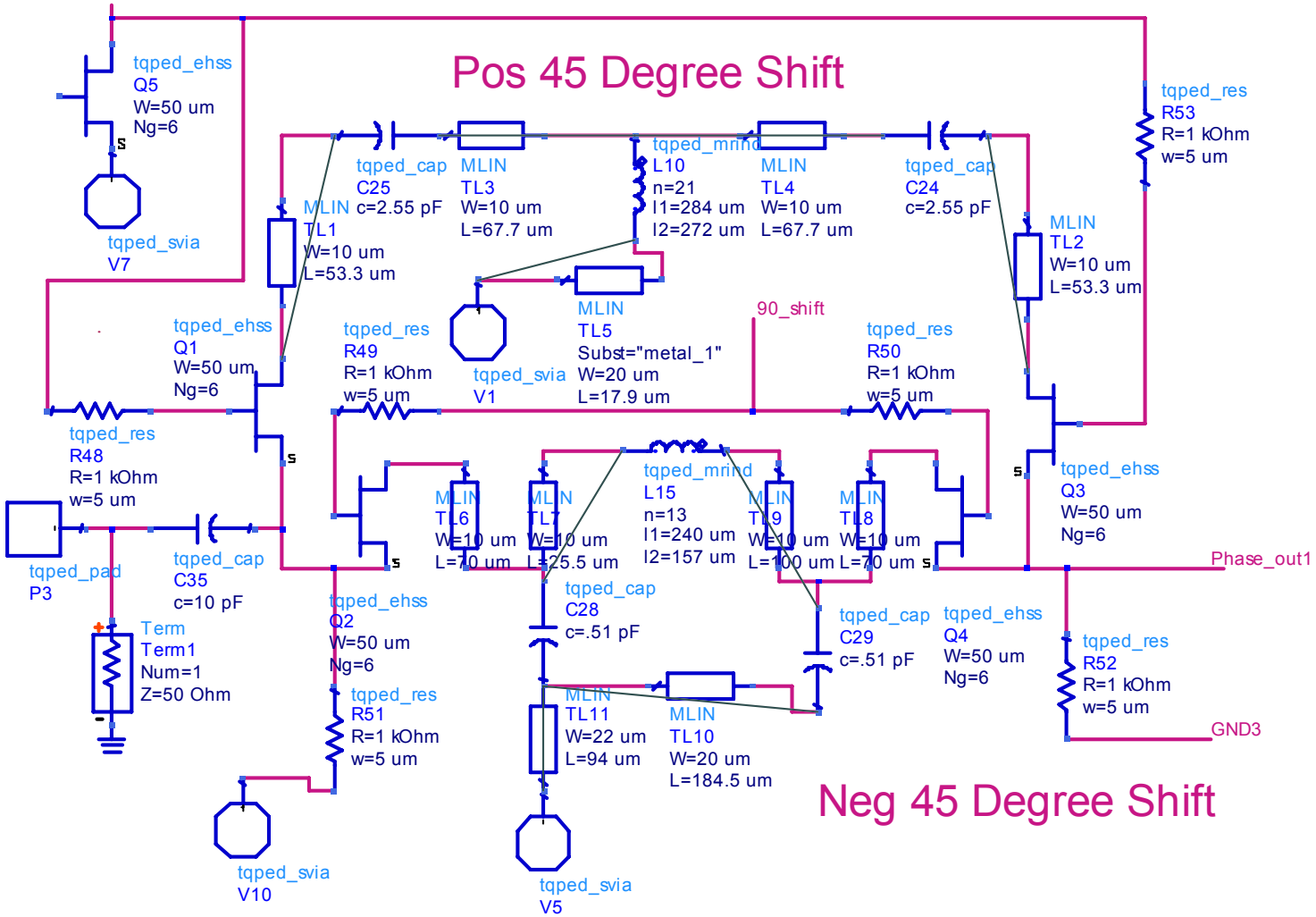
Two Bit Phase Shifter Schematic with Interconnects



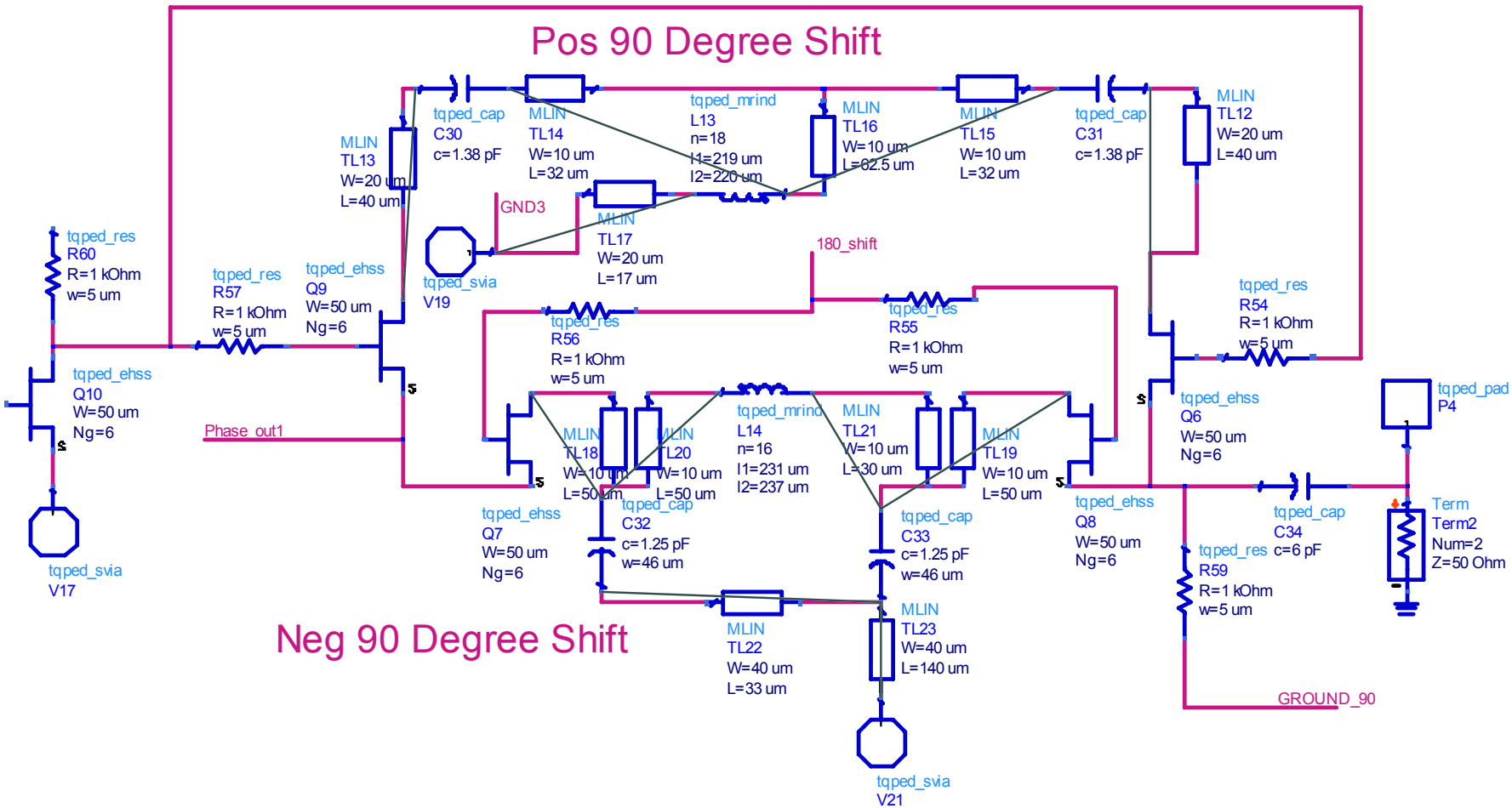
Two Bit Phase Shifter



90 Degree Phase Shift

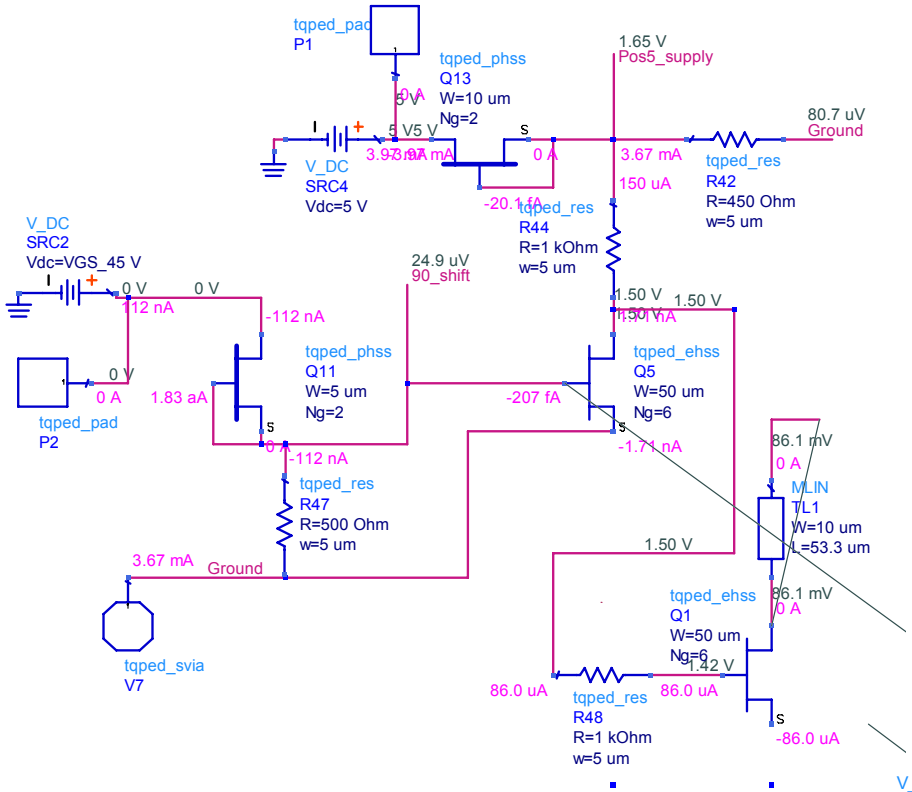


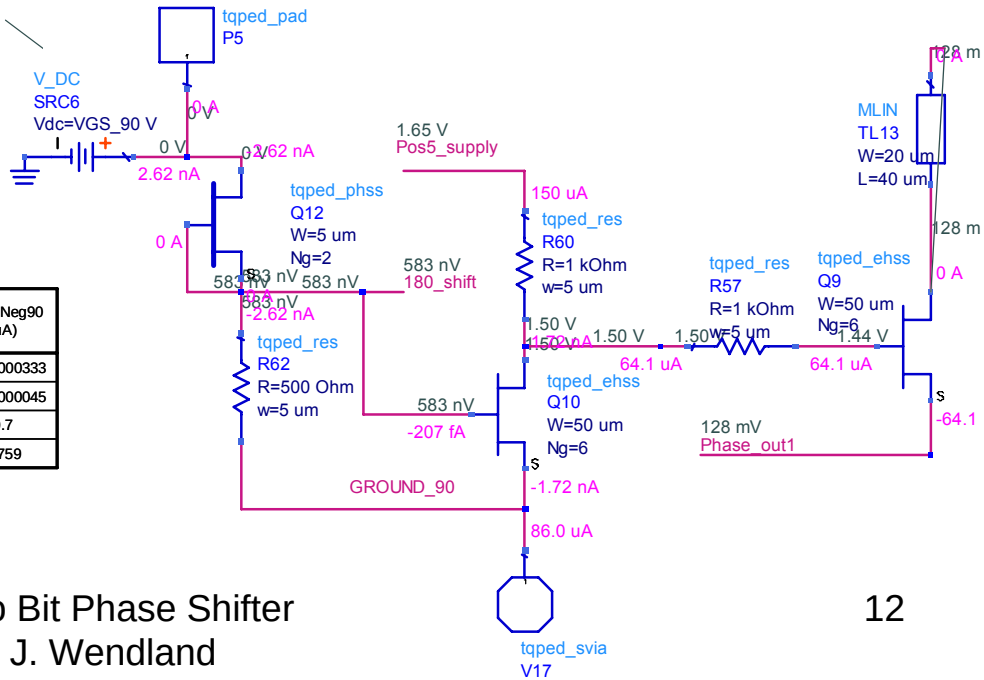
180 Degree Phase Shift



DC Switch Bias

Zero Degrees/Ref

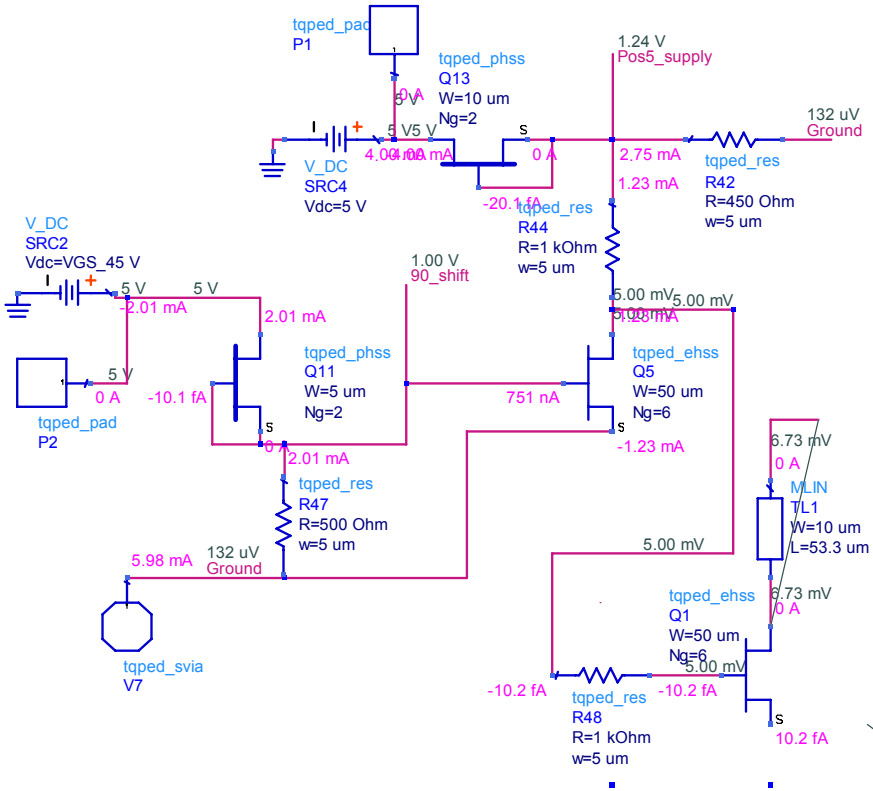


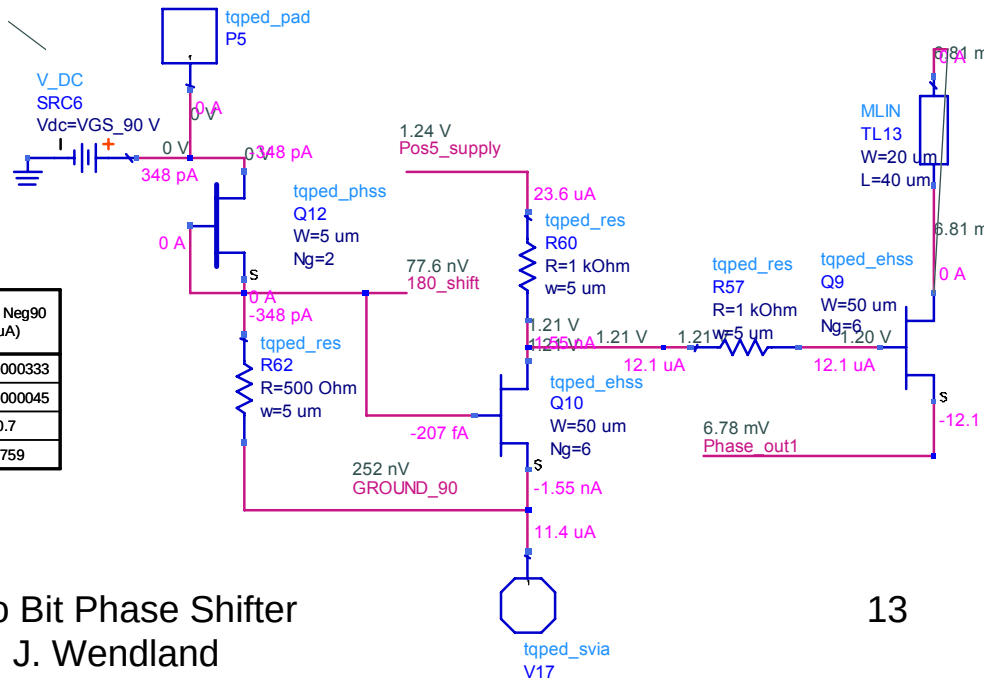


Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90(V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
0	0	0	1.42	2.50E-05	1.44	5.8E-07	86	0.000000306	64	0.000000333
90	5	0	0.005	1	1.2	7.8E-08	0.00000001	0.7	12	0.000000045
180	0	5	1.2	1.90E-05	0.005	1	11	0.000000045	0.000000011	0.7
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

DC Switch Bias

90 Degrees

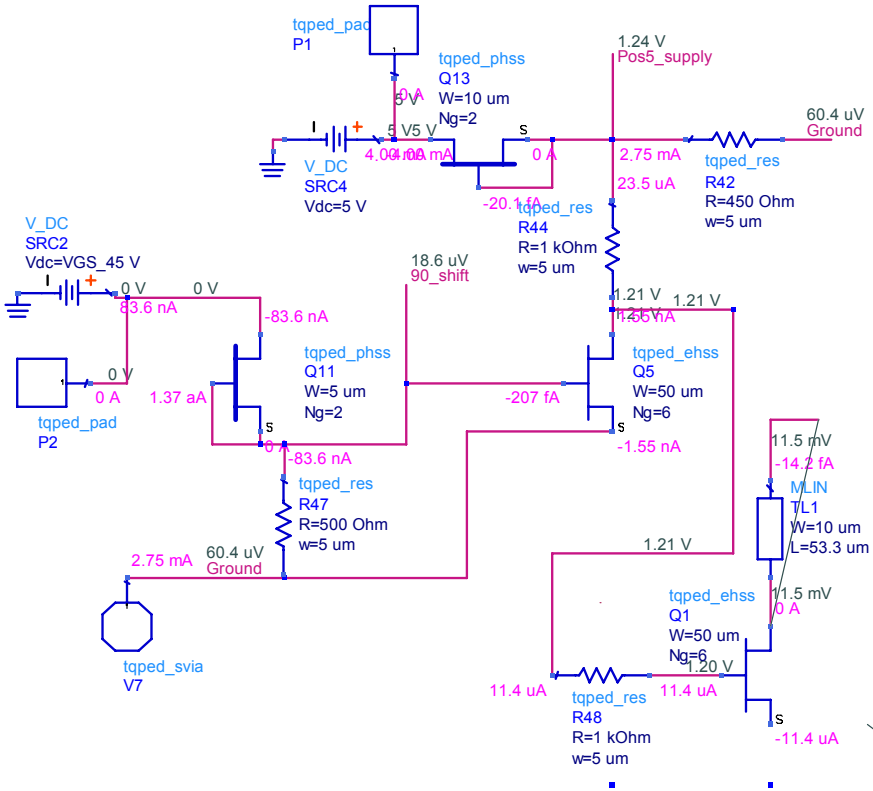


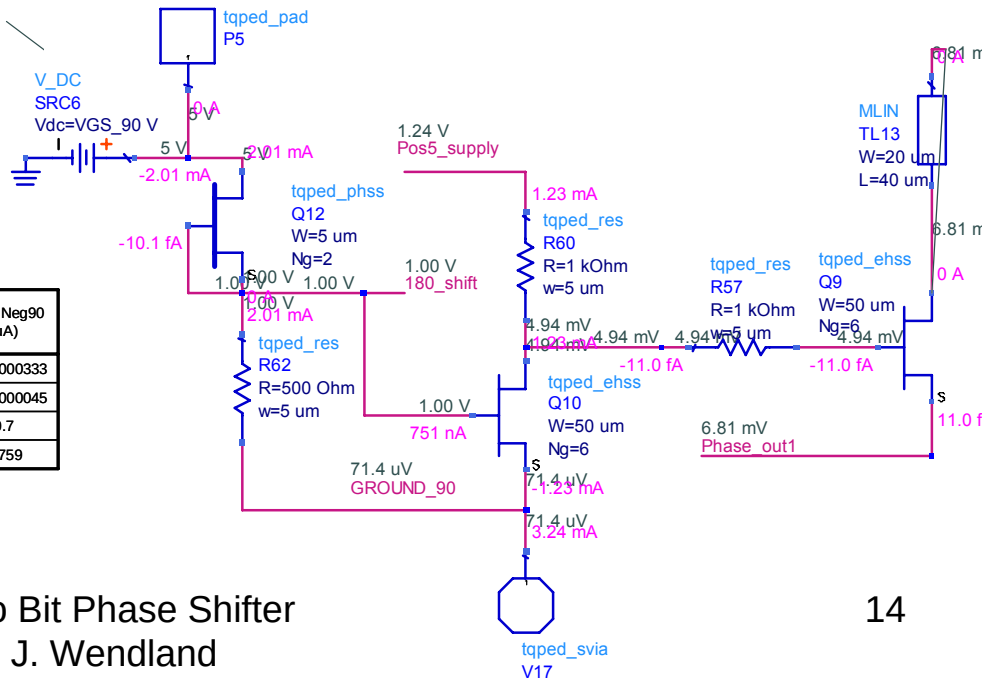


Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90(V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
0	0	0	1.42	2.50E-05	1.44	5.8E-07	86	0.000000306	64	0.000000333
90	5	0	0.005	1	1.2	7.8E-08	0.00000001	0.7	12	0.000000045
180	0	5	1.2	1.90E-05	0.005	1	11	0.000000045	0.000000011	0.7
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

DC Switch Bias

180 Degrees

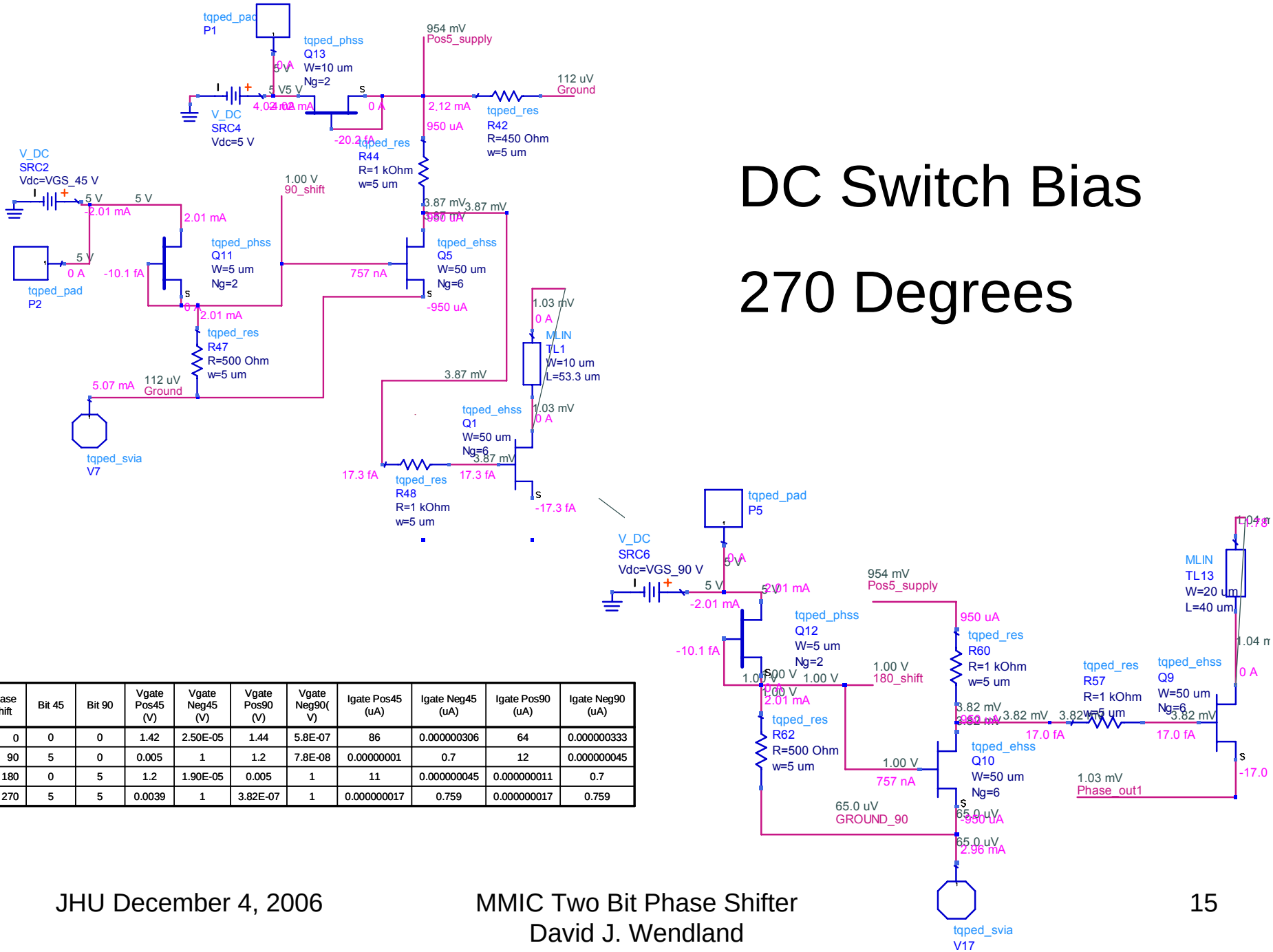




Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90(V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
0	0	0	1.42	2.50E-05	1.44	5.8E-07	86	0.000000306	64	0.000000333
90	5	0	0.005	1	1.2	7.8E-08	0.00000001	0.7	12	0.000000045
180	0	5	1.2	1.90E-05	0.005	1	11	0.000000045	0.000000011	0.7
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

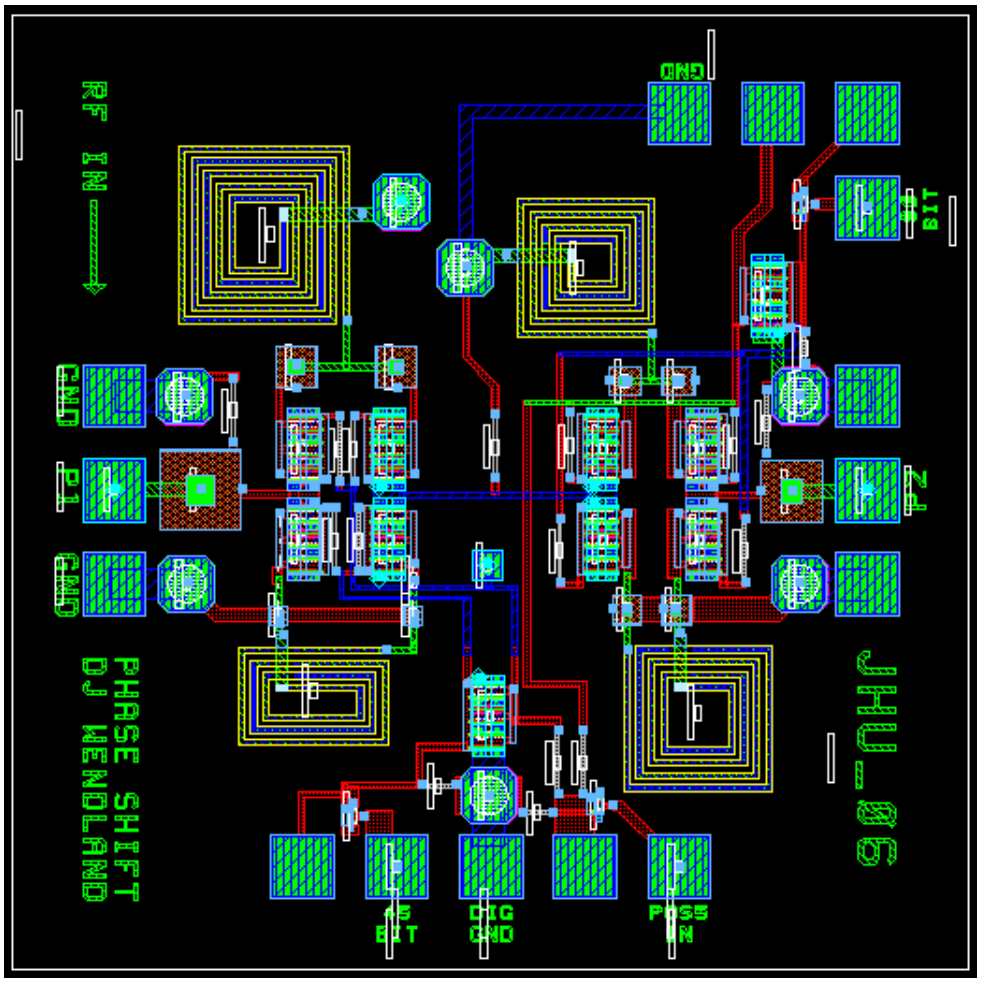
DC Switch Bias

270 Degrees



Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90(V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
0	0	0	1.42	2.50E-05	1.44	5.8E-07	86	0.000000306	64	0.000000333
90	5	0	0.005	1	1.2	7.8E-08	0.00000001	0.7	12	0.000000045
180	0	5	1.2	1.90E-05	0.005	1	11	0.000000045	0.000000011	0.7
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

Two Bit Phase Shifter Layout on 60mil x 60 mil GaAs Substrate



Design Specification

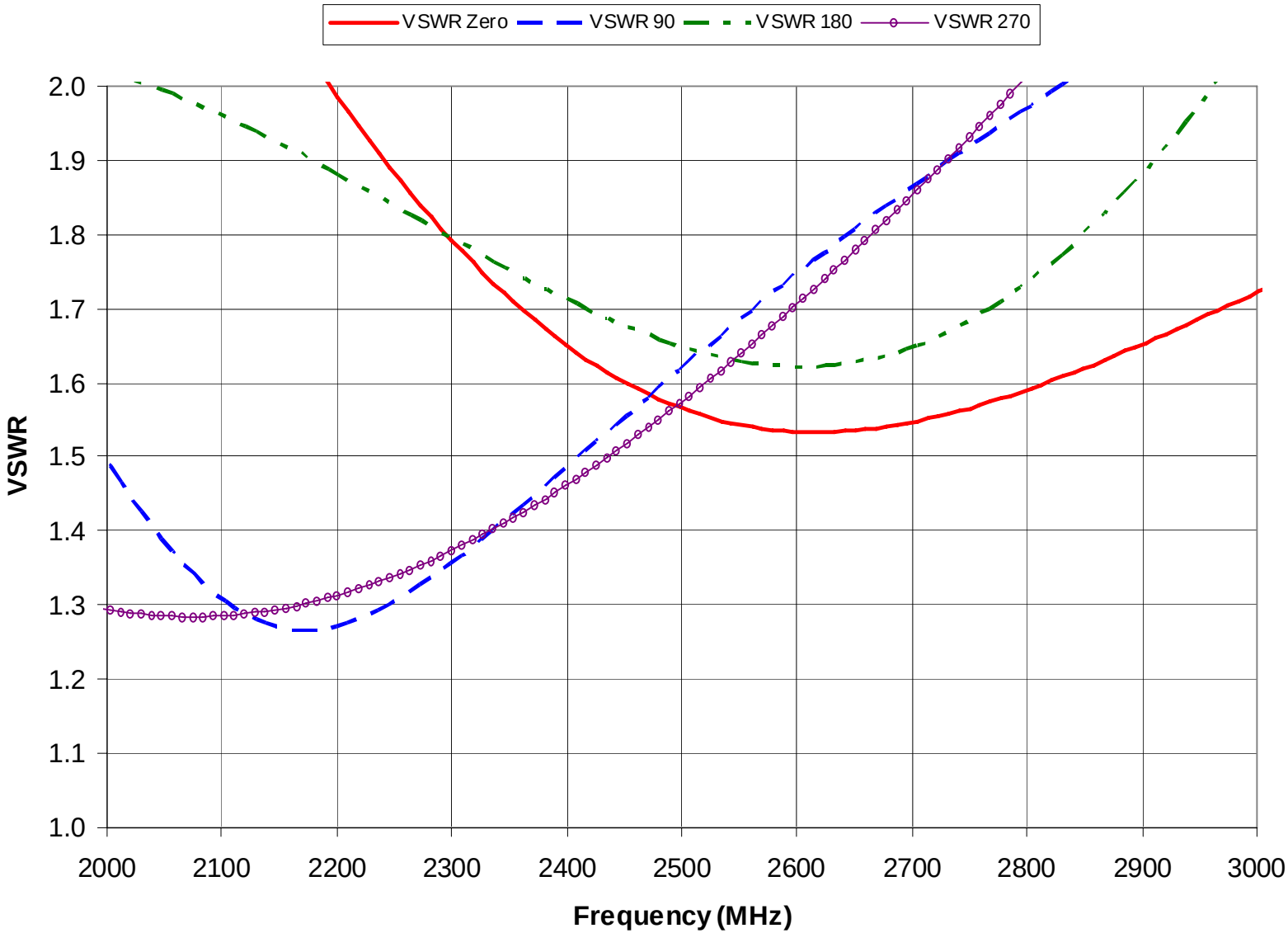
- Frequency: 2305 MHz to 2497 MHz
- Insertion loss: Less than 4dB (3dB Goal)
- Insertion Balance: +/- 1dB
- Phase shift: 90 and 180 degrees steps
- VSWR, 50 Ohms: Less than 1.5:1
- Supply Voltage: +/- 5 Volts
- Control Voltage: TTL(goal); or 0, -5V
- Size: 60x60 mil ANACHIP

Achieved Specification

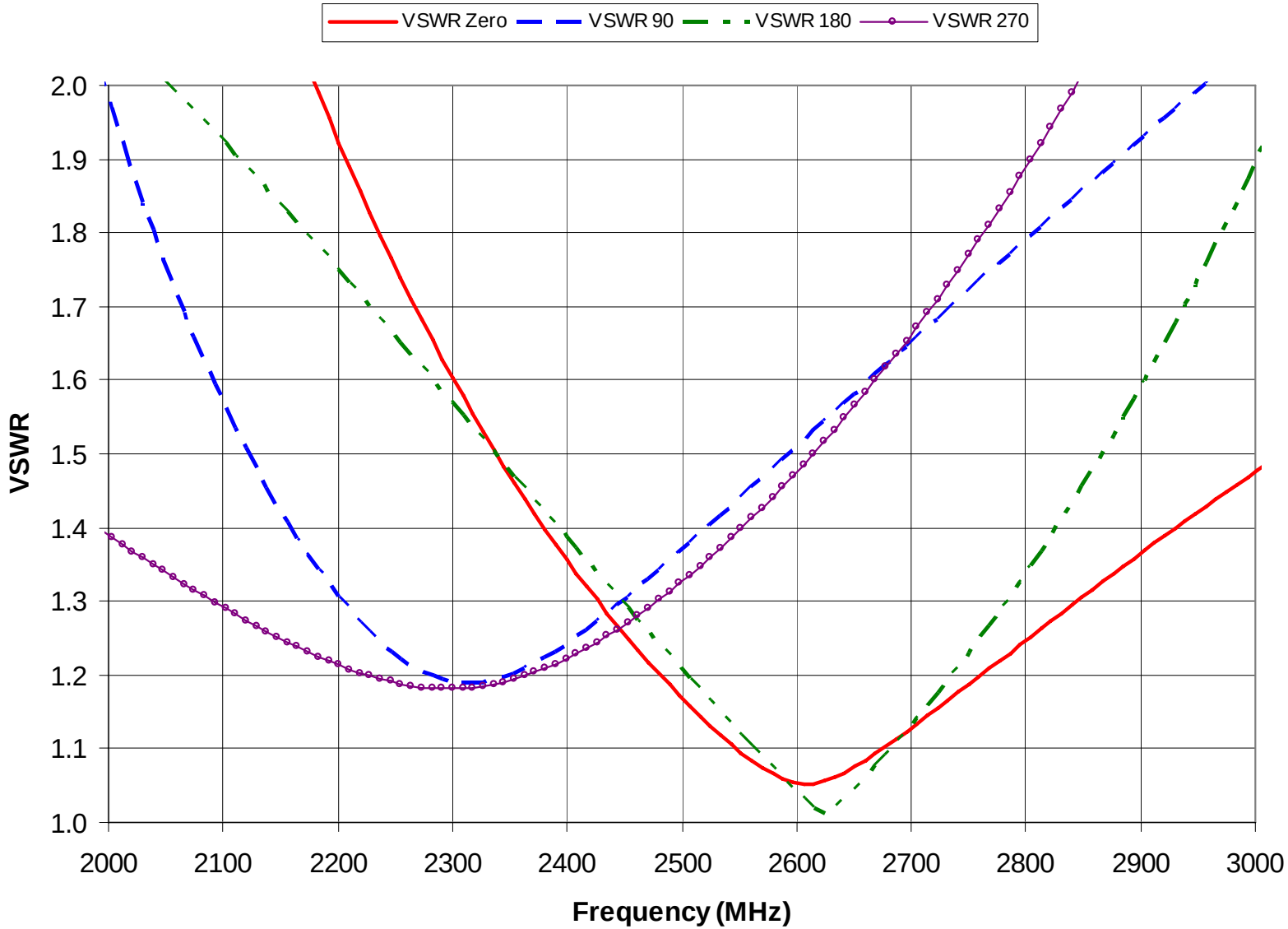
- The Specification of VSWR better then 1.5:1 was not achieved.
- A VSWR better then 1.8:1 was achieved

- Frequency(1.8:1 VSWR): 2300 MHz to 2642 MHz
- 1.8:1 VSWR Bandwidth: 342 MHz
- Insertion loss: 3.77 dB (2300 to 2500 MHz)
  3.96 dB (2300 to 2642 MHz)
- Insertion Balance: 0.45 dB (2300 to 2500 MHz)
  0.68 dB (2300 to 2642 MHz)

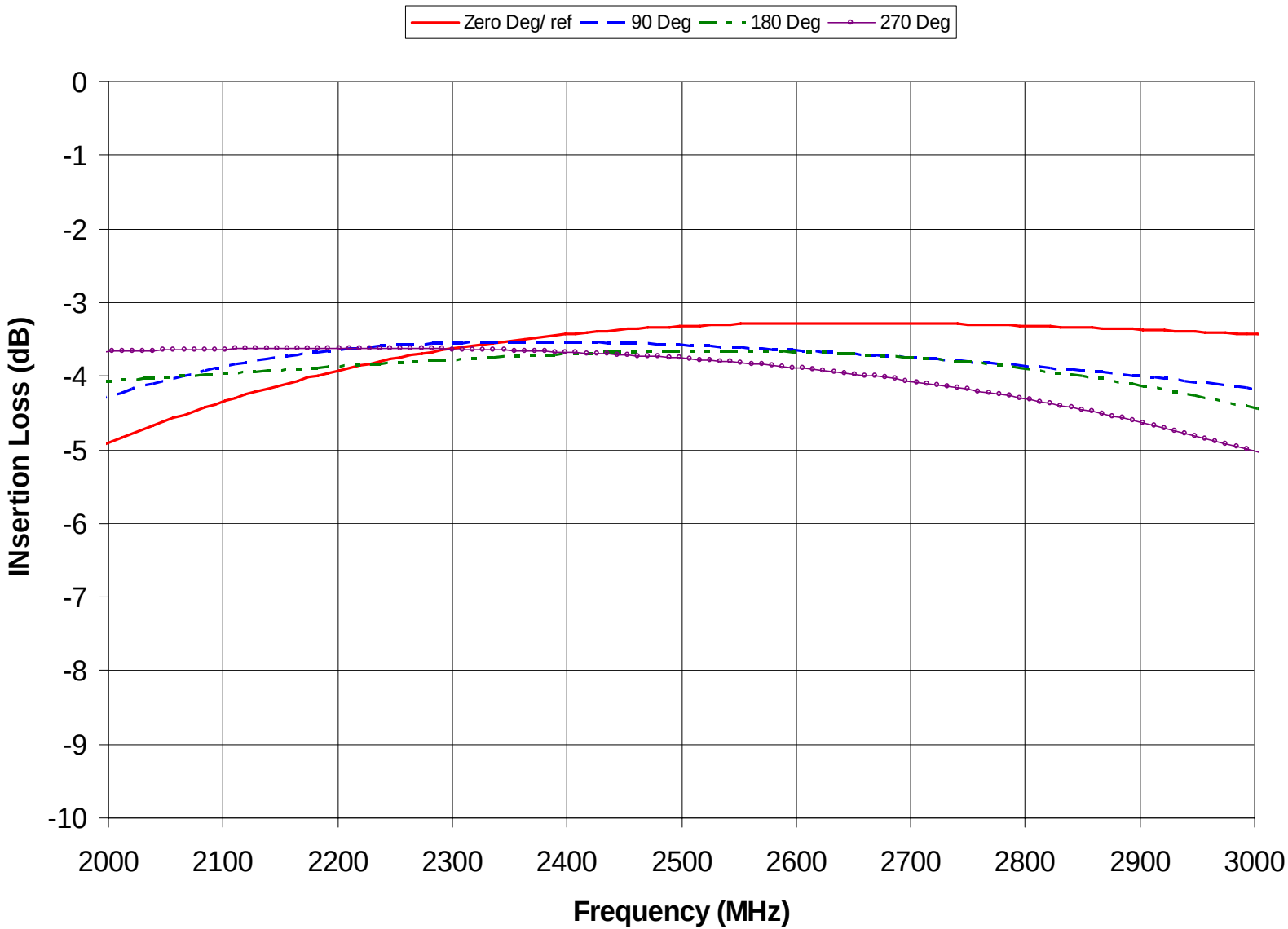
Two Bit Phase Shifter Input VSWR



Two Bit Phase Shifter Output VSWR



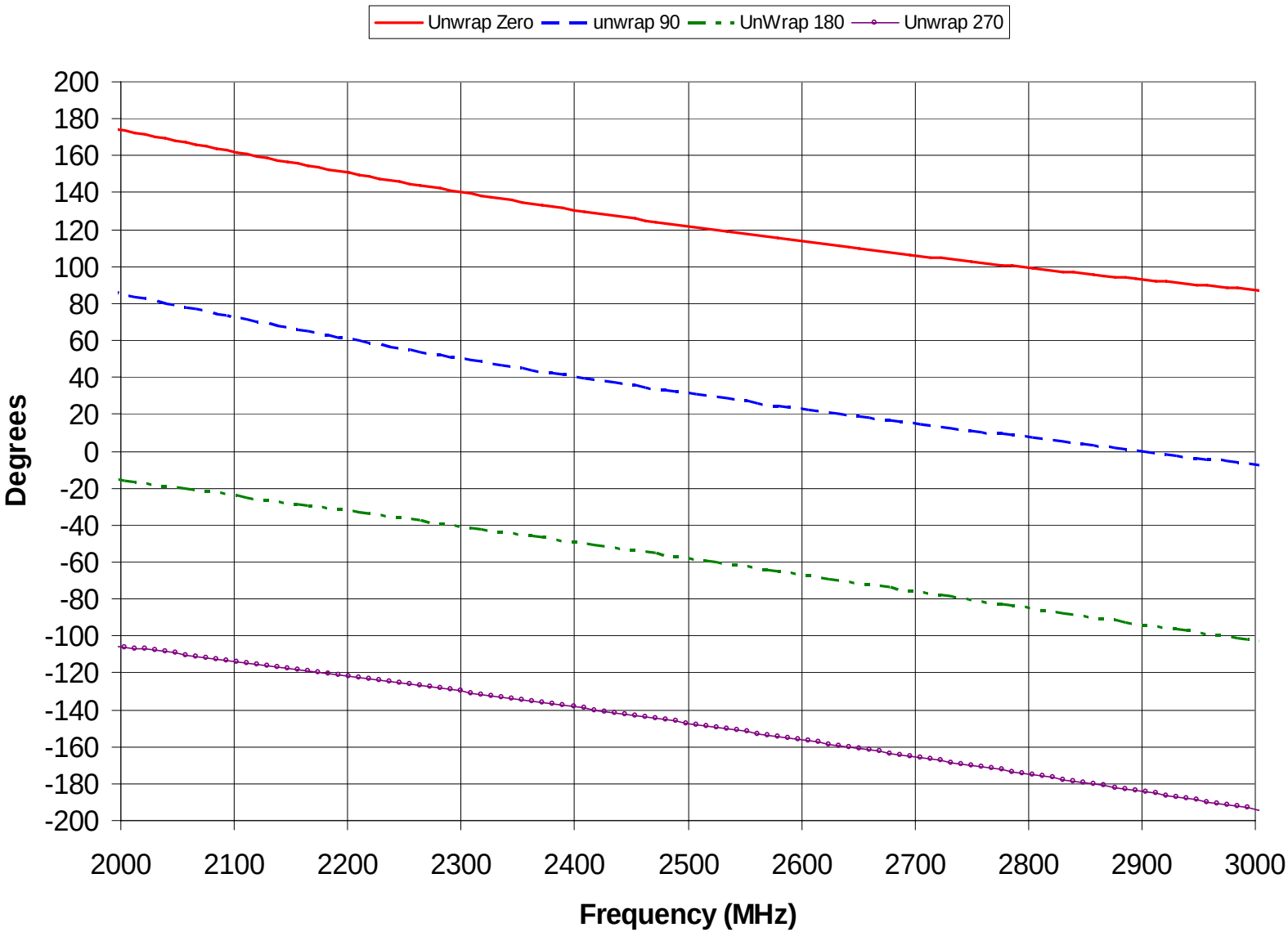
Two Bit Phase Shifter Insertion Loss (S21)



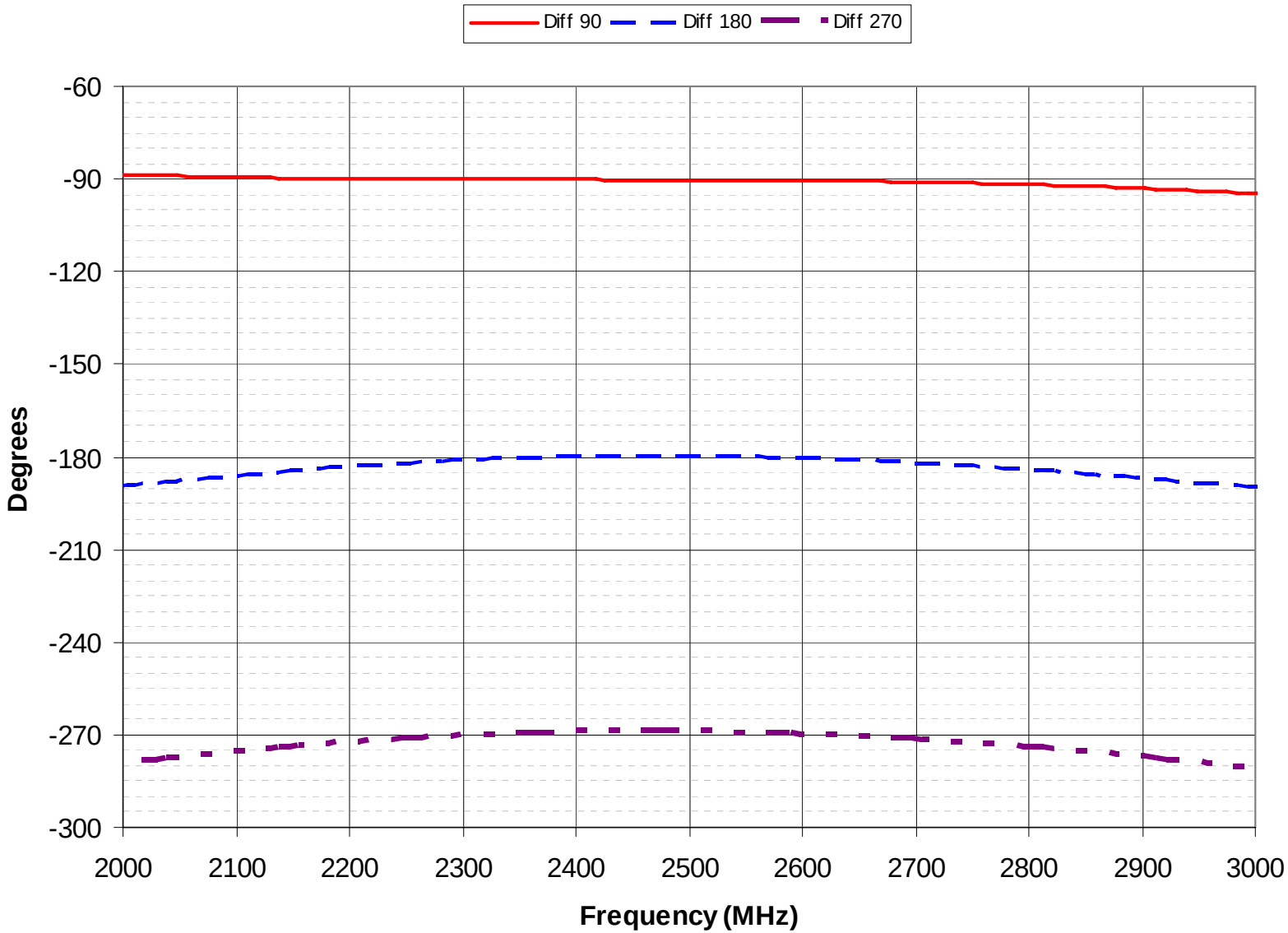
Achieved Specification

- Phase Shift: 90 and 180 degrees step
- Phase Flatness (2300 to 2500 MHz):
  - 90 Degree Shift -- 0.15 Deg.
  - 180 Degree Shift -- 1.4 Deg.
  - 270 Degree Shift -- 0.15 Deg.
- Phase Flatness (2300 to 2642 MHz):
  - 90 Degree Shift -- 0.53 Deg.
  - 180 Degree Shift -- 1.40 Deg.
  - 270 Degree Shift -- 0.49 Deg

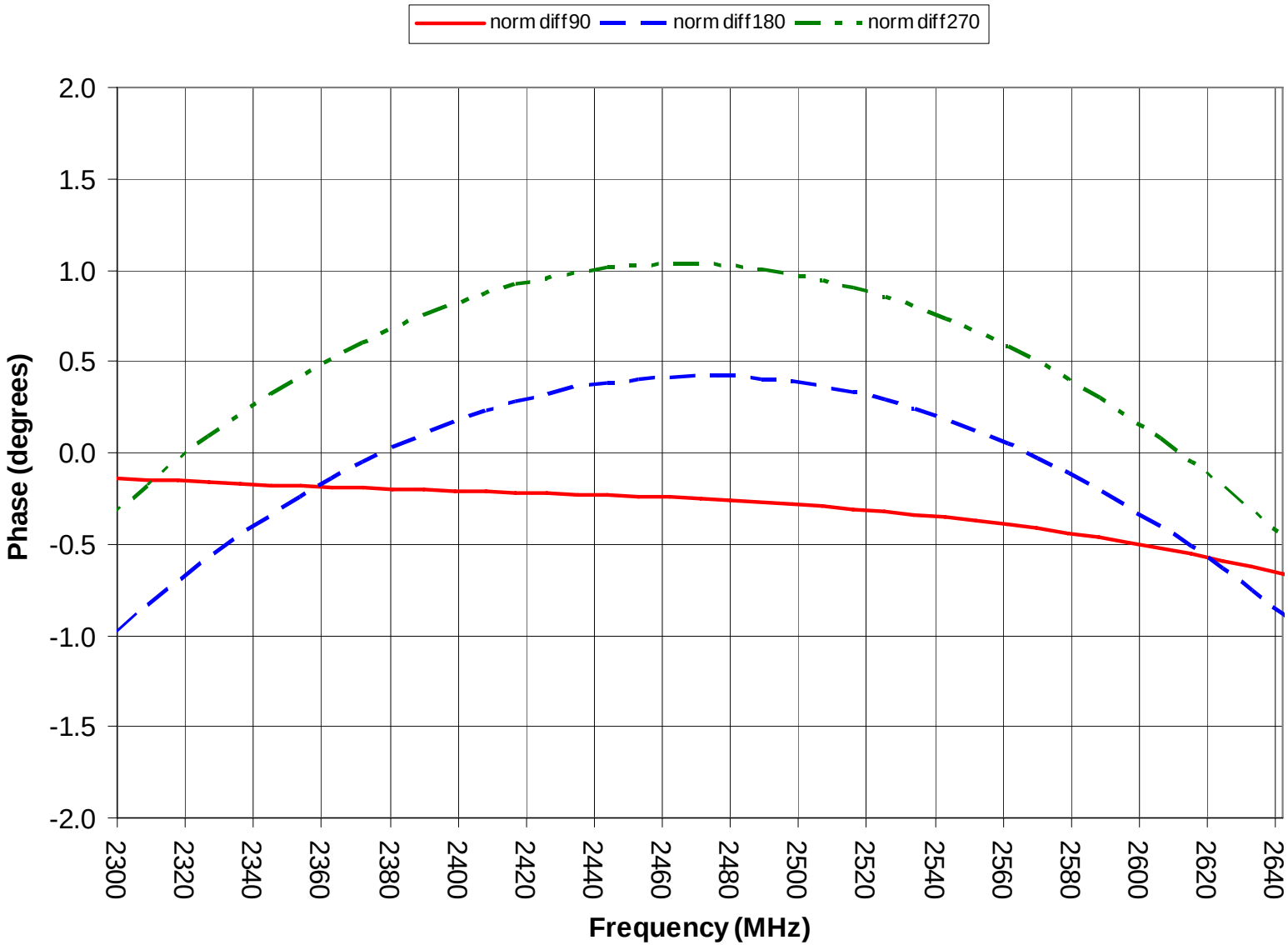
Two Bit Phase Shifter Unwrap Phase (S21)



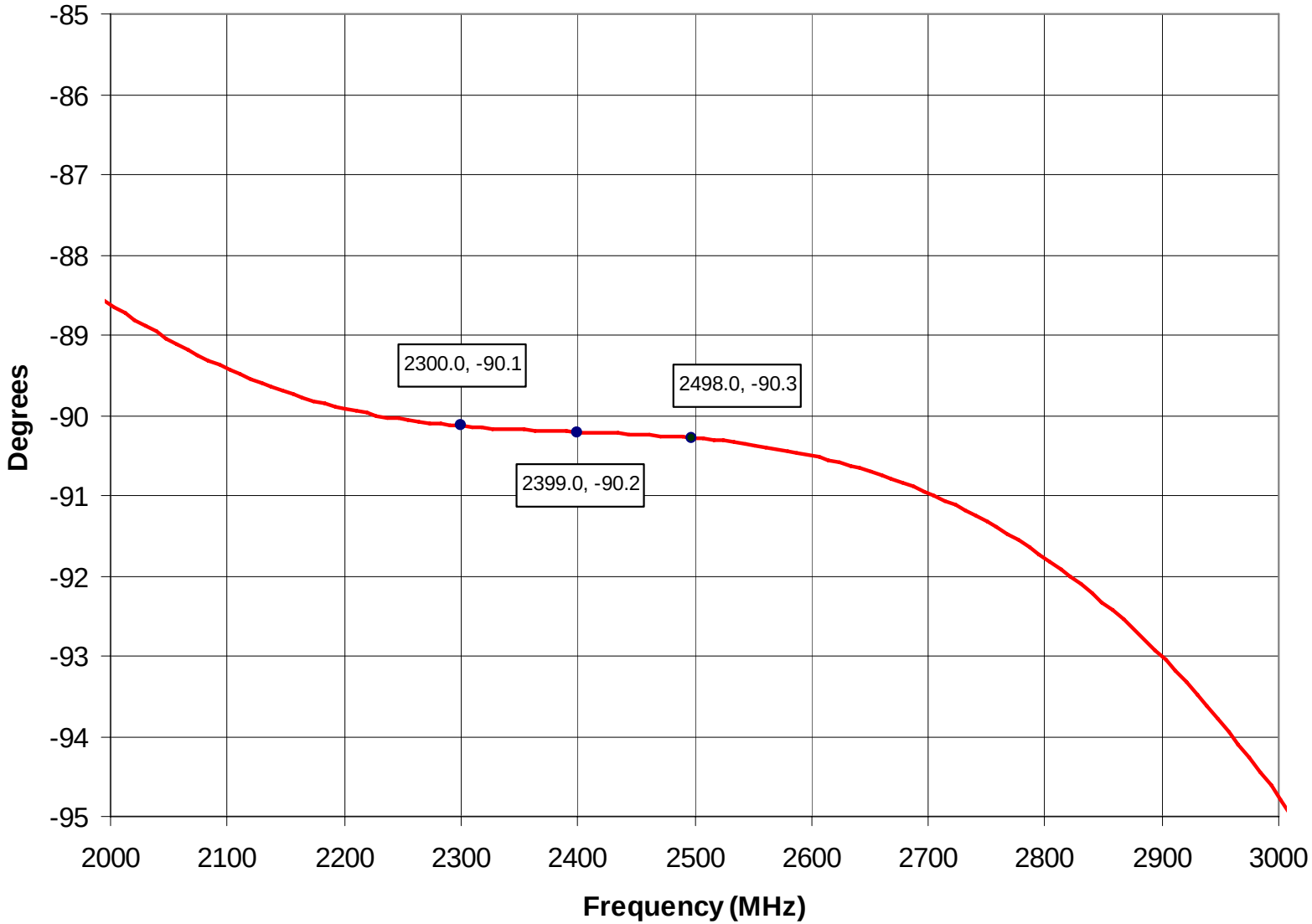
Two Bit Phase Shifter; Phase Difference



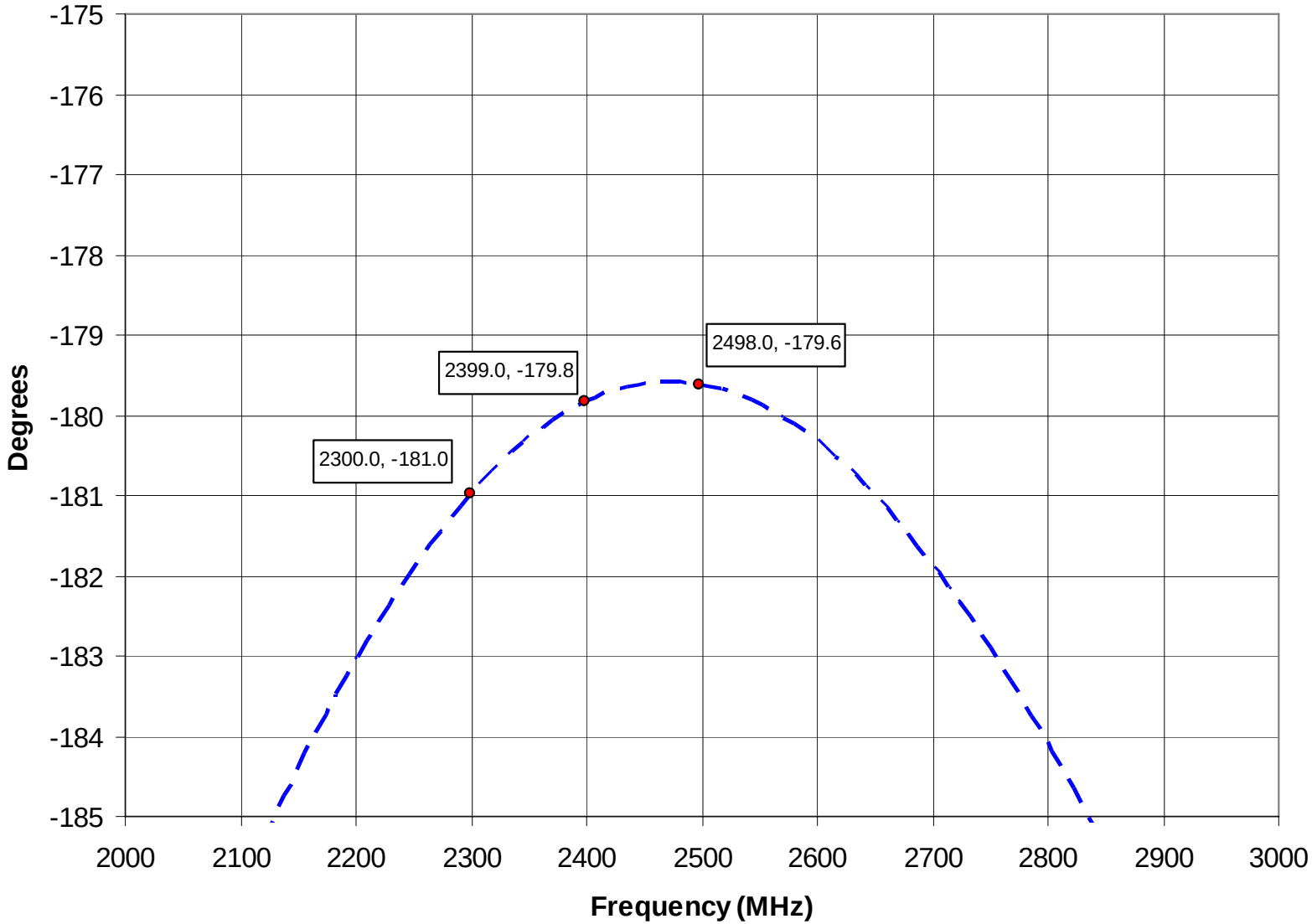
Two Bit Phase Shifter: Normalized Phase Difference



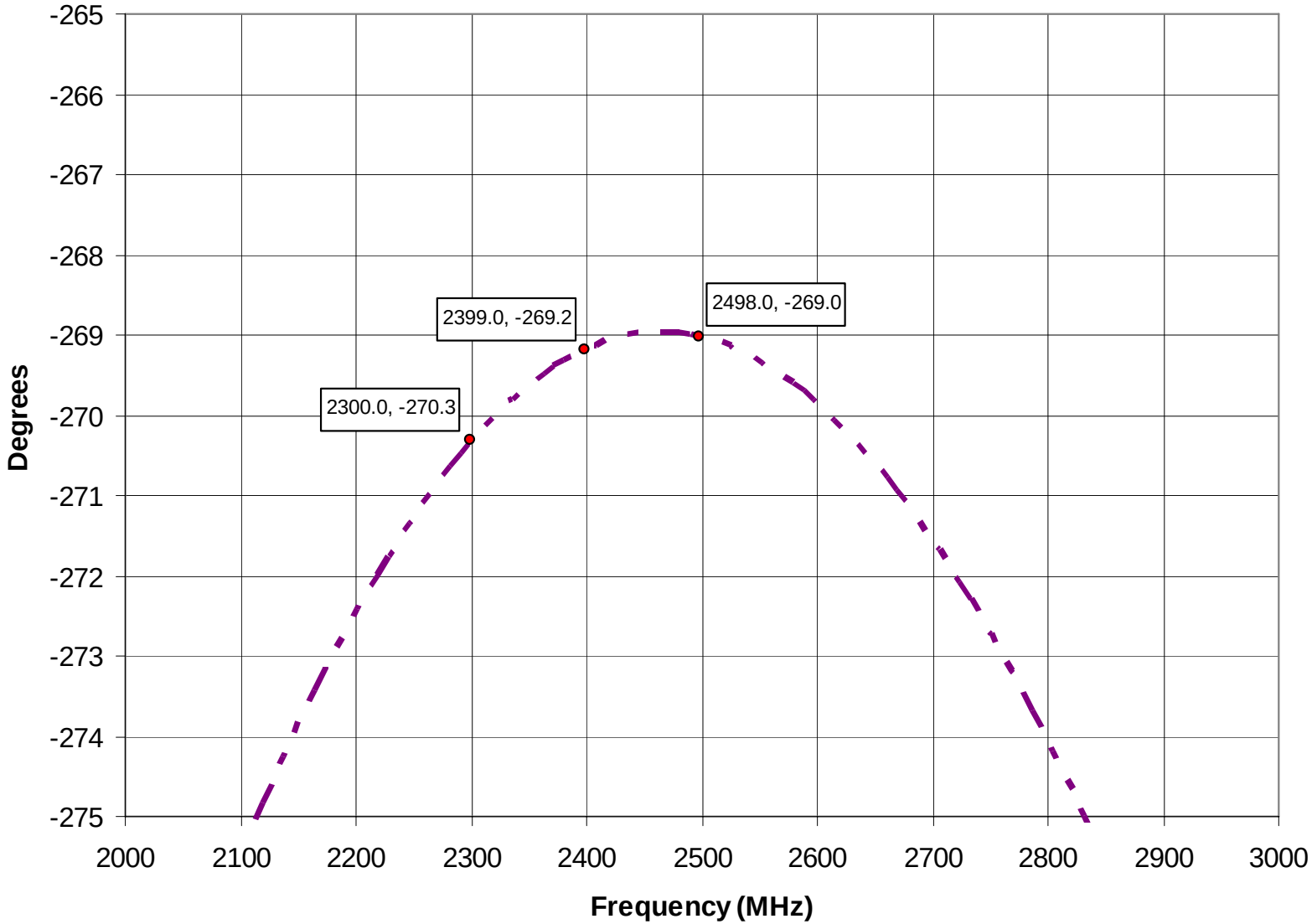
Two Bit Phase Shifter; Phase Difference = 90 Degrees



Two Bit Phase Shifter; Phase Difference = 180 Degrees



Two Bit Phase Shifter; Phase Difference = 270 Degrees



Achieved Specification

- Control Voltage is TTL (zero and +5V)
- Supply Voltage is +5 Volts

- Design fit on the 60 x 60 mil ANACHIP

Things to look at

- Pay more attention to input VSWR
  - Concentrated on phase and insertion loss
- Switch size
  - Used default transistor size
  - A smaller switch may work as well while conserving space
- Wide Banding
  - Use two series 45 Deg element instead of a single 90 deg. element
- Switch gate voltage
  - Changed depending on phase selected

DC Gate Bias

Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90(V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
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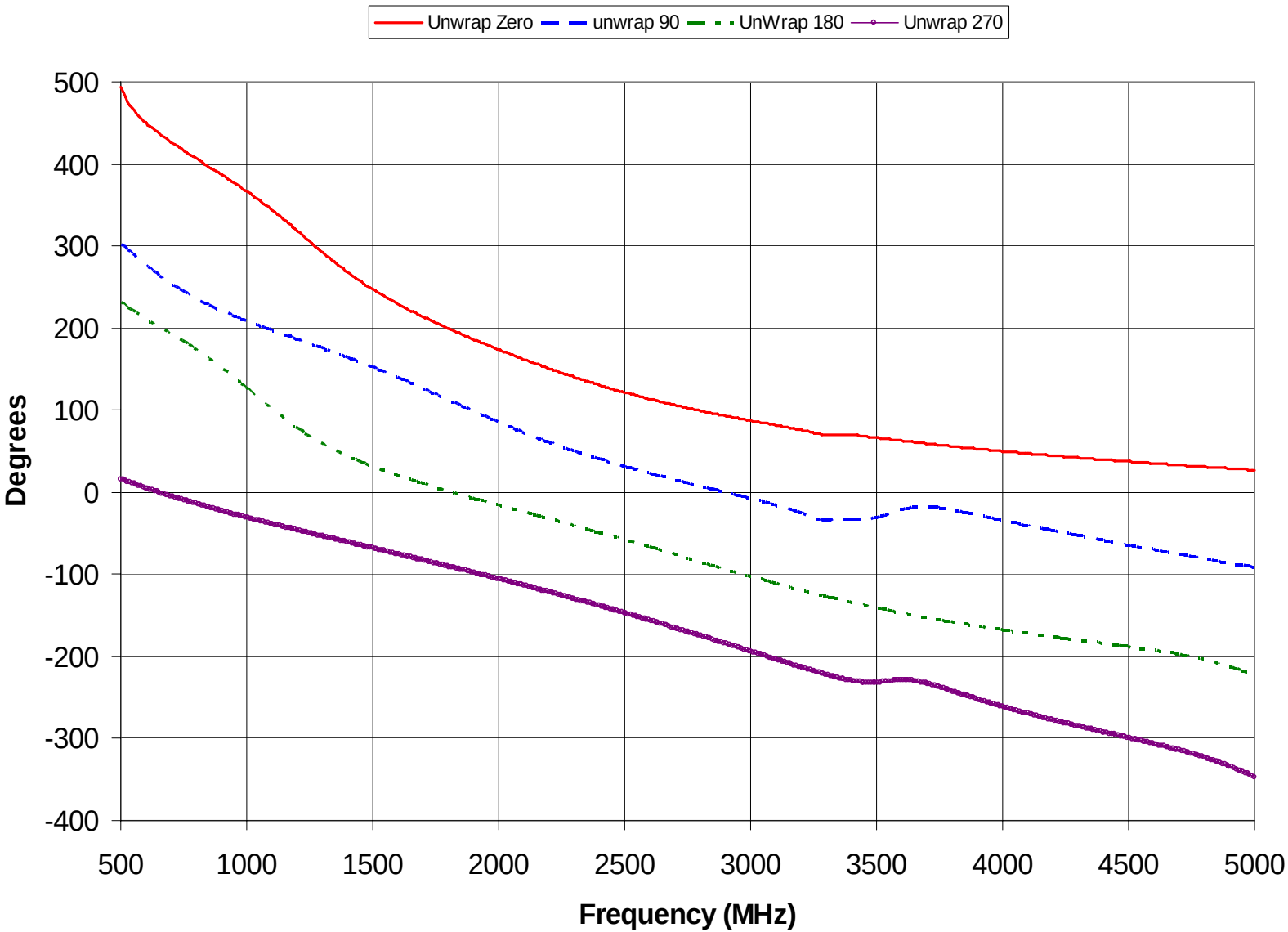
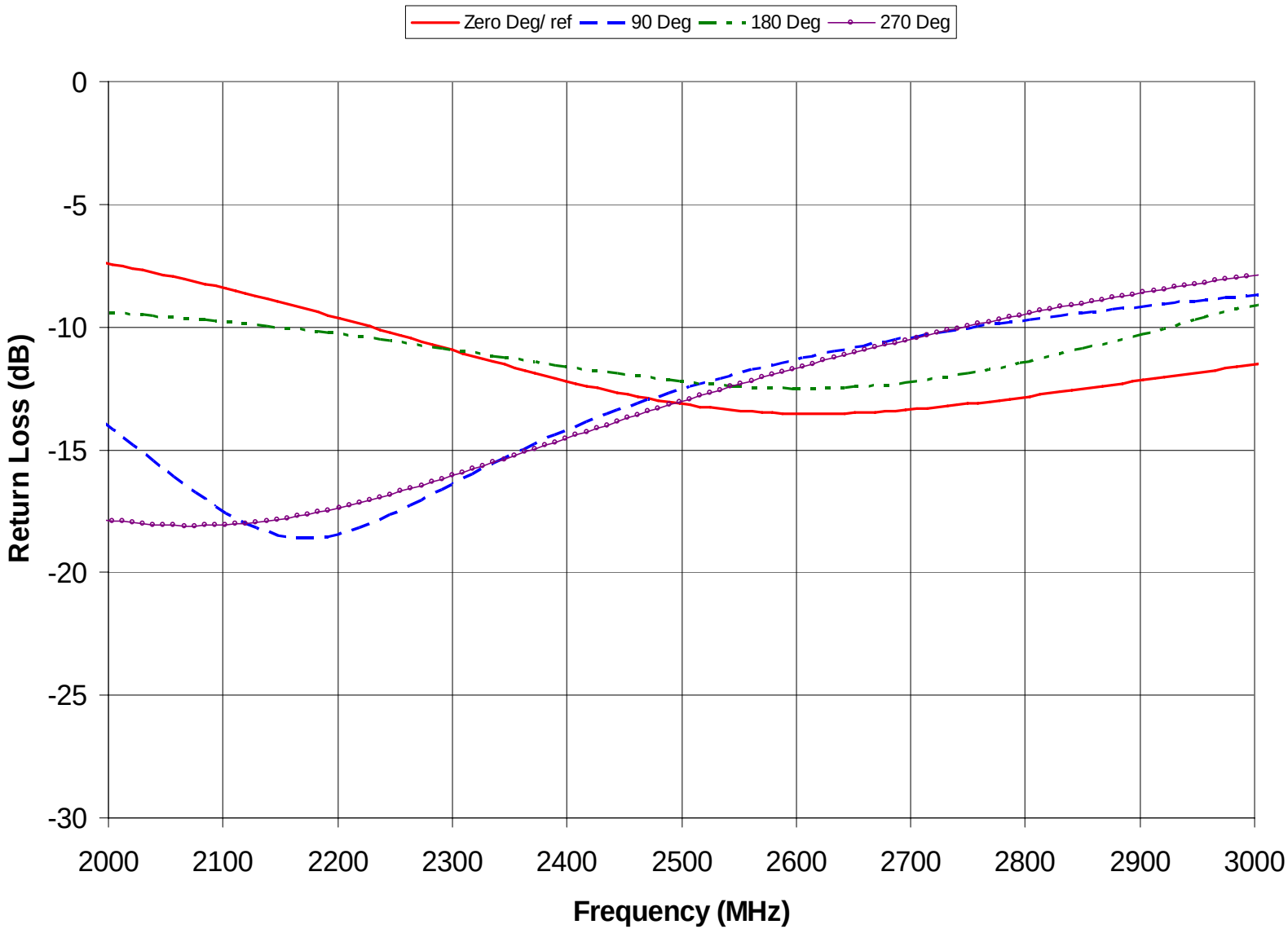
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

Backup Slides

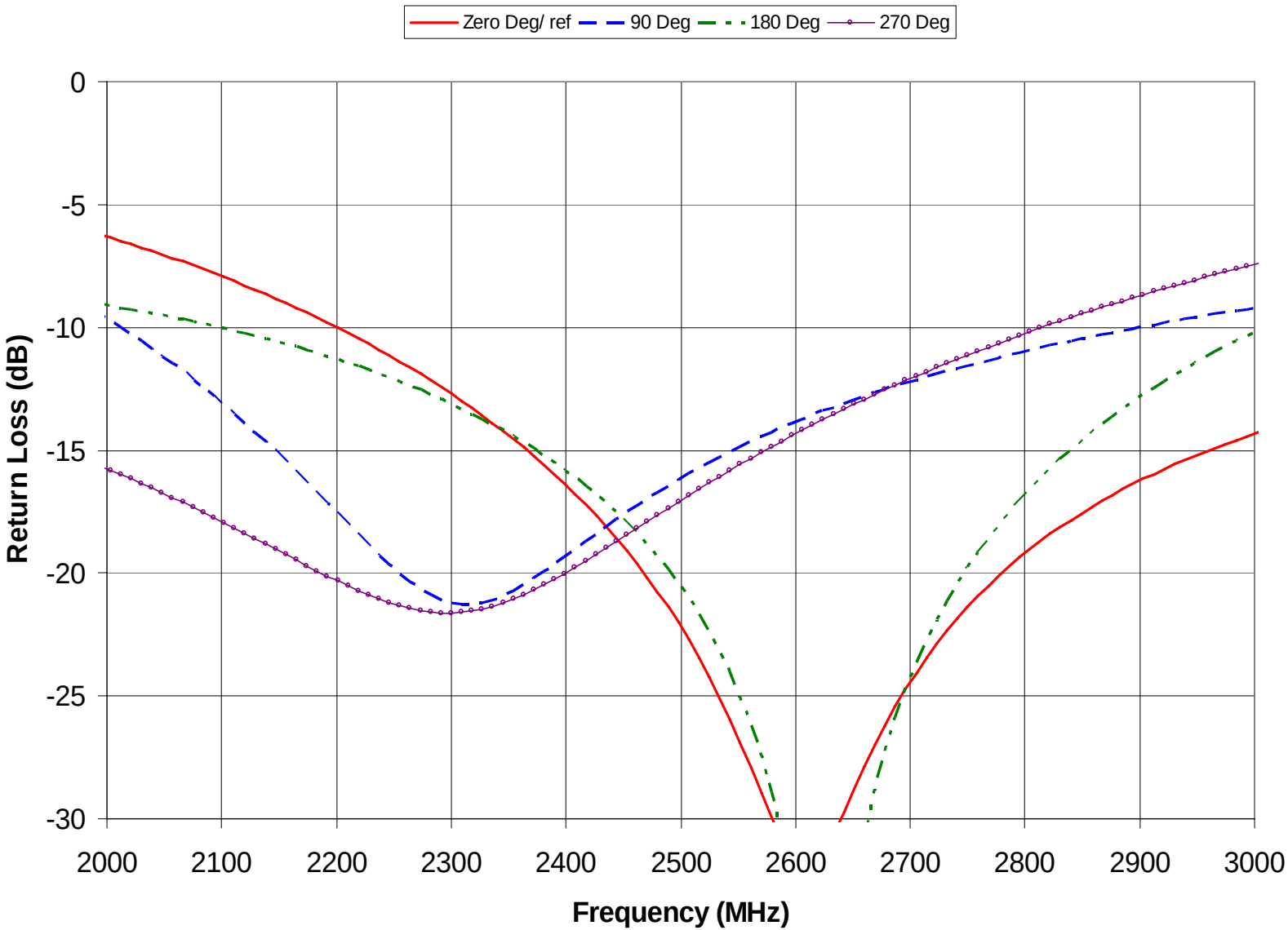
Two Bit Phase Shifter Unwrap Phase (S21)

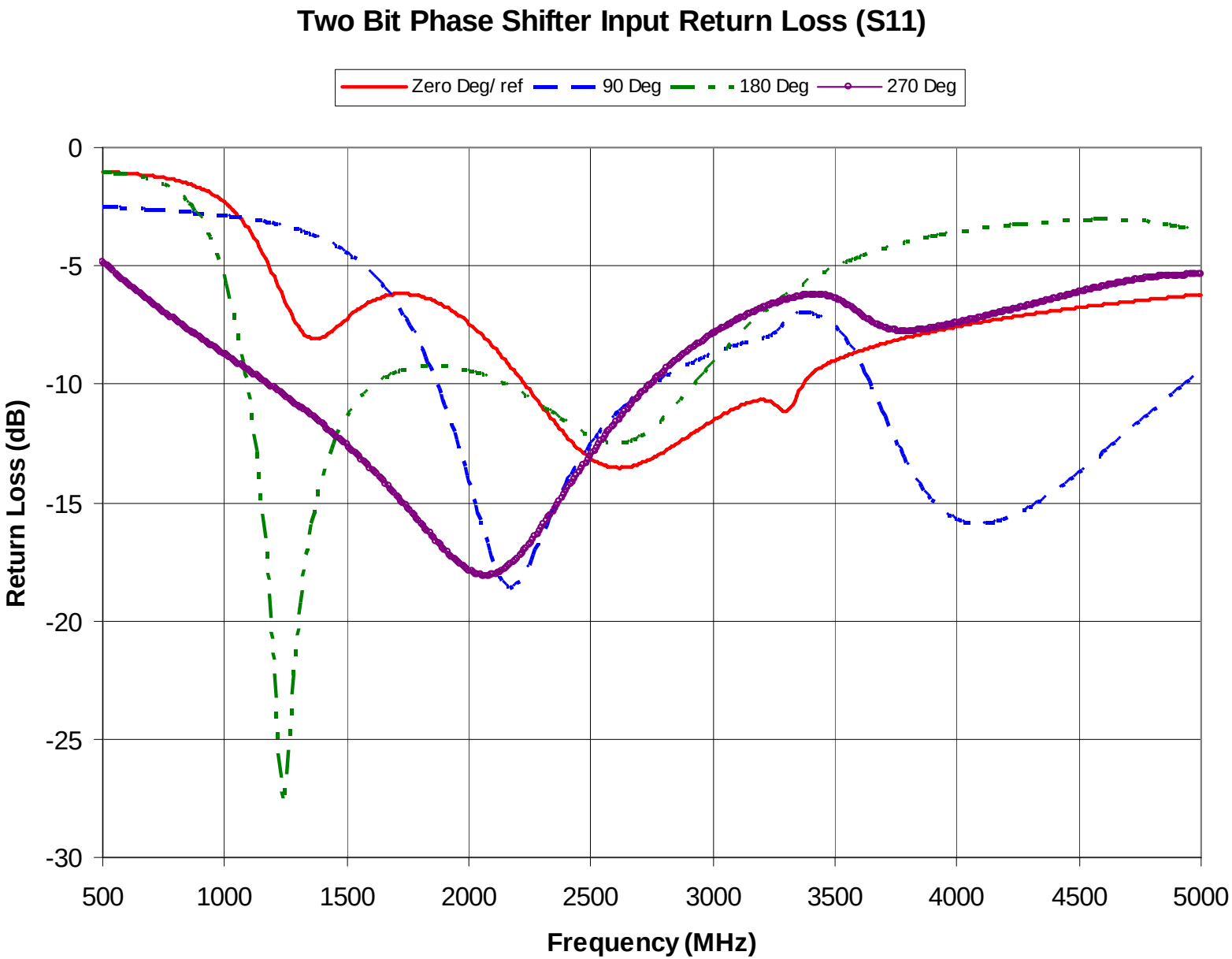


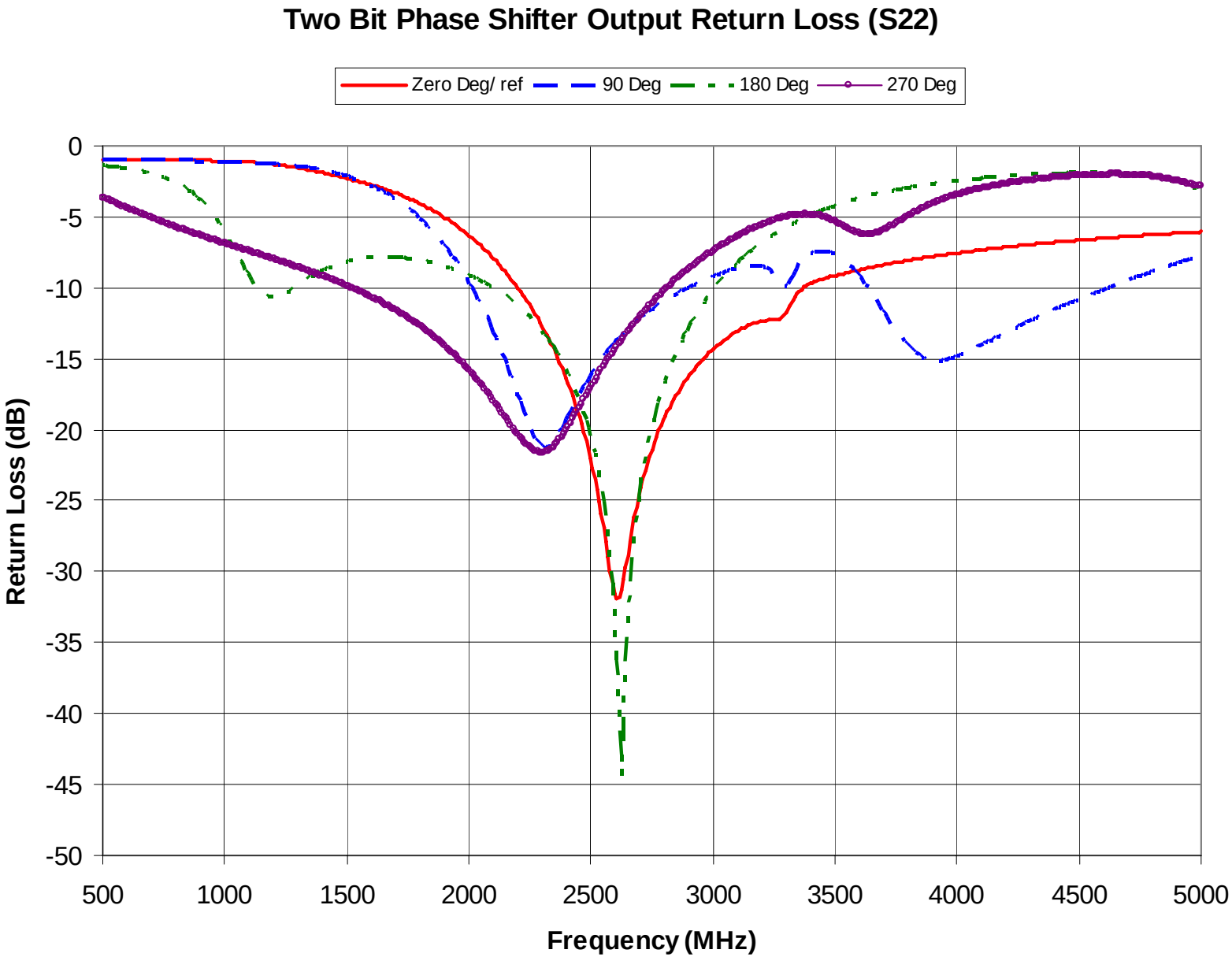
Two Bit Phase Shifter Input Return Loss (S11)

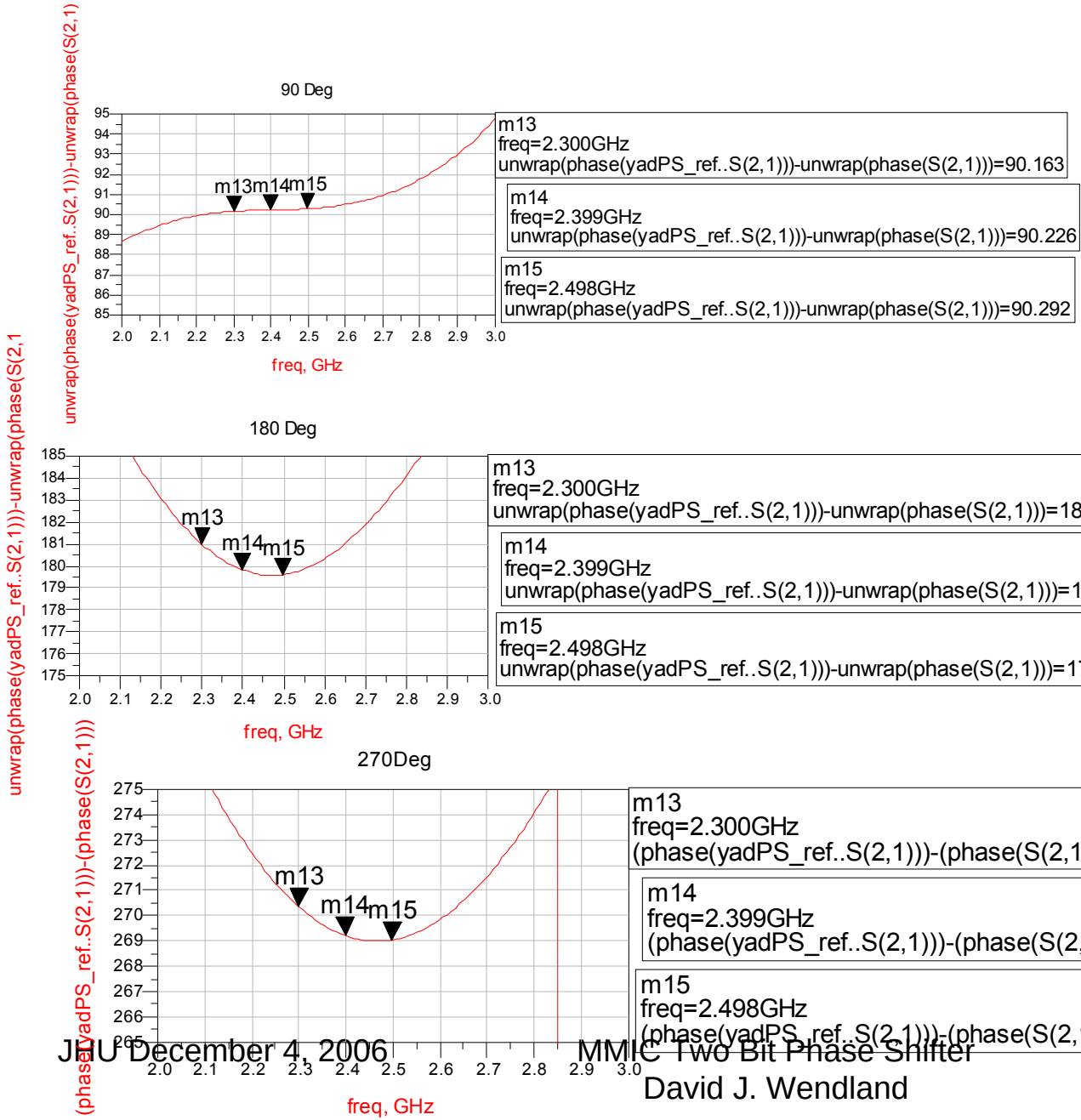


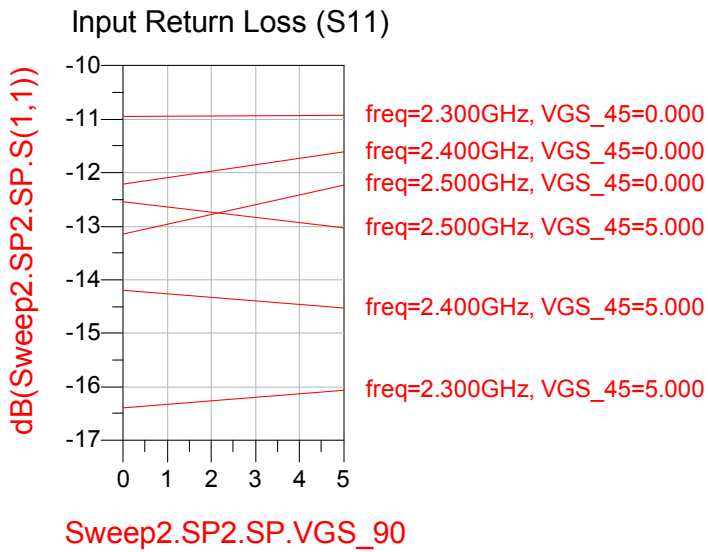
Two Bit Phase Shifter Output Return Loss (S22)

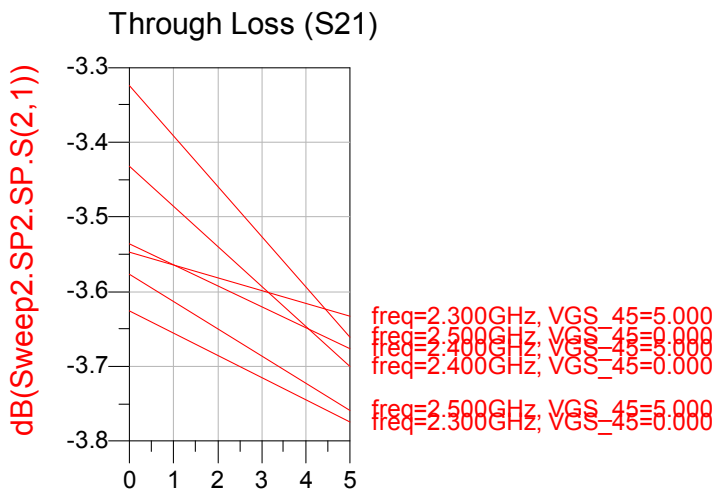


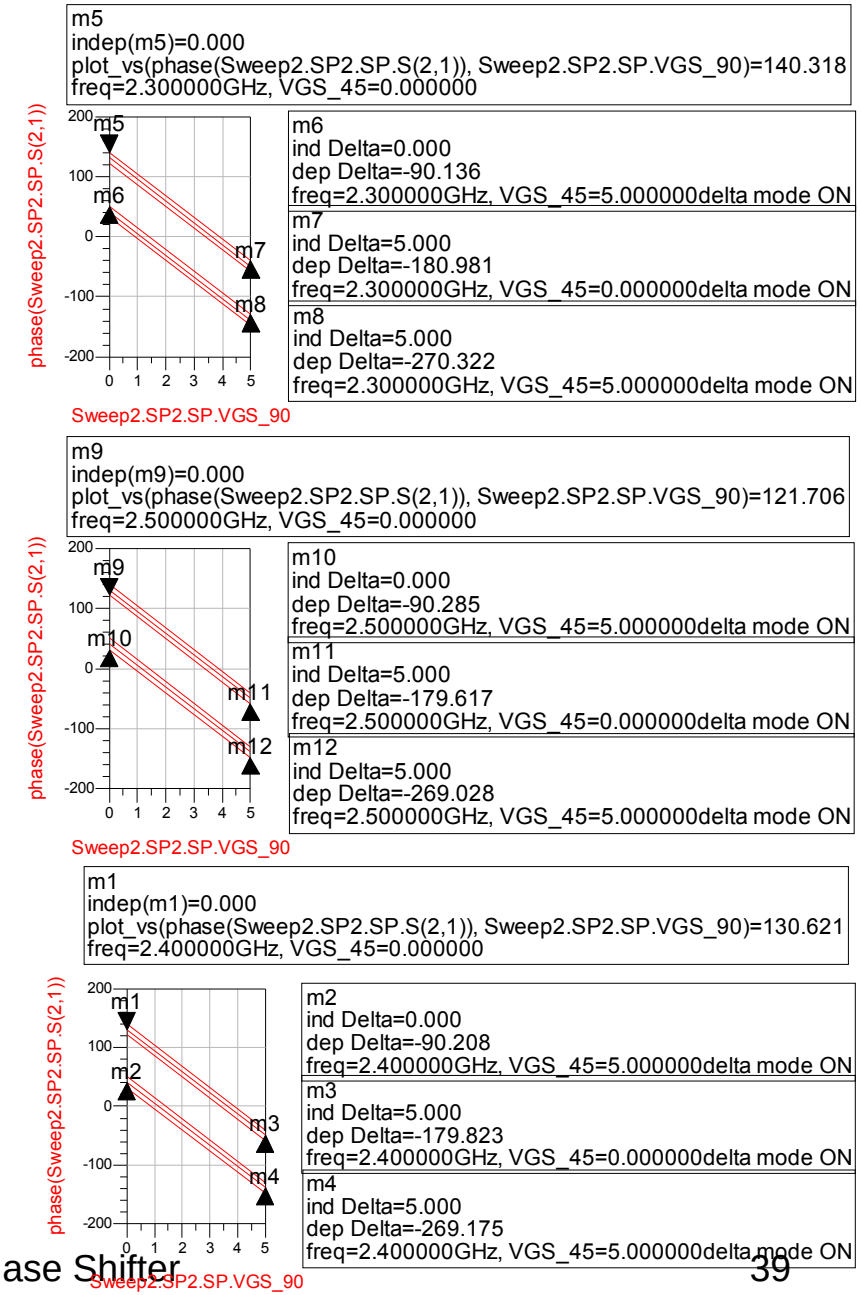

Two Bit Phase Shifter Input Return Loss (S11)
Zero Deg/ ref
90 Deg
180 Deg
270 Deg
0
-5
-10
-15
-20
-25
-30
Return Loss (dB)
500
1000
1500
2000
2500
3000
3500
4000
4500
5000
Frequency (MHz)


Two Bit Phase Shifter Output Return Loss (S22)
Zero Deg/ ref
90 Deg
180 Deg
270 Deg
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
Return Loss (dB)
500
1000
1500
2000
2500
3000
3500
4000
4500
5000
Frequency (MHz)


90 Deg
unwrap(phase(yadPS_ref..S(2,1)))-unwrap(phase(S(2,1)))
freq, GHz
m13
freq=2.300GHz
unwrap(phase(yadPS_ref..S(2,1)))-unwrap(phase(S(2,1)))=90.163
m14
freq=2.399GHz
unwrap(phase(yadPS_ref..S(2,1)))-unwrap(phase(S(2,1)))=90.226
m15
freq=2.498GHz
unwrap(phase(yadPS_ref..S(2,1)))-unwrap(phase(S(2,1)))=90.292
180 Deg
unwrap(phase(yadPS_ref..S(2,1)))-unwrap(phase(S(2,1)))
freq, GHz
m13
freq=2.300GHz
unwrap(phase(yadPS_ref..S(2,1)))-unwrap(phase(S(2,1)))=180.981
m14
freq=2.399GHz
unwrap(phase(yadPS_ref..S(2,1)))-unwrap(phase(S(2,1)))=179.830
m15
freq=2.498GHz
unwrap(phase(yadPS_ref..S(2,1)))-unwrap(phase(S(2,1)))=179.612
270Deg
(phase(yadPS_ref..S(2,1)))-(phase(S(2,1)))
freq, GHz
m13
freq=2.300GHz
(phase(yadPS_ref..S(2,1)))-(phase(S(2,1)))=270.347
m14
freq=2.399GHz
(phase(yadPS_ref..S(2,1)))-(phase(S(2,1)))=269.202
m15
freq=2.498GHz
(phase(yadPS_ref..S(2,1)))-(phase(S(2,1)))=269.032


Input Return Loss (S11)
dB(Sweep2.SP2.SP.S(1,1))
-10
-11
-12
-13
-14
-15
-16
-17
0 1 2 3 4 5
freq=2.300GHz, VGS_45=0.000
freq=2.400GHz, VGS_45=0.000
freq=2.500GHz, VGS_45=0.000
freq=2.500GHz, VGS_45=5.000
freq=2.400GHz, VGS_45=5.000
freq=2.300GHz, VGS_45=5.000
Sweep2.SP2.SP.VGS_90


Through Loss (S21)
dB(Sweep2.SP2.SP.S(2,1))
-3.3
-3.4
-3.5
-3.6
-3.7
-3.8
0 1 2 3 4 5
freq=2.300GHz, VGS_45=5.000
freq=2.500GHz, VGS_45=0.000
freq=2.400GHz, VGS_45=5.000
freq=2.400GHz, VGS_45=0.000
freq=2.500GHz, VGS_45=5.000
freq=2.300GHz, VGS_45=0.000
Sweep2.SP2.SP.VGS_90


m5
indep(m5)=0.000
plot_vs(phase(Sweep2.SP2.SP.S(2,1)), Sweep2.SP2.SP.VGS_90)=140.318
freq=2.300000GHz, VGS_45=0.000000
m6
ind Delta=0.000
dep Delta=-90.136
freq=2.300000GHz, VGS_45=5.000000delta mode ON
m7
ind Delta=5.000
dep Delta=-180.981
freq=2.300000GHz, VGS_45=0.000000delta mode ON
m8
ind Delta=5.000
dep Delta=-270.322
freq=2.300000GHz, VGS_45=5.000000delta mode ON
phase(Sweep2.SP2.SP.S(2,1))
200
100
0
-100
-200
0 1 2 3 4 5
Sweep2.SP2.SP.VGS_90
m9
indep(m9)=0.000
plot_vs(phase(Sweep2.SP2.SP.S(2,1)), Sweep2.SP2.SP.VGS_90)=121.706
freq=2.500000GHz, VGS_45=0.000000
m10
ind Delta=0.000
dep Delta=-90.285
freq=2.500000GHz, VGS_45=5.000000delta mode ON
m11
ind Delta=5.000
dep Delta=-179.617
freq=2.500000GHz, VGS_45=0.000000delta mode ON
m12
ind Delta=5.000
dep Delta=-269.028
freq=2.500000GHz, VGS_45=5.000000delta mode ON
Sweep2.SP2.SP.VGS_90
m1
indep(m1)=0.000
plot_vs(phase(Sweep2.SP2.SP.S(2,1)), Sweep2.SP2.SP.VGS_90)=130.621
freq=2.400000GHz, VGS_45=0.000000
m2
ind Delta=0.000
dep Delta=-90.208
freq=2.400000GHz, VGS_45=5.000000delta mode ON
m3
ind Delta=5.000
dep Delta=-179.823
freq=2.400000GHz, VGS_45=0.000000delta mode ON
m4
ind Delta=5.000
dep Delta=-269.175
freq=2.400000GHz, VGS_45=5.000000delta mode ON
Sweep2.SP2.SP.VGS_90