S-Band Low Power Low Noise Amplifier

By: Noah Hughes
Larry Macejka

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Johns Hopkins University
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Abstract

The design of a MMIC low power low noise amplifier (LNA) circuit will be described in this paper. The amplifier design is based on the requirements of an S-band duplex transceiver and designed to operate with very low power. The LNA operates with a DC power consumption of approximately 17mW drawing 5.14mA at 3.3 V. The amplifier has a 1dB bandwidth of ~500MHz around the required 2305 to 2497 MHz operating range. The noise figure of the LNA is less than the design requirement of 3dB and the gain reaches 27dB under the operating bandwidth. In addition the output port match exceeds –15dB and the input port match is better than –10dB. The stability of the amplifier is unconditionally stable between 0.5 and 5 GHz. This design is placed in the 60 X 60 mil Anachip layout as required the Triquint for fabrication.

Introduction

This report will focus on the design, simulation, layout, optimization and test plan for the low power low noise amplifier. The LNA is at the front end of the S-band receiver providing the first stage of amplification after the antenna and adding as little noise as possible, shown in Figure 2. The design consists of a two-stage amplifier design powered by two positive 3.3V sources, shown in Figure 1. Two 4 X 15um (60um) EMODE FETs are used in the amplifier due to their higher gain and lower noise figure. The output and intermediate matching networks are used to ensure a proper match and maximum gain, while the input-matching network sets the noise figure for the amplifier. Finally a feedback network is used on each of the amplifier stages to broaden the gain, stabilize the amplifier and reduce power consumption.

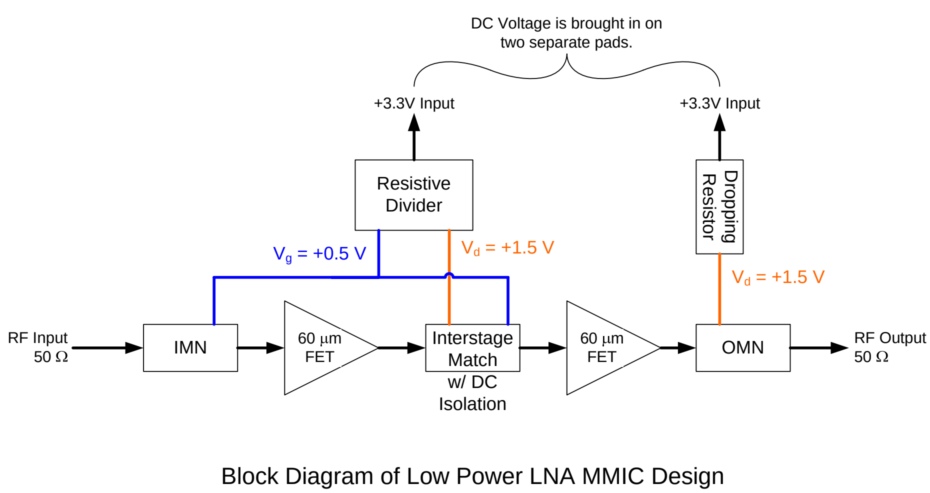


Figure 1: Two Stage Low Power LNA

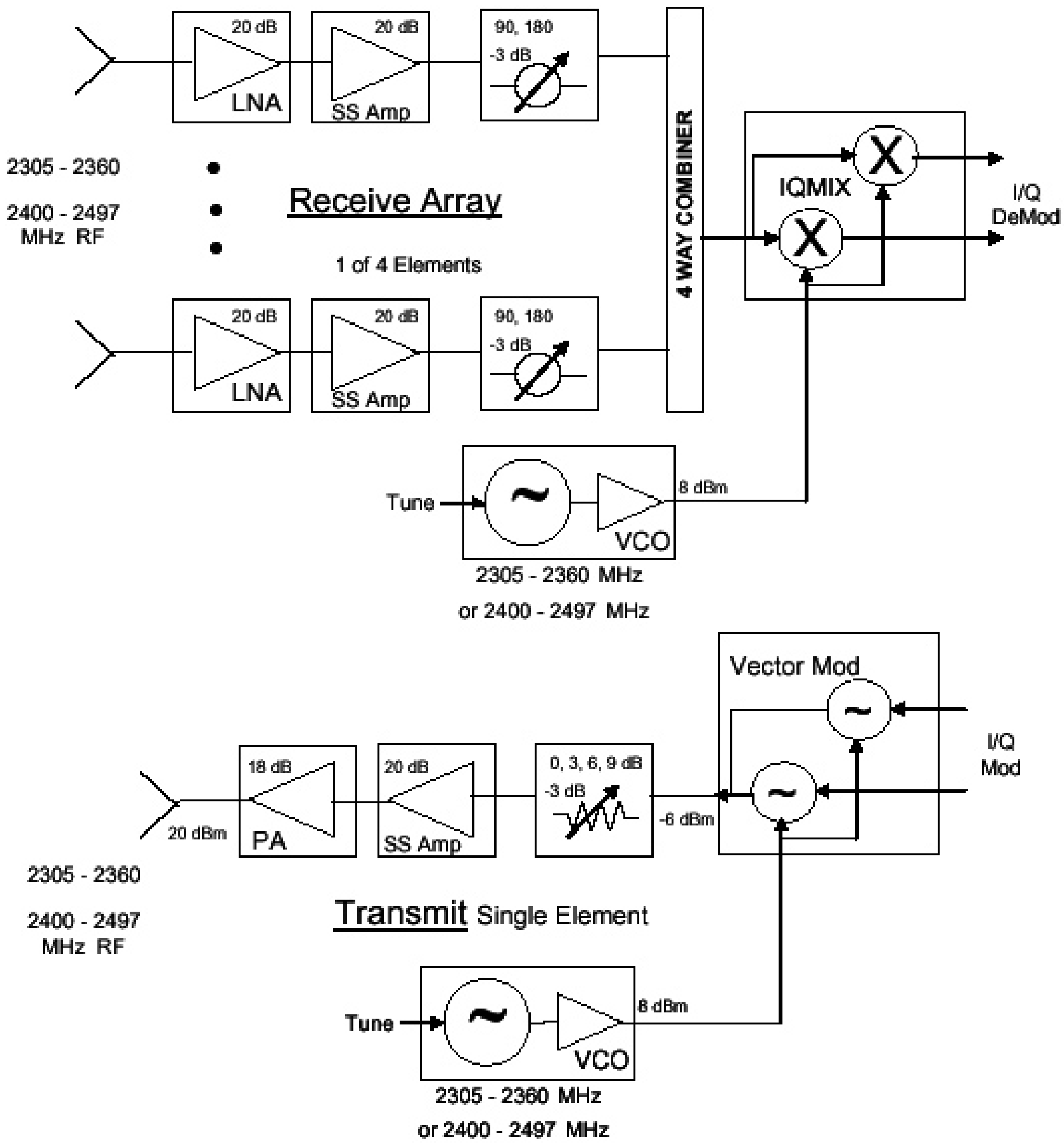


Figure 2: Duplex Transceiver System

Design

Originally the LNA design was focused on reducing the power consumption of the amplifier to a level where it could be powered by a battery. To achieve this both stages of the amplifier were stabilized using a resistor and capacitor to provide a feedback path between the drain and gate. Initially there was concern the feedback path on the first stage of the amplifier would increase the noise figure above the requirement, but we later found this to be not the case. With the two FET's stabilized two identical single stage LNAs were designed using ideal components. The input matching circuit of amplifier was tuned to produce the best noise figure possible, while the output matching circuit was tuned to the best VSWR. As an initial cut at the design the two stages were cascaded together. The results of this initial simulation were favorable resulting in a noise figure of ~1.8dB and a gain of ~30dB across the design band, which removed our concern of the feedback network. At that point the number and size of components in the matching networks was taken into account especially the intermediate matching network, which consisted of 2 inductors and 2 capacitors. Both the intermediate and output matching networks were retuned to a shunt inductor and series capacitor topology. This provided an effective RF disconnect between the power input and the RF trace and reduced the number of components to two apiece.

After the ideal design produced favorable simulation results, the ideal components were replaced with Triquint components and simulated again. Initially the circuit had to be retuned due to differences between the Triquint and ideal models. The extra resistance in the Triquint models also increased the noise figure slightly to ~2dB and reduced the gain to ~27dB, but still remained well within design margin. At this point a flaw in the design was discovered. The two drain power supplies could not be combined together on the chip without causing the amplifier to become unstable. To alleviate this problem a resistive divider was installed on one of the drain sources allowing it to provide both gate voltages as well as one of the drain supplies. This allowed the amplifier chip to only require two 3.3V power supply lines from the same power supply.

With this problem out of the way, the iterative layout and interconnect simulation process began. The two stage LNA was initially layed out with just the components. The amplifier's interconnect was added in later according to the orientation and placement of the components. Special consideration was taken to ensure the trace width of the amplifier's interconnect did not violate any current carrying restrictions, given that most of the circuit was routed on Metal 0. Once a reasonable layout was created, the microstrip interconnect was placed in a simulation along with the rest of the amplifier. This resulted in multiple iterations of tuning the circuit in the simulation and then changing the layout accordingly. In the end, a favorable compromise was achieved that resulted in an error free layout and a simulation that passed all of the design requirements.

Requirements& Trade-Offs

	Requirement		
Parameter	**Desired**	**Goal**	**Expected Performance**
Frequency	2305 – 2497MHz		2305 - 2497
Bandwidth	800MHz		800 MHz
Gain	>20dB		27.5 dB

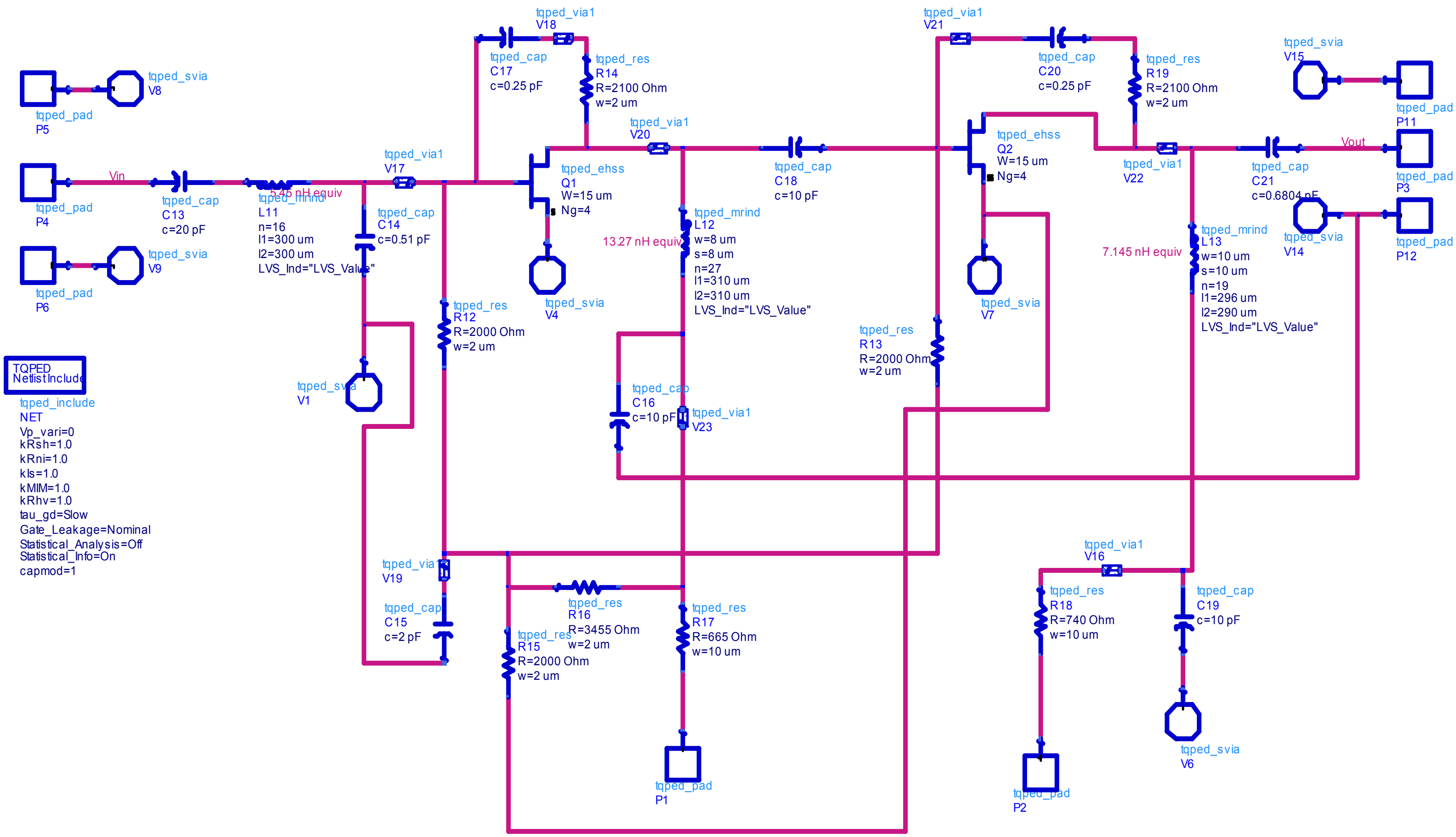
Noise Figure	< 4dB	3dB	2.258 dB
Gain Ripple	+/-1dB		+/-1dB
Input/Output VSWR	1.5:1		Input VSWR: 1.78:1 Output VSWR: 1.01:1
Voltage Supply	3.3V		3.3V
Power Dissipation	10mW per stage		16.96mW two stage Amp
Size/ Packaging	60 X 60 mil Chip		60 X 60 mil Chip

Trade Offs/ Optimization

Many trade offs in the design were required even in the early stages. While stabilizing the FET in the design, we had many choices including using series or shunt resistors as well as an inductor between the FET source and ground. Unfortunately all of these forced us to drop voltage across resistors and thus increase the power consumption of the amplifier drastically. In order to avoid this, a feedback structure was used using a resistor and capacitor in series between the gate and drain of the FET. The downside of the feedback stability method was the additional noise that would be "fed back" to the input of the LNA. Fortunately after finishing the design, the noise figure increased only slightly and was well below the 3dB requirement.

The other major trade off dealt with the bias structure in the amplifier. Originally the LNA required 4 separate voltage supply inputs of +0.5V and +1.5V (2 each). The design became unstable if the voltage inputs were connected together on chip. To overcome this design flaw, resistive dividers were added to the input of the voltage supply to serve a dual purpose. First the resistive dividers reduce the 3.3V input supply to the required 1.5V for the drain bias and second it taps off the 1.5V and reduces it to the required 0.5V gate bias. Using this method the number of supply voltages required was reduced to two inputs of +3.3V. The remaining two voltage supplies could have been combined on chip via a resistor, but after performing a preliminary layout the two voltage supplies were on opposite sides. This prohibited the combination of the last two voltage supplies on chip.

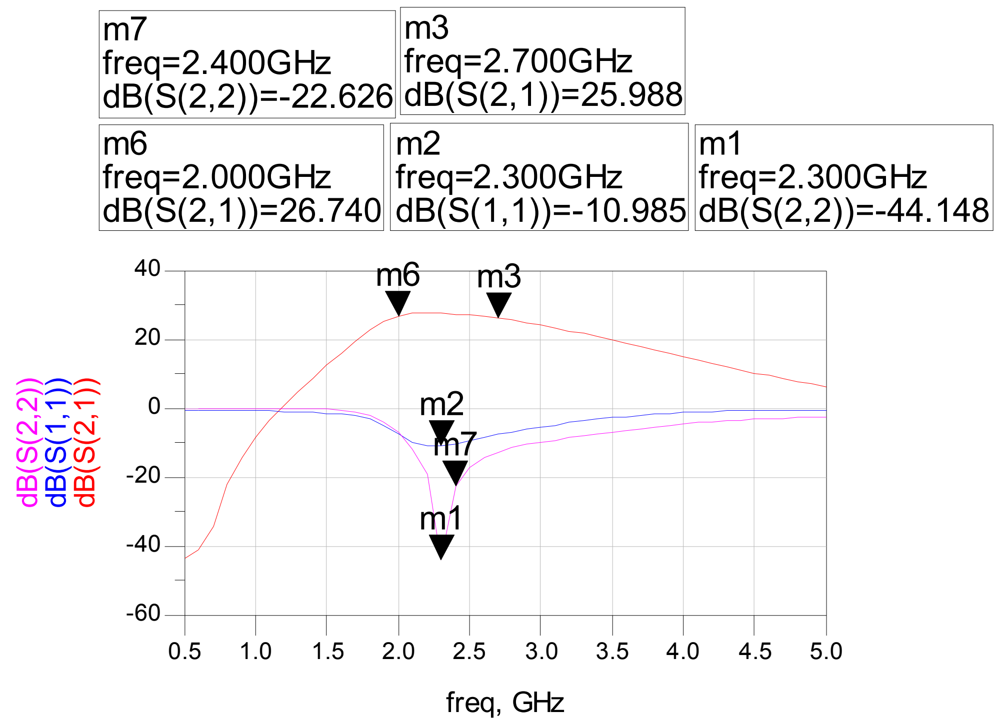
Schematic



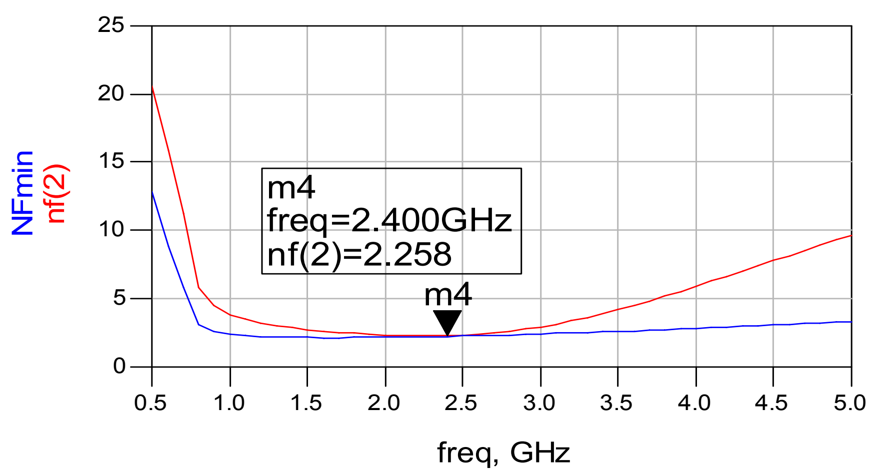
tqped_pad
P5
tqped_svia
V8
tqped_pad
P4
Vin
tqped_cap
C13
c=20 pF
tqped_mrind
L11
n=16
l1=300 um
l2=300 um
LVS_Ind="LVS_Value"
5.45 nH equiv
tqped_pad
P6
tqped_svia
V9
TQPED
Netlist Include
tqped_include
NET
Vp_vari=0
kRsh=1.0
kRni=1.0
kIs=1.0
kMIM=1.0
kRhv=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
capmod=1
tqped_svia
V1
tqped_cap
C14
c=0.51 pF
tqped_via1
V17
tqped_cap
C17
c=0.25 pF
tqped_via1
V18
tqped_res
R14
R=2100 Ohm
w=2 um
tqped_ehss
Q1
W=15 um
Ng=4
tqped_svia
V4
tqped_res
R12
R=2000 Ohm
w=2 um
tqped_via
V19
tqped_cap
C15
c=2 pF
tqped_res
R15
R=2000 Ohm
w=2 um
tqped_res
R16
R=3455 Ohm
w=2 um
tqped_via1
V20
tqped_mrind
L12
w=8 um
s=8 um
n=27
l1=310 um
l2=310 um
LVS_Ind="LVS_Value"
13.27 nH equiv
tqped_cap
C16
c=10 pF
tqped_via1
V23
tqped_res
R17
R=665 Ohm
w=10 um
tqped_pad
P1
tqped_cap
C18
c=10 pF
tqped_via1
V21
tqped_res
R13
R=2000 Ohm
w=2 um
tqped_ehss
Q2
W=15 um
Ng=4
tqped_svia
V7
tqped_cap
C20
c=0.25 pF
tqped_res
R19
R=2100 Ohm
w=2 um
tqped_via1
V22
tqped_mrind
L13
w=10 um
s=10 um
n=19
l1=296 um
l2=290 um
LVS_Ind="LVS_Value"
7.145 nH equiv
tqped_cap
C21
c=0.6804 pF
Vout
tqped_svia
V15
tqped_pad
P11
tqped_pad
P3
tqped_svia
V14
tqped_pad
P12
tqped_via1
V16
tqped_res
R18
R=740 Ohm
w=10 um
tqped_cap
C19
c=10 pF
tqped_svia
V6
tqped_pad
P2

Linear Simulations

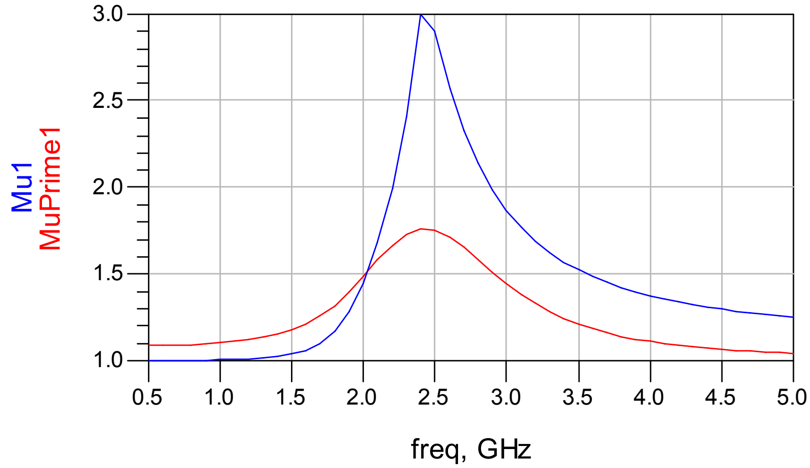
S_Parameters



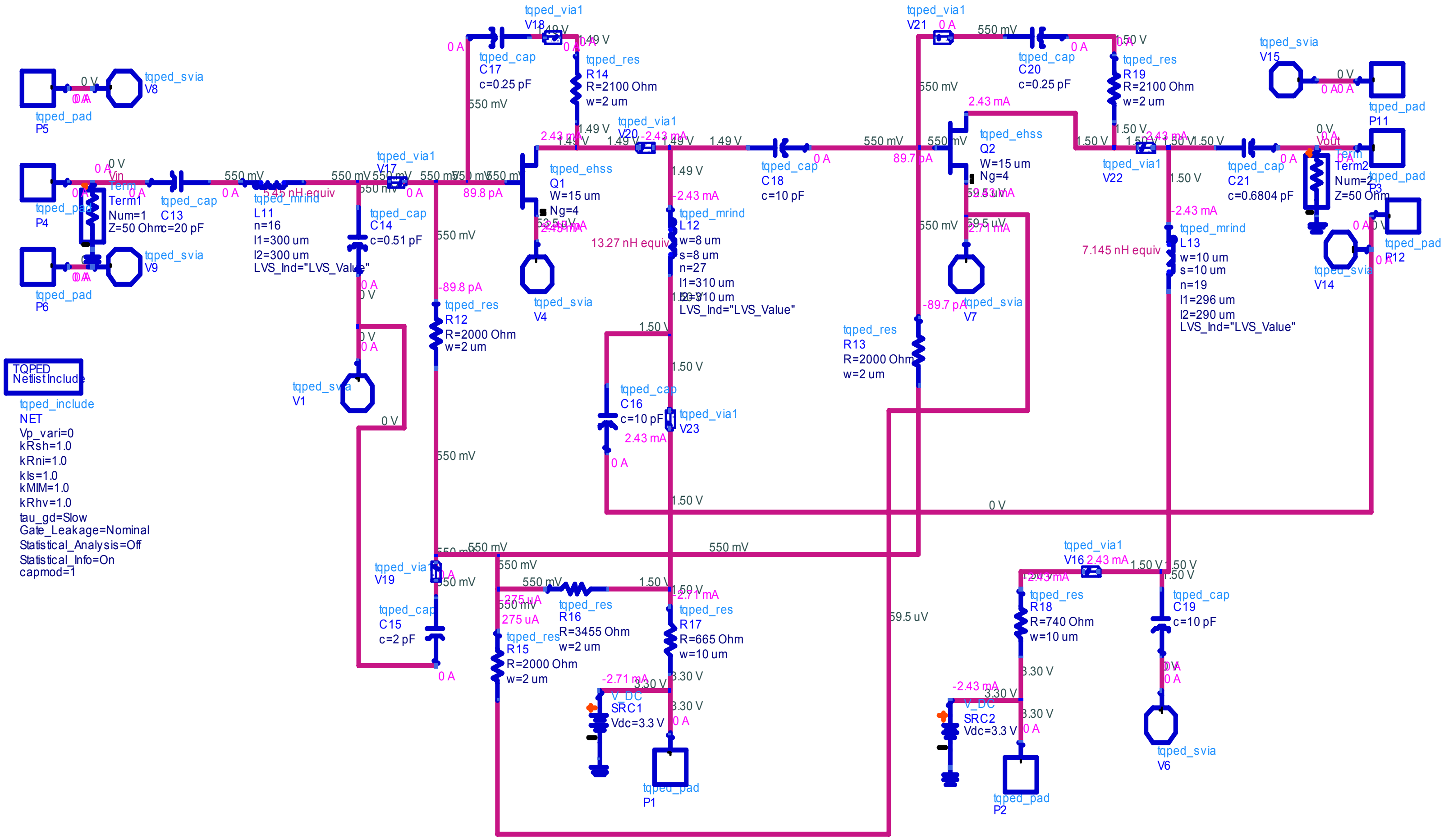
Noise Figure



Stability

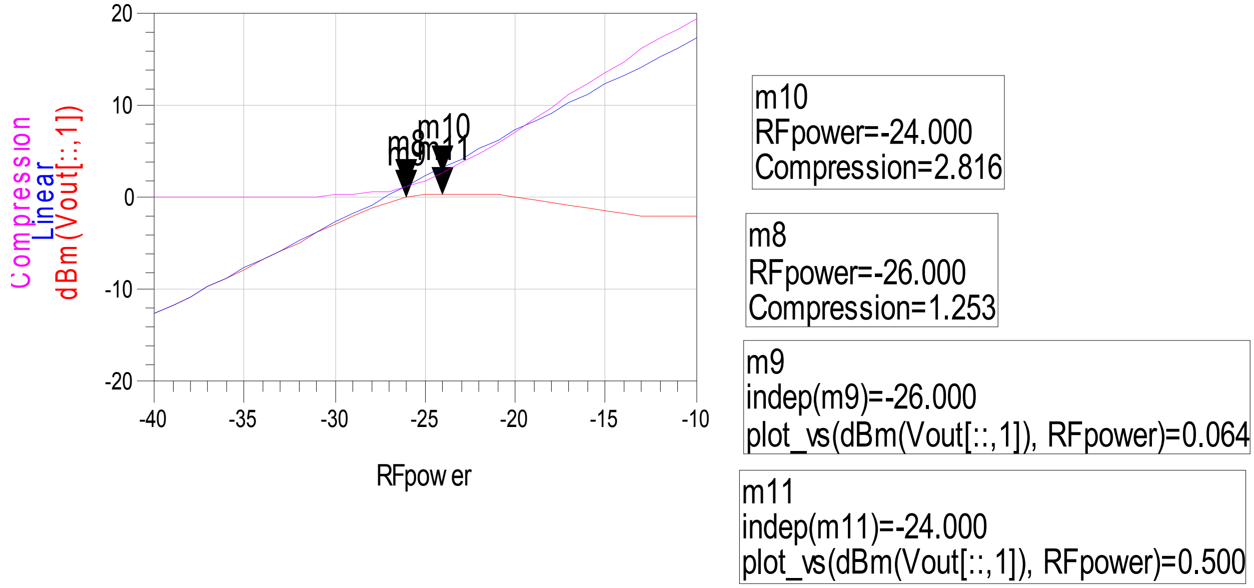


DC Annotation

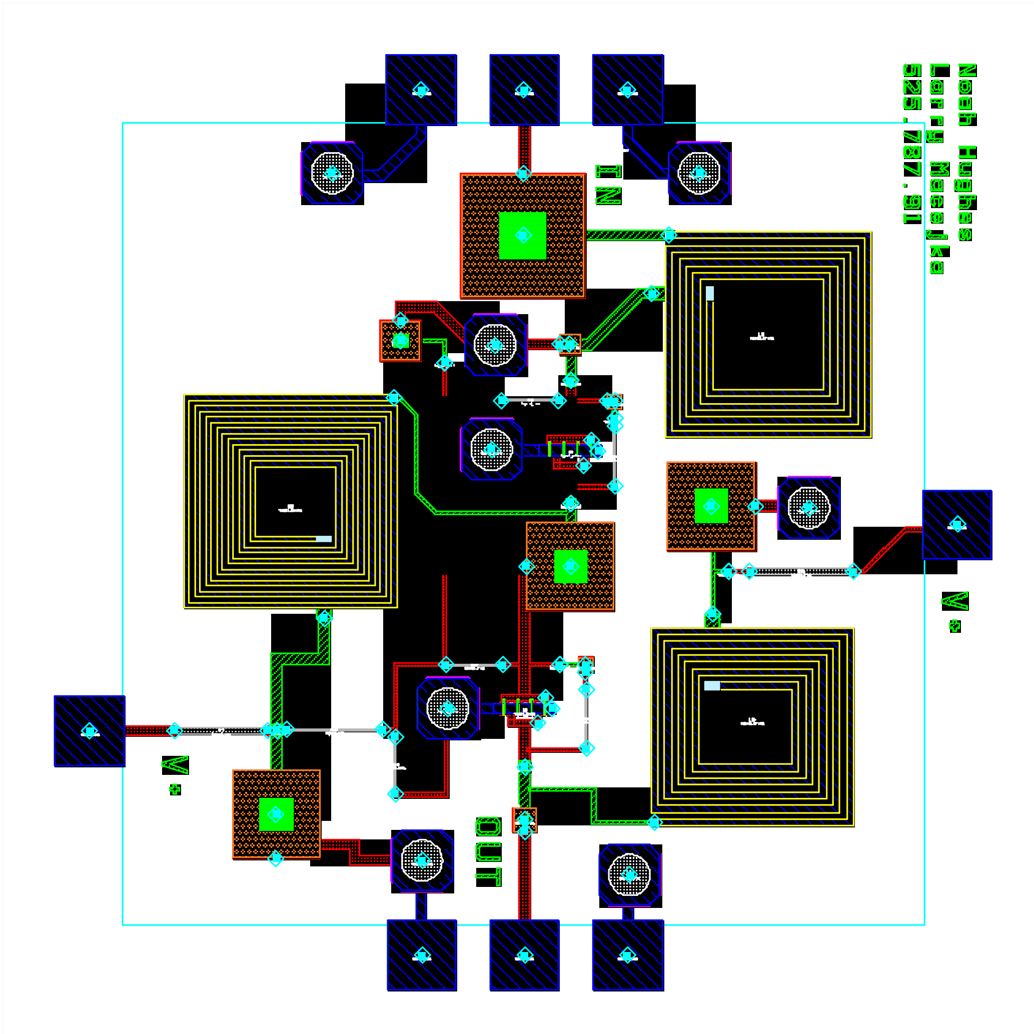


Non-Linear Simulation:

Power Output



Layout



Test Plan

The following test equipment is necessary to test the full extent of this Low Power LNA Design:

3.3V Power Supply with Needle Probe
Network Analyzer
Cables and Ground Signal Ground (GSG) Probes
Calibration Substrate for MMIC Testing
Noise Figure Meter
RF Signal Generator (capable of generating frequencies in 2-3 GHz range)
Power Meter or Spectrum Analyzer

Test Procedures

S-parameter Measurement

1.) Calibrate the network analyzer from 1 GHz to 10GHz.
2.) Connect the 3.3V needle probe to the DC pads on the MMIC labeled "V+". The order in which they are connected is not important.
3.) Slowly increase the voltage to 3.3V to determine that the amplifier is working correctly.
4.) Verify that the total current draw on the power supply is around 5.13 mA.
5.) Connect the input GSG Probes on the "IN" pads on the chip.
6.) Connect the output GSG Probes on the "OUT" pads on the chip.
7.) Measure the S-Parameter data measurements and save them to a disk.

Noise Figure Measurement

Using the configuration of the MMIC mentioned in the S-parameter measurement, proceed to do the following:

1.) Remove the SMA cable from the port labeled "OUT" on the GSG Probe.
2.) Connect the Noise Figure Meter to the SMA port on the GSG Probe.
3.) Remove the SMA cable from the port labeled "IN" on the GSG Probe.
4.) Connect the noise source to the GSG Probe on the "IN" side of the MMIC.
5.) Use the Noise Figure Meter to take a measurement.

Compression Point Measurement

Using the configuration of the MMIC mentioned in the Noise Figure Measurement, proceed to do the following:

1.) Remove the SMA cable from the port labeled "OUT" on the GSG Probe.
2.) Connect the Power Meter to the SMA port on the GSG Probe.
3.) Remove the SMA cable from the port labeled "IN" on the GSG Probe.
4.) Connect a signal generator to the GSG Probe on the "IN" side of the MMIC making sure that the RF output of the device is off or around –80 dBm.
5.) Set the signal generator to 2.4 GHz.
6.) Beginning at –40 dBm, sweep the power input at 1 dB steps. Measure the power output at each interval.
7.) Whenever the output does not increase by 1 dB with respect to the input power, you have reached the 1 dB compression point. Determining what exact value this compression point occurs at can be either done using interpolation or Microsoft Excel.

Conclusion

Testing the low power LNA should have at least 20dB gain. The gain flatness should be less than 1 dB over a band of 500 MHz measured from the center frequency (2305 to 2497 MHz). Also, the Input match should have around –10.9dB of loss at 2.4 GHz and the output match should have around -44dB of loss at 2.3 GHz. The power consumption should be somewhere around 16.96 mW (taking the measured current and multiplying it by the supply voltage).