

**The Johns Hopkins University
Whiting School of Engineering**

525.787 MMIC Design, Fall 2006

Instructors John Penn and Dr. Michel Reece

High Efficiency, Medium Power Amplifier

Peter L. Smith

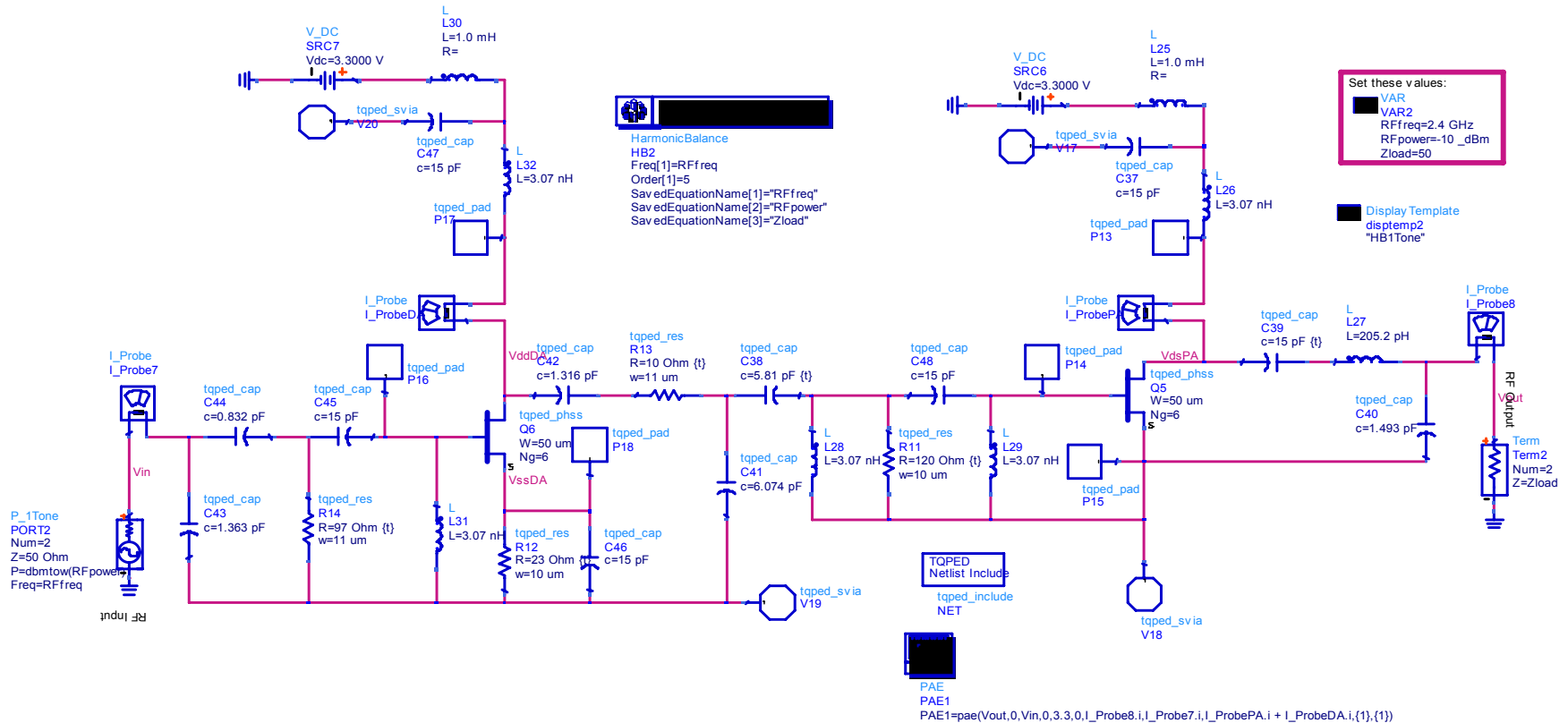
Introduction

- High efficiency, medium power amplifier using TriQuint 6x50 0.5 μ m Dmode PHEMTs (TQPED PHSS).
- On chip drain and gate bias networks, output matching network, and input matching networks
- The goal is efficiency to get the most RF output power for a given DC consumption (i.e. battery life).

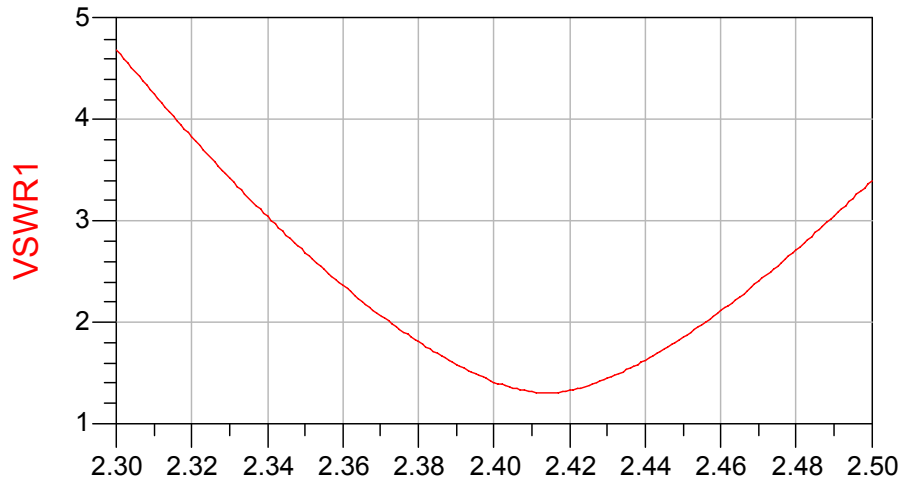
Design Approach

- 2 stages amplifier
- Step 1, design the output stage = power amp, biased at approximately $I_{\max}/2$ (~ 55 mA)
- Step 2, design the 2nd stage = driver amp, biased to attain spec ($\sim 15\text{--}20\%$ I_{dss})
- Step 3, put the two stages together
 - simplify the inter-stage topology
 - tune parameters to maximize PAE (particularly the driver amp source to ground resistor)

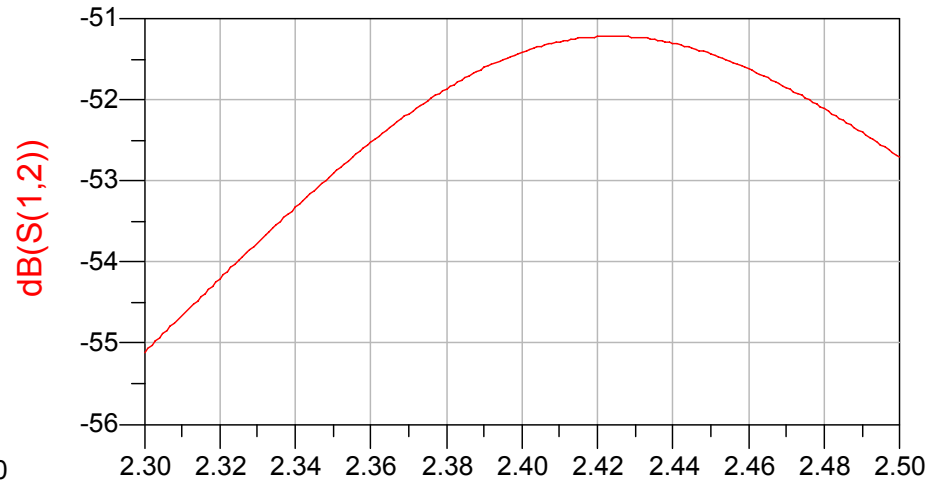
Two Stage Power Amp Schematic



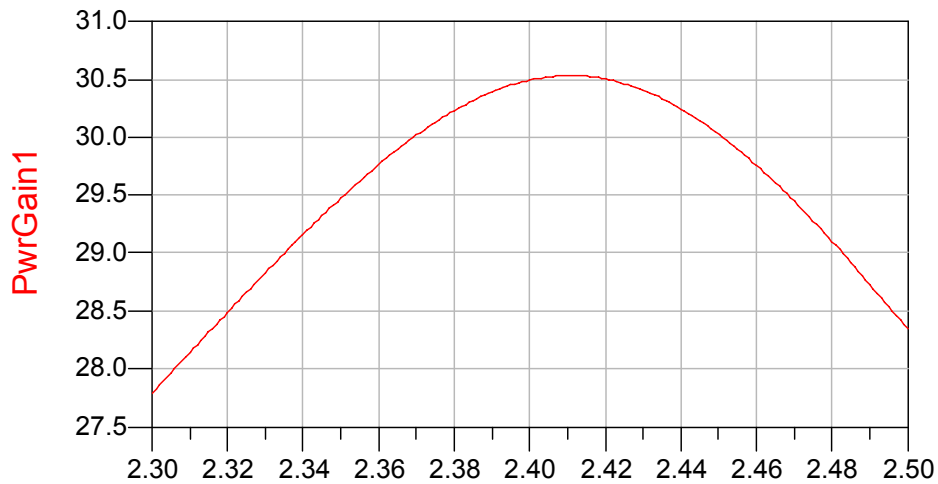
Two Stage Power Amp Voltage Domain Simulation



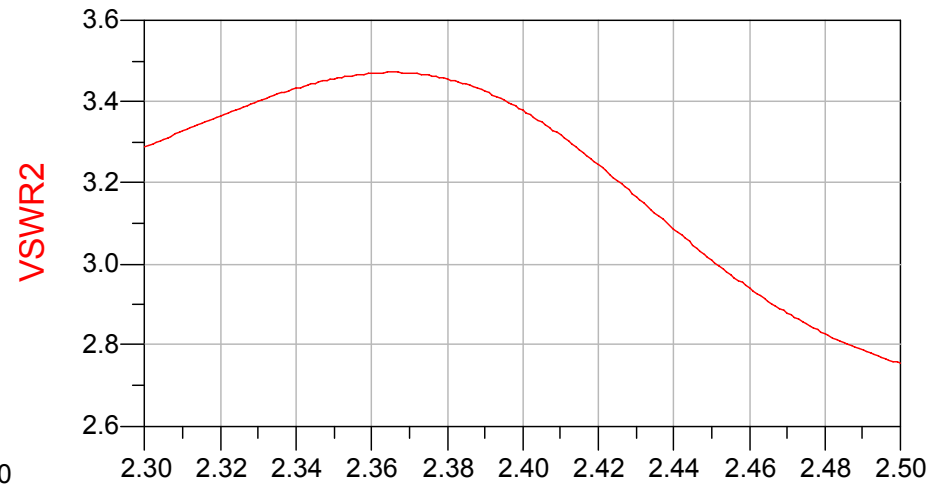
freq, GHz



freq, GHz

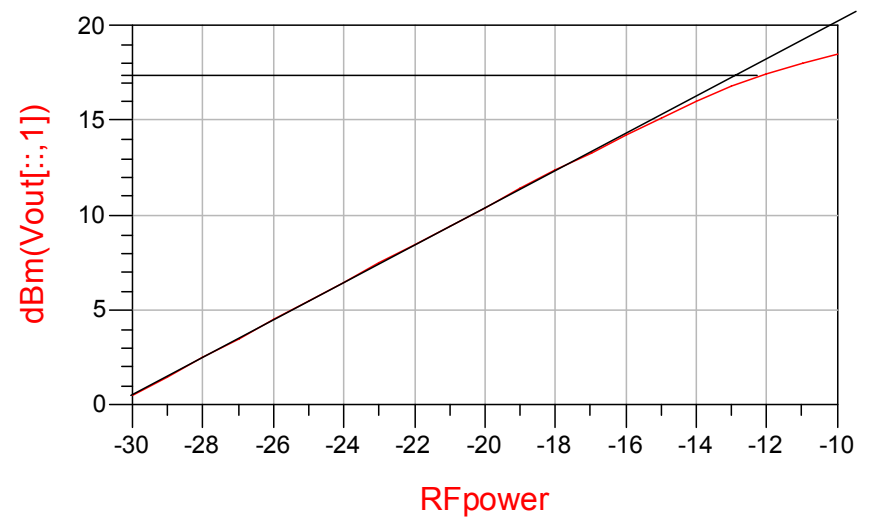
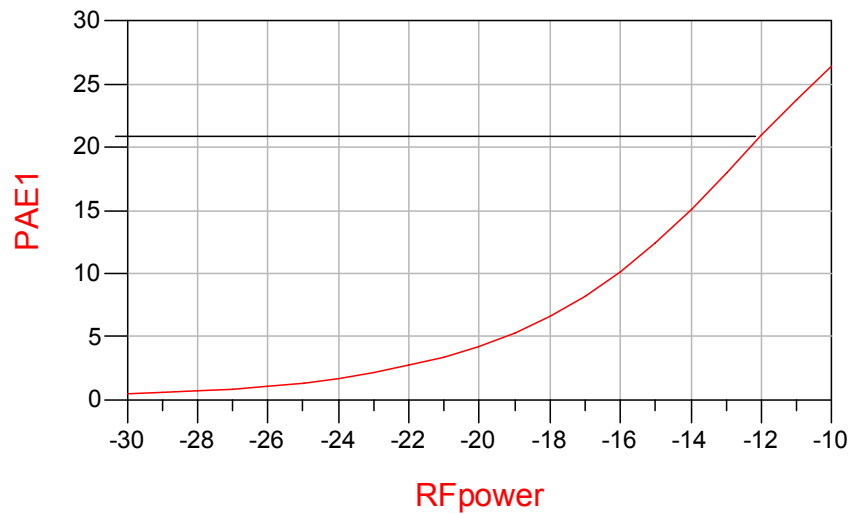
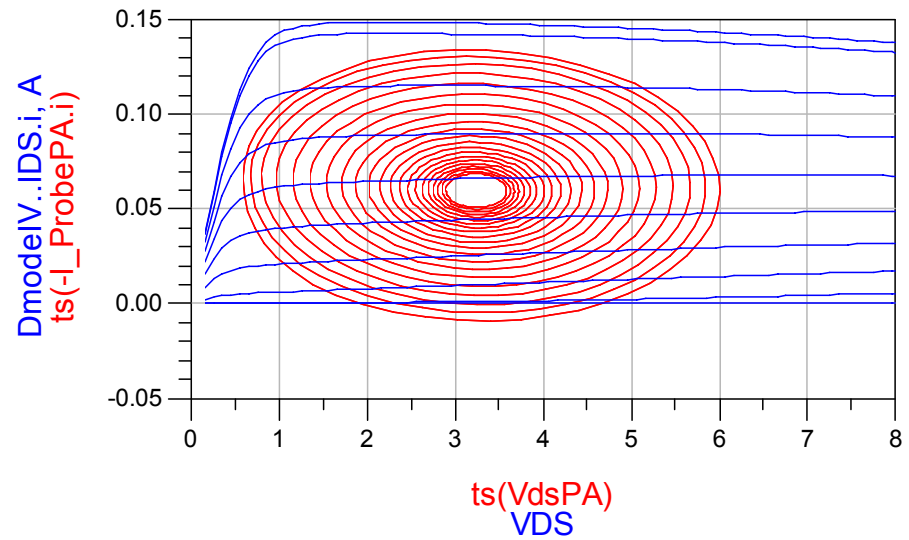
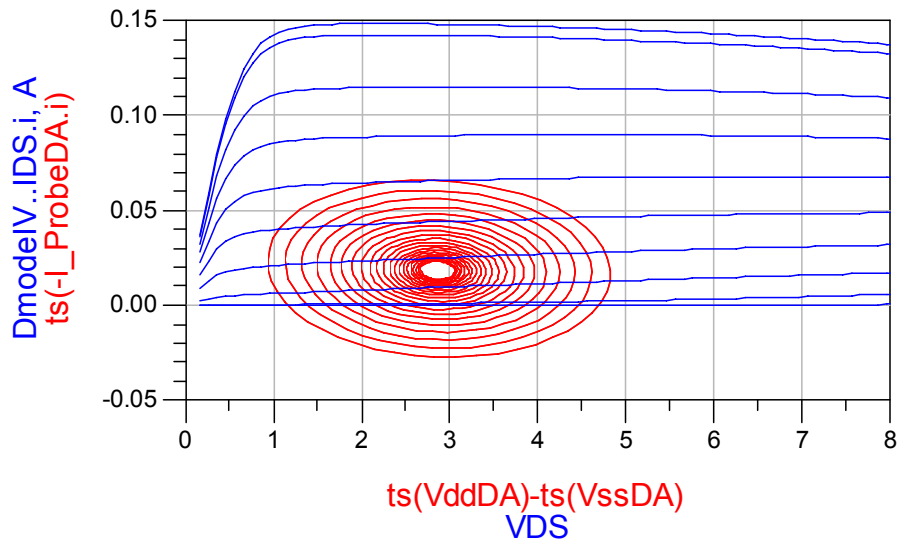


freq, GHz

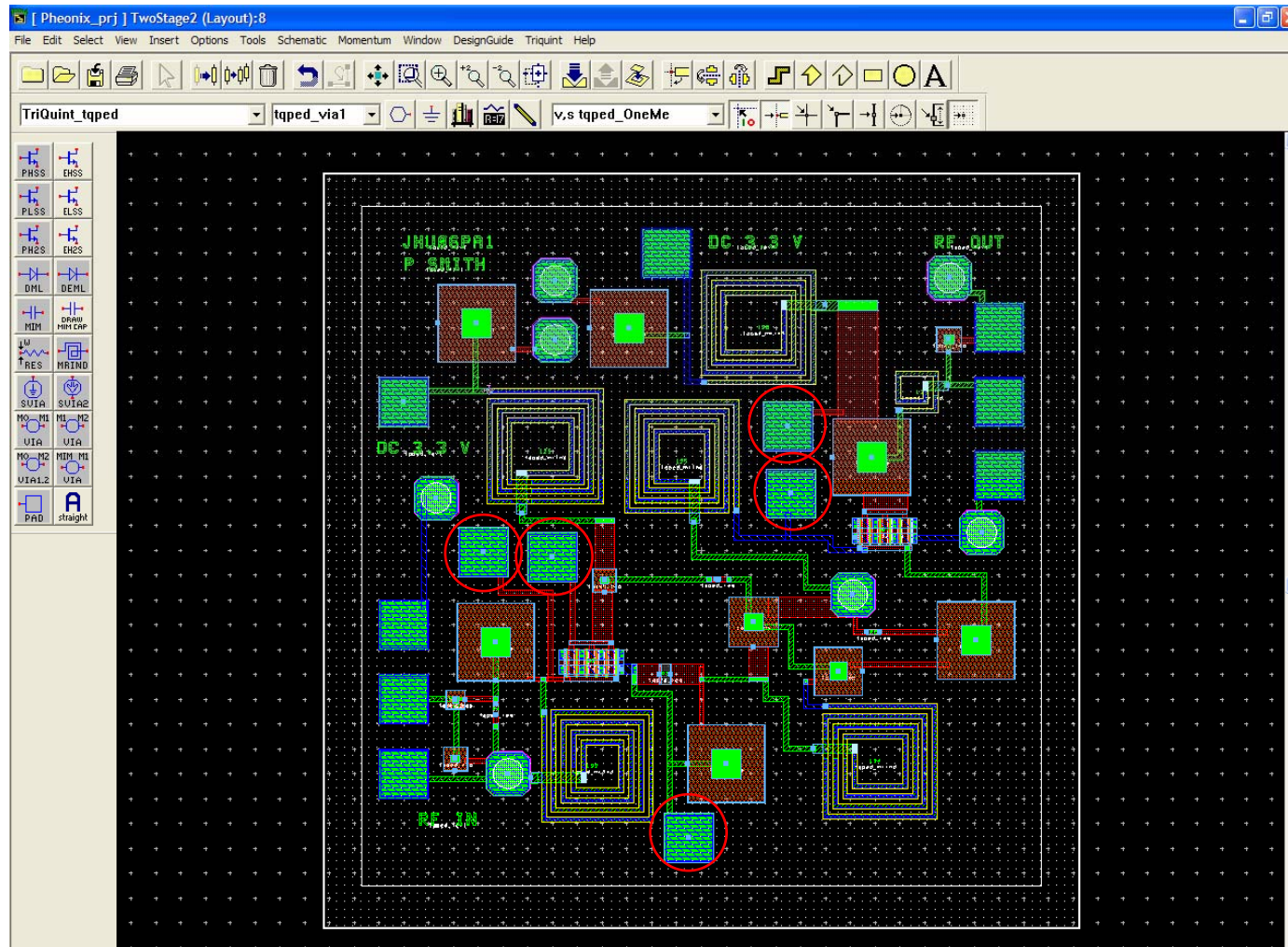


freq, GHz

2 Stage Power Amp Power Domain Simulation



2 Stage Power Amp Layout



Lessons Learned and Things I Would Have Done If I Had More Time

1. In the next stage of development we'll combine the two DC sources into one DC source. Currently, when I do this, the design becomes extremely unstable.
2. I need to consider another method of minimizing gain ripple.
3. I would like to vary the various parameters, such as input voltage, capacitance values, inductance values, resistance values, in order to test for sensitivity.
4. I would like to implement the microstrip to get a better estimate of performance.
5. I would like to try the Emode transistor.
6. I would like to find a better biasing scheme.

Conclusion

- A high efficiency, medium power amplifier was designed using TriQuint 6x50 0.5 μ m Dmode PHEMTs (TQPED PHSS).
- On chip drain and gate bias networks, output matching network, and input matching networks were implemented.
- The goal was maximum efficiency to get the most RF output power for a given DC consumption (i.e. battery life).

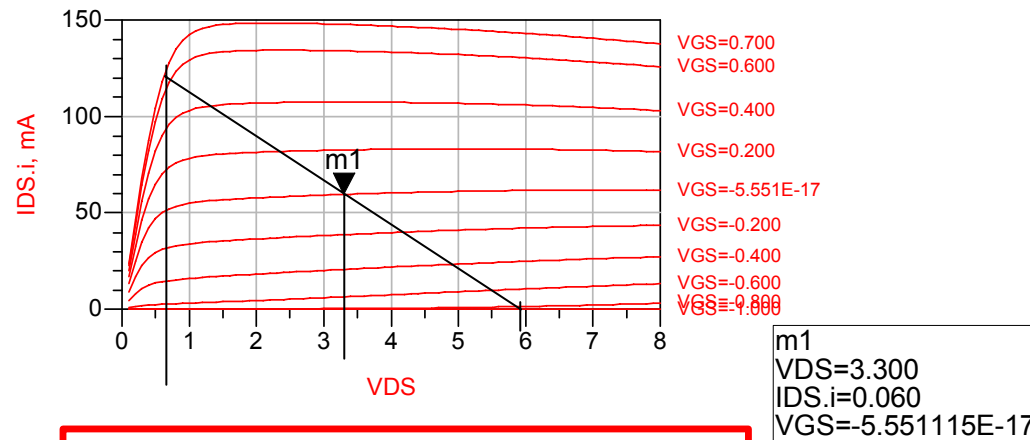
Table 1. Summary of Two Stage Power Amp Performance

	Desired	Attained
REQUENCY	2.305-2.497 GHz	2.305-2.497 GHz
GAIN	threshold 18 dB, objective 20 dB	30.5 dB peak, 28.8 dB min
GAIN RIPPLE	0.5 dB	2.5 dB
OUTPUT POWER	TBD	17 dBm, 1 dB compression
PAE	threshold 20% @ 1 dB, objective 25% @ 1 dB	21%
VSWR, 50 Ω	1.5:1 input & output	4.8 max input, 3.5 max output
SUPPLY VOLTAGE	+3.3 V signal voltage supply at, goal (3 to 3.6 V range)	+3.3 V

BACKUP

Power Amp Bias

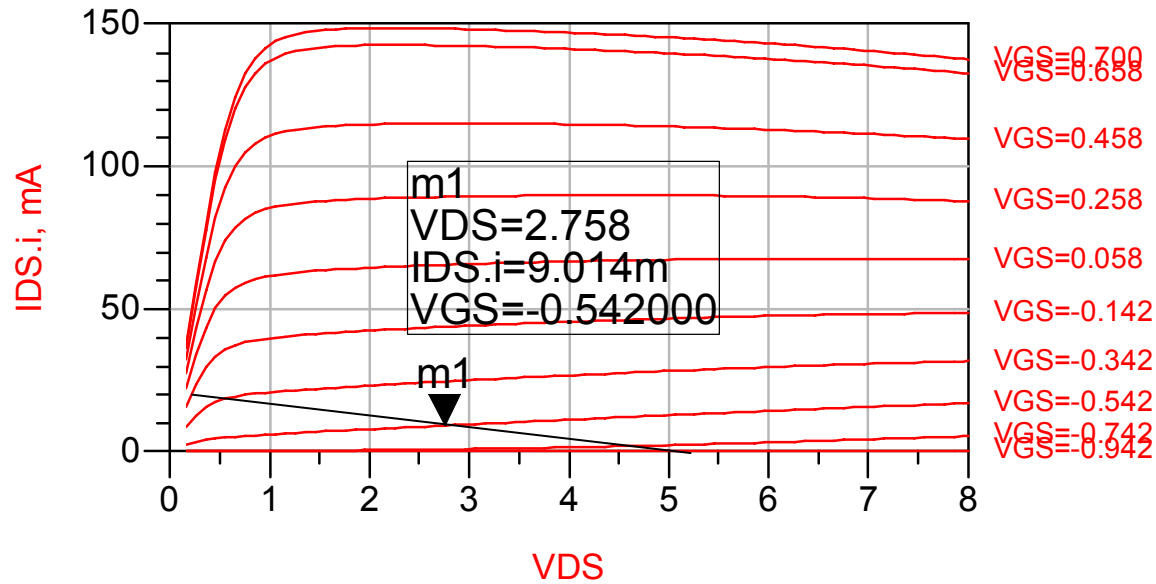
Setting V_{ds} to 3.3 V we see in Figure (1) that V_{gs} equal 0 V is a reasonable bias point. It also has the advantage of very simple bias circuitry.



Values at bias point indicated by marker m1.
 Move marker to update.

VDS	Device Power Consumption, Watts
3.300	0.196

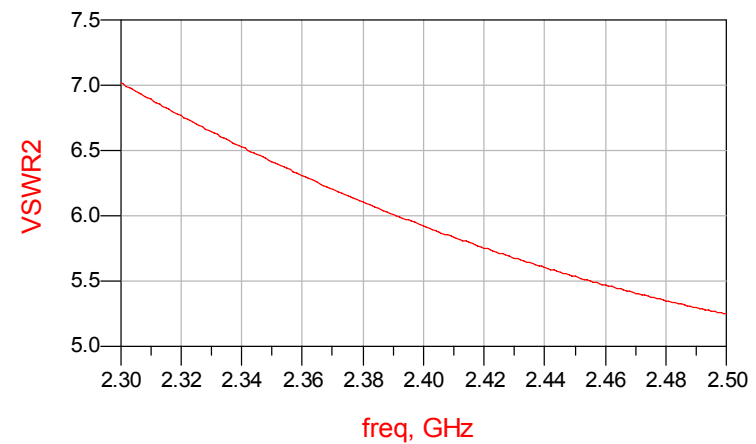
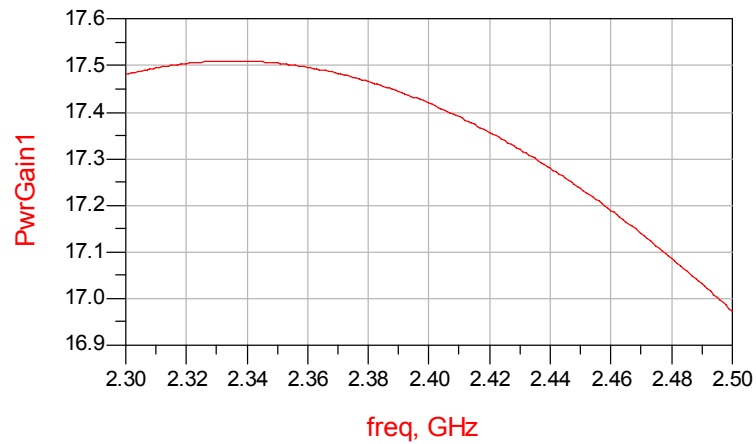
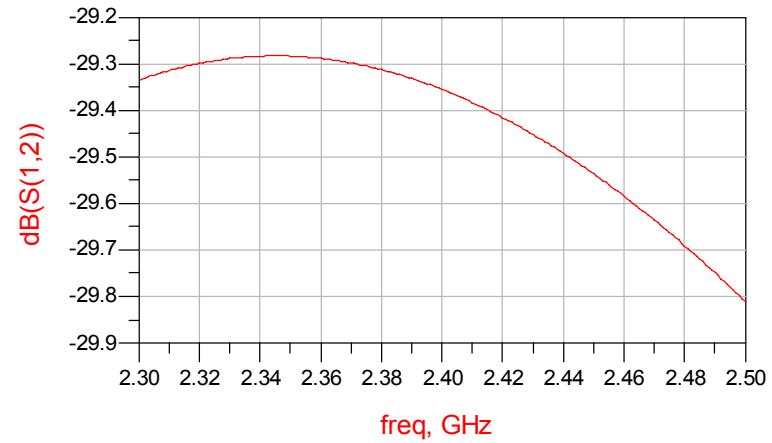
Driver Amp Bias



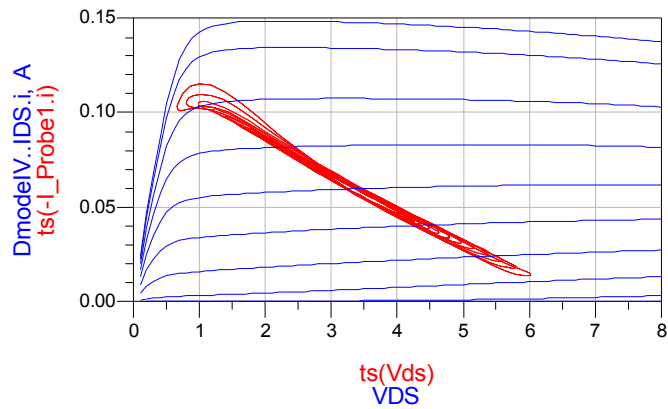
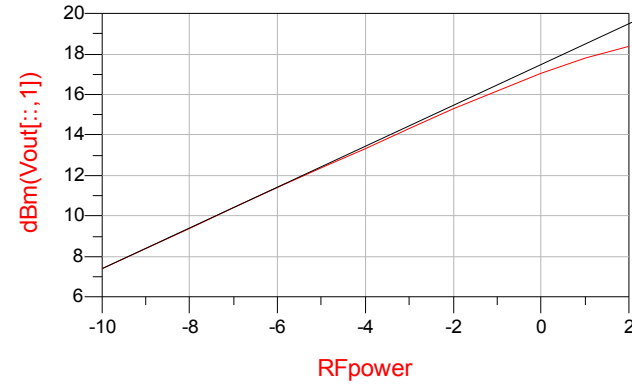
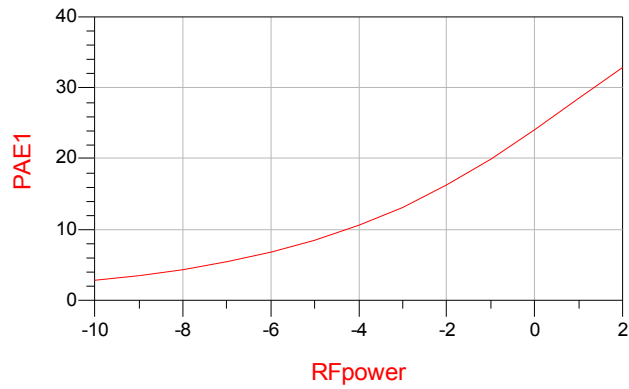
Values at bias point indicated by marker m1.
Move marker to update.

VDS	Device Power Consumption, Watts
2.758	0.025

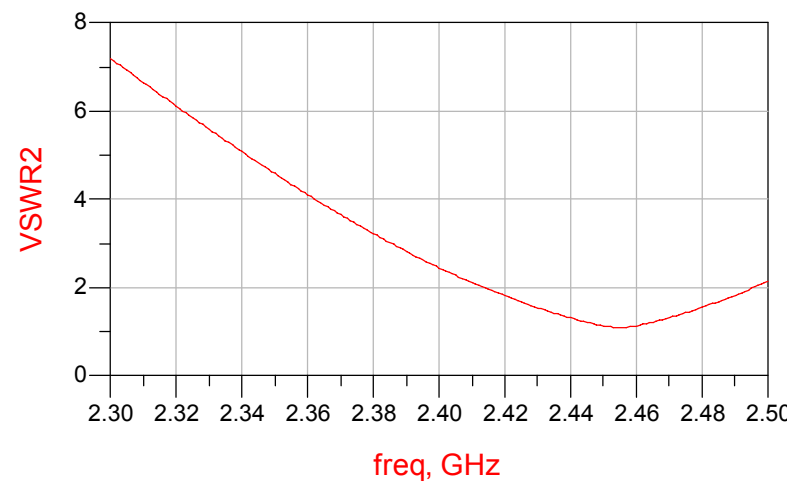
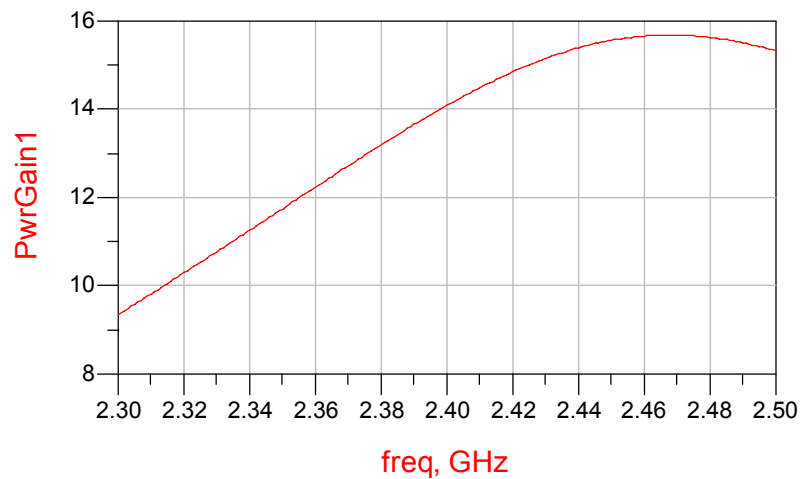
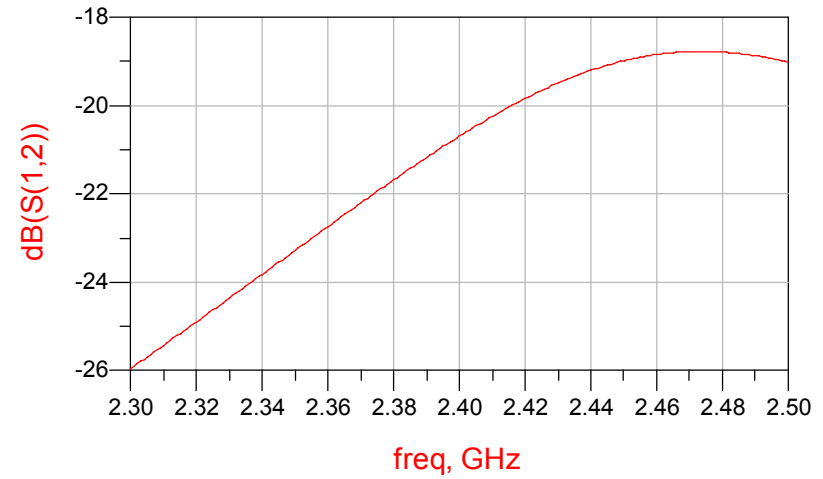
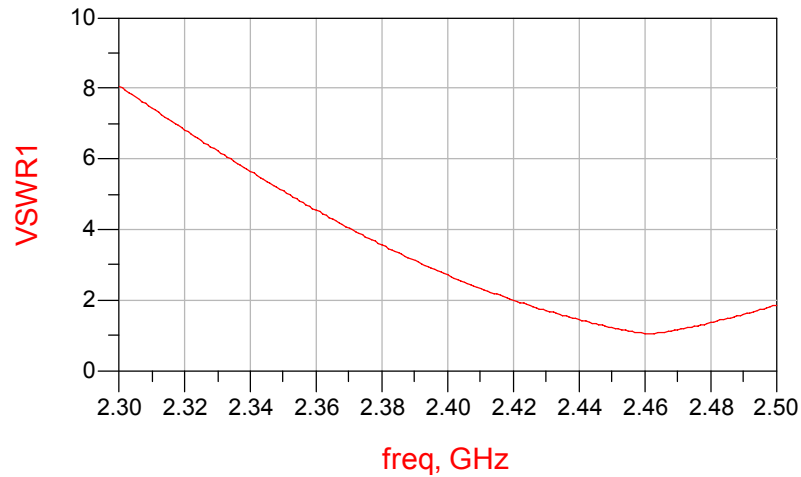
Voltage Domain Performance of the Power Amp



Power Domain Performance of the Power Amp



Voltage Domain Performance for the Driver Amp



Power Domain Performance for the Driver Amp

