

**The Johns Hopkins University  
Whiting School of Engineering**

*525.787 MMIC Design, Fall 2006*

Instructors John Penn and Dr. Michel Reece

High Efficiency, Medium Power Amplifier

Peter L. Smith

## Table of Contents

<b>1. Abstract</b>	<b>3</b>
<b>2. Introduction</b>	<b>3</b>
<b>3. Design Approach</b>	<b>4</b>
<b>3.1. Power Amp</b>	<b>4</b>
<b>3.1.1. Determine Bias Point, PAE, and RCripps</b>	<b>4</b>
<b>3.1.2. Add Bias Circuitry</b>	<b>5</b>
<b>3.1.3. Stabilize</b>	<b>5</b>
<b>3.1.4. Matching Network</b>	<b>6</b>
<b>3.2. Driver Amp</b>	<b>8</b>
<b>3.2.1. Determine Bias Point</b>	<b>8</b>
<b>3.2.2. Add Bias Circuitry</b>	<b>9</b>
<b>3.2.3. Stabilize</b>	<b>9</b>
<b>3.2.4. Matching Network</b>	<b>10</b>
<b>4. High Efficiency Medium Power Amplifier</b>	<b>12</b>
<b>4.1. Schematic</b>	<b>13</b>
<b>4.2. Simulations</b>	<b>14</b>
<b>4.3. Layout</b>	<b>16</b>
<b>4.4. Test Plans</b>	<b>16</b>
<b>5. Lessons Learned, Summary</b>	<b>17</b>
<b>6. Conclusion</b>	<b>17</b>

## Table of Figures and Tables

<b>Figure 1.</b> Dmode FET IV Curves with Power Amp Bias	<b>4</b>
<b>Figure 2.</b> PA Bias Circuitry	<b>5</b>
<b>Figure 3.</b> Power Amp Schematic	<b>6</b>
<b>Figure 4.</b> Voltage Domain Performance of the Power Amp	<b>7</b>
<b>Figure 5.</b> Power Domain Performance of the Power Amp	<b>7</b>
<b>Figure 6.</b> Bias and Load Line for the Driver Amp	<b>8</b>
<b>Figure 7.</b> Driver Amp Bias Circuitry	<b>9</b>
<b>Figure 8.</b> Driver Amp Schematic	<b>10</b>
<b>Figure 9.</b> Voltage Domain Performance of the Driver Amp	<b>11</b>
<b>Figure 10.</b> Power Domain Performance of the Driver Amp	<b>12</b>
<b>Figure 11.</b> Two Stage Power Amp Schematic	<b>13</b>
<b>Figure 12.</b> Voltage Domain Performance of the Amp 2 Stage	<b>14</b>
<b>Figure 13.</b> Power Domain Performance of the 2 Stage Amp	<b>15</b>
<b>Figure 15.</b> 2 Stage Power Amp Layout	<b>16</b>
<b>Table 1.</b> Summary of Two Stage Power Amp Performance	<b>17</b>

## 1. Abstract

This paper describes the design and simulated performance of a two stage power amp. The simulation was performed using ADS. The associated layout is also provided. The critical design parameter is power added efficiency (PAE). A PAE of 21% was attained.

## 2. Introduction

Design a high efficiency, medium power amplifier using TriQuint 6x50 0.5 $\mu$ m Dmode PHEMTs (TQPED PHSS). Use on chip drain and gate bias networks, output matching network, and input matching network. The goal is efficiency to get the most RF output power for a given DC consumption (i.e. battery life). Try to attain the following specified values.

REQUENCY: 2.305-2.497 GHz

GAIN, small signal: threshold 18 dB, objective 20 dB

GAIN RIPPLE:  $\pm 0.5$  dB max

OUTPUT POWER: > TBD

POWER ADDED EFFICIENCY: > threshold 20 % @ 1 dB compression,  
objective 25 % @ 1 dB compression

VSWR, 50  $\Omega$ : < 1.5:1 input & output

SUPPLY VOLTAGE: signal voltage supply at +3.3 V, goal (3 to 3.6 V range)

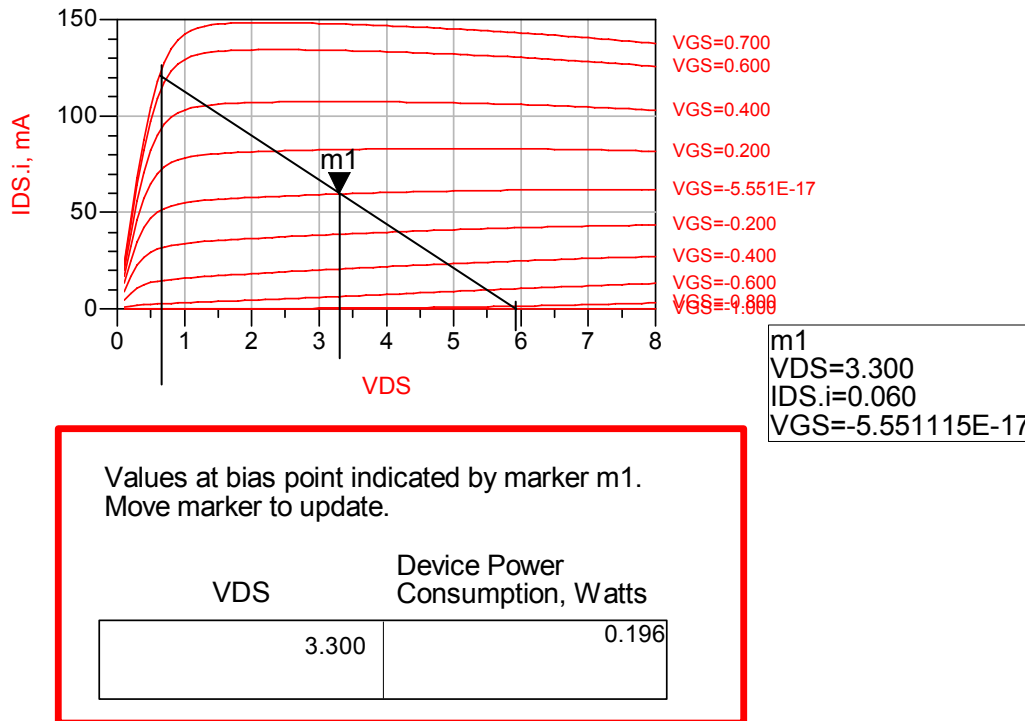
### 3. Design Approach

The overarching design strategy will be to use two stages. We'll begin by designing the output stage, biased at approximately  $I_{\max}/2$  (~ 55 mA). This will be the power amp. Next we'll add a second stage biased to attain spec (~ 15–20%  $I_{\text{dss}}$ ). This will be the driver amp. Finally we'll put the two stages together and simplify the inter-stage topology as much as possible.

#### 3.1. Power Amp

##### 3.1.1. Determine Bias Point, PAE, and RCripps

Setting  $V_{\text{ds}}$  to 3.3 V we see in Figure (1) that  $V_{\text{gs}}$  equal 0 V is a reasonable bias point. It also has the advantage of very simple bias circuitry.

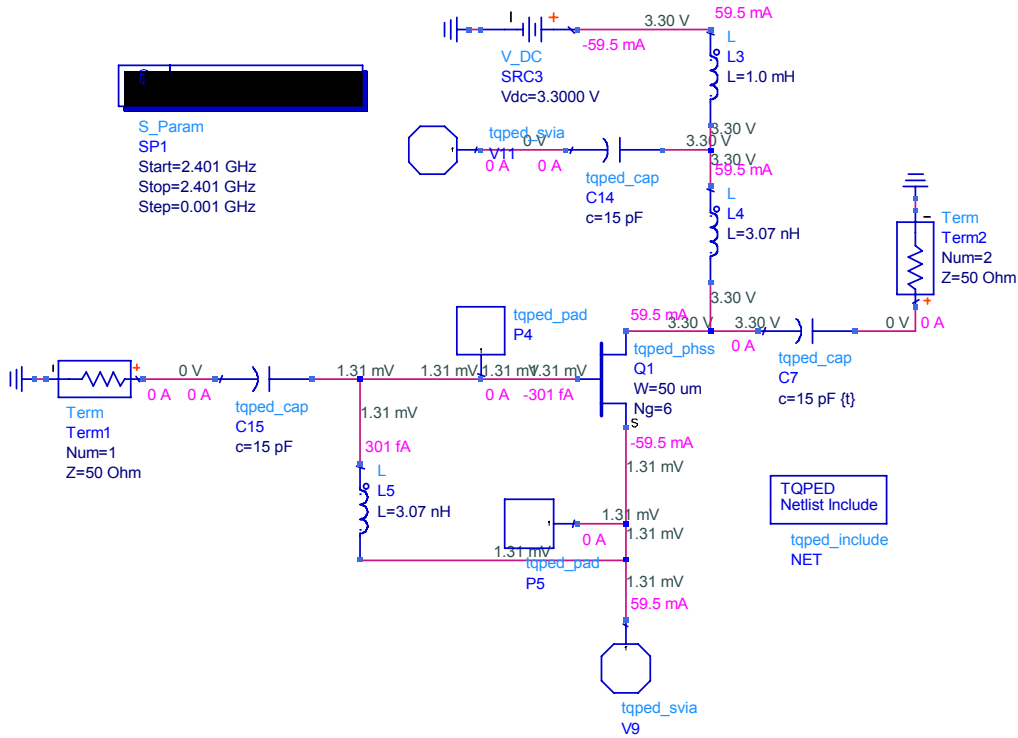


**Figure 1.** Dmode FET IV Curves with Power Amp Bias

From the load line we see that  $\Delta V_{\text{DS}}$  is  $2 \times (3.3 - 0.65) \text{V} = 5.2 \text{V}$  and  $\Delta I_{\text{DS}}$  is about 120 mA. So the RF output power should be around 78 mW. The device power consumption is 196 mW, giving a Power Added Efficiency (PAE) of approximately 39%.  $R_{\text{cripps}}$  is given by  $\Delta V_{\text{DS}} / \Delta I_{\text{DS}}$  which equals  $43.3 \Omega$ .

### 3.1.2. Add Bias Circuitry

In the design of the bias circuits we want to use the largest inductance and capacitance feasible. For our application feasibility is determined by the percentage of chip area an element requires. After some bitter experience it is found that a 15 pF capacitor and 3 nH inductor are close to the larger end of what will fit on the square chip. (If we had more time we would have experimented with what fits on the largest chip, just to allow for the largest possible inductor and capacitor values; but that actually takes much more time than one would at first think – at least for a neophyte such as myself) This bias circuitry is illustrated in Figure (2).



**Figure 2.** PA Bias Circuitry

Note the pads will be used for testing the DC bias on the chip.

### 3.1.3. Stabilize

Using the tuner, we find that a 120 Ω shunt resistor on the input stabilizes the device from 0.1 GHz to 20 GHz.

### 3.1.4. Matching Network

We use “Cripps Method” to get the output matching circuit. The impedance looking into the output of the amplifier is equivalent to a 2.9 nH shunt inductor ( $L_{ds}$ ) in parallel with a 323  $\Omega$  shunt resistor ( $R_{ds}$ ), which gives a  $Z_{22}$  of  $5.866 + j43.159 \Omega$ . We want to resonate out the reactance and add a load resistance of  $R_{cripps}$  as determined in (3.1.1). Doing this causes the  $Z_{22}$  looking into the circuit to be  $21.976 - j21.648 \Omega$ . That is, we will use the Smith chart to select the circuit corresponding to the path going from  $21.976 + j21.648 \Omega$  to 50  $\Omega$  and which uses the most reasonable values while avoiding the edges of the Smith chart. Using the smith chart program we find that a 206.8 pH series inductor followed by a 1.502 pF shunt capacitor provide that Cripps output matching circuit. We place these in the ADS schematic and then find that  $Z_{11}$  is given by  $57.693 + j46.875 \Omega$ . We conjugate match this value. That is, design the input matching circuitry to map  $57.693 + j46.875 \Omega$  to 50  $\Omega$ . Doing this yields 1.223 pF shunt capacitor followed by a 3.172 nH series inductor. At the first pass, the output VSWR shows a problem. It is found to be 6.45. Changing the output match in order to lower the output VSWR to 1.5, results in an unacceptable PAE of around 1.5 %. Adding an output matching circuit results in a VSWR of at least 3.5 and decreases the PAE from around 30% to 15%. As PAE is the critical parameter, we’ll accept whatever VSWR we get and assume the chip is connected to an isolator on the output. With the 100 Ohm shunt resistor and matching circuitry we arrive at the power amp illustrated in Figure (3).

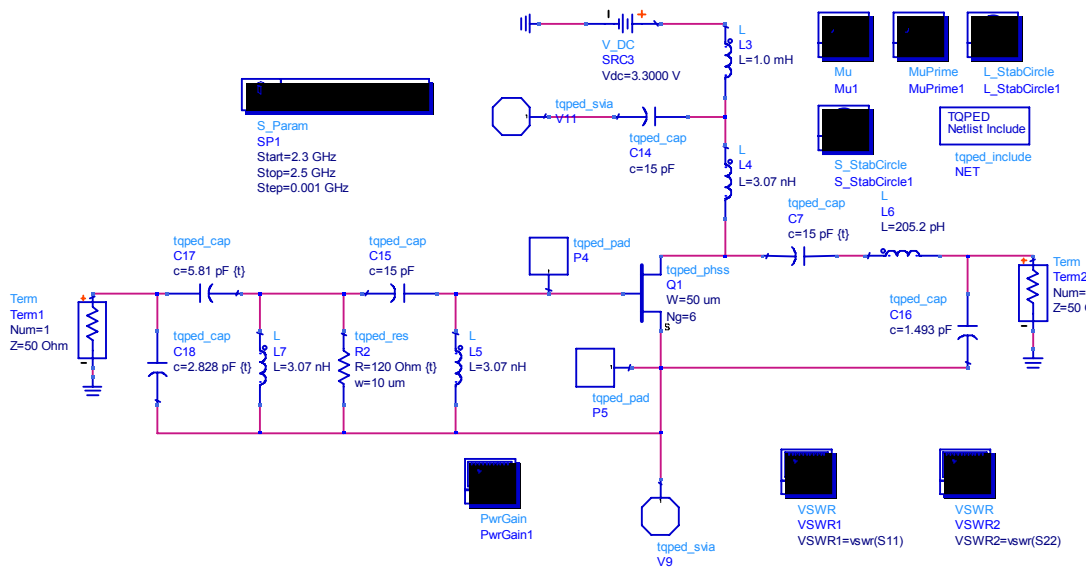
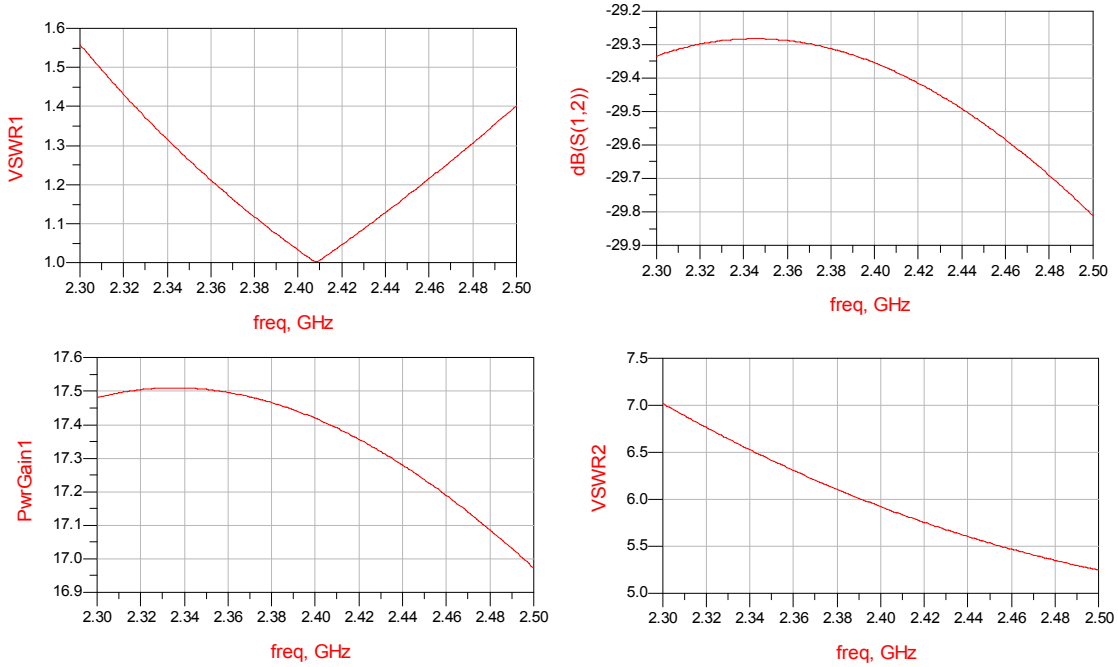


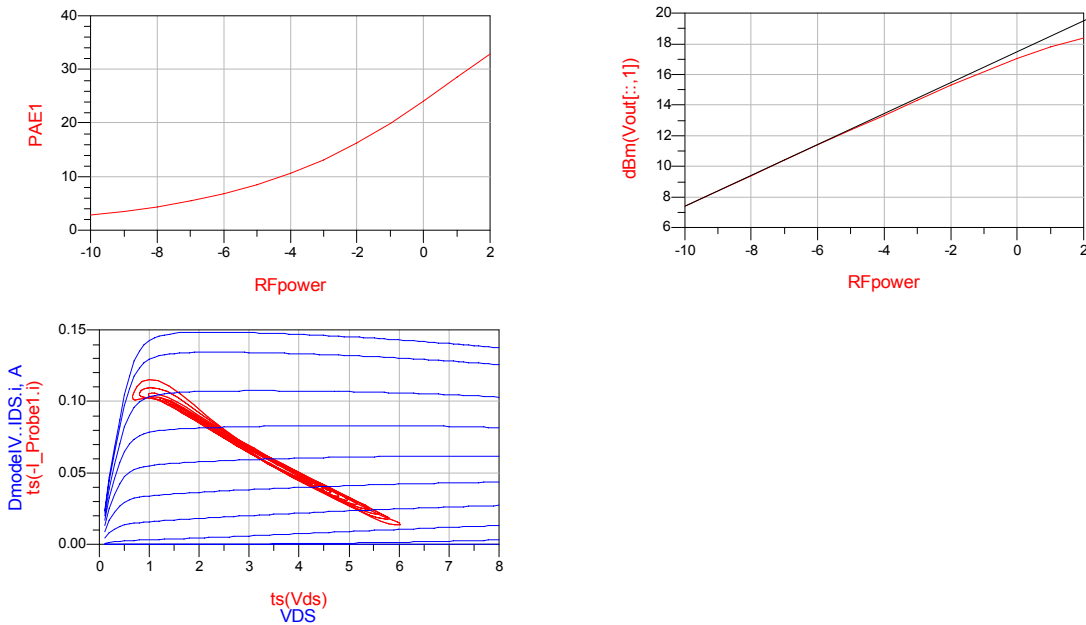
Figure 3. Power Amp Schematic

The VSWR, S12, and power gain are provided in Figure (4).



**Figure 4.** Voltage Domain Performance of the Power Amp

Note, VSWR1 is input VSWR and VSWR2 is output side VSWR (looking into the output). Note that we have insufficient gain, hence the need for the driver amp. The load line, power out, and PAE are provided in Figure (5).



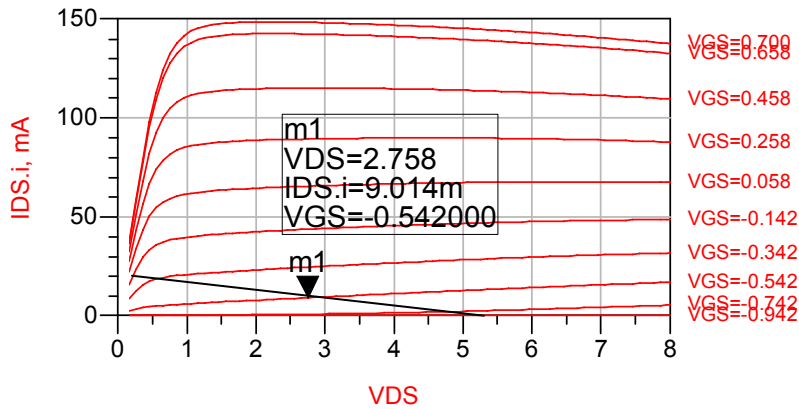
**Figure 5.** Power Domain Performance of the Power Amp

Note that the 1 dB of compression occur at approximately at 2 dBm RF power in. At this point RF power out is 18 dBm, and PAE is 31%. Thus, we would like the drive amp to be linear up until a little beyond 2 dBm, since we don't want it to compress before the power amp.

### 3.2. Driver Amp

#### 3.2.1. Determine Bias Point

For the driver amp we will seek gain with minimal DC power. This may be accomplished with the load line shown in Figure (6).



Values at bias point indicated by marker m1.  
 Move marker to update.

VDS	Device Power Consumption, Watts
2.758	0.025

**Figure 6.** Bias and Load Line for the Driver Amp

From the load line we see that  $\Delta V_{DS}$  is  $2 \times (2.758 - 0.25) V = 5.0 V$  and  $\Delta I_{DS}$  is about 20 mA. So the RF output power should be around 12.54 mW. The device power consumption is 25 mW.

### 3.2.2. Add Bias Circuitry

We will accomplish this bias with the circuitry illustrated in Figure (7).

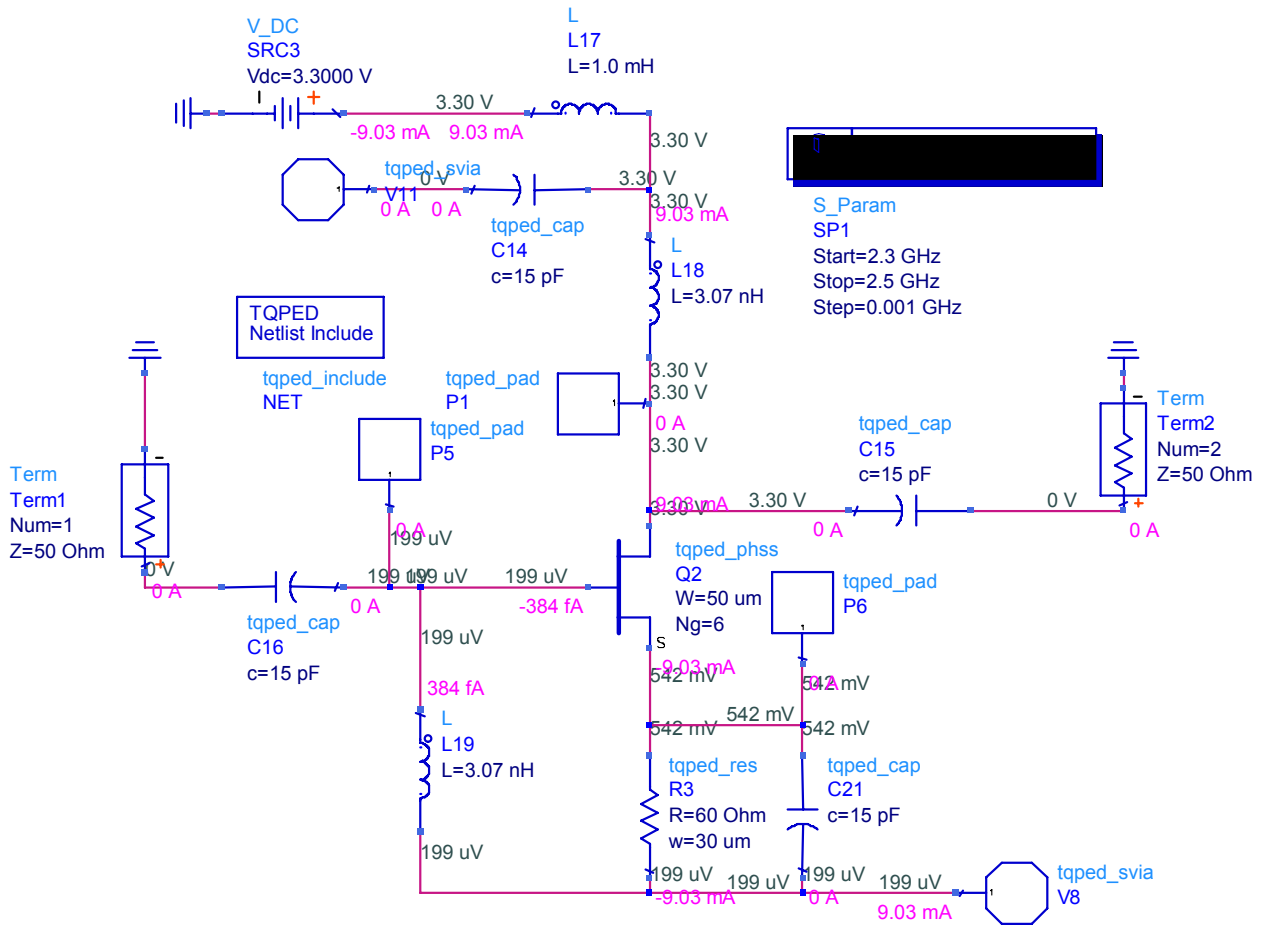


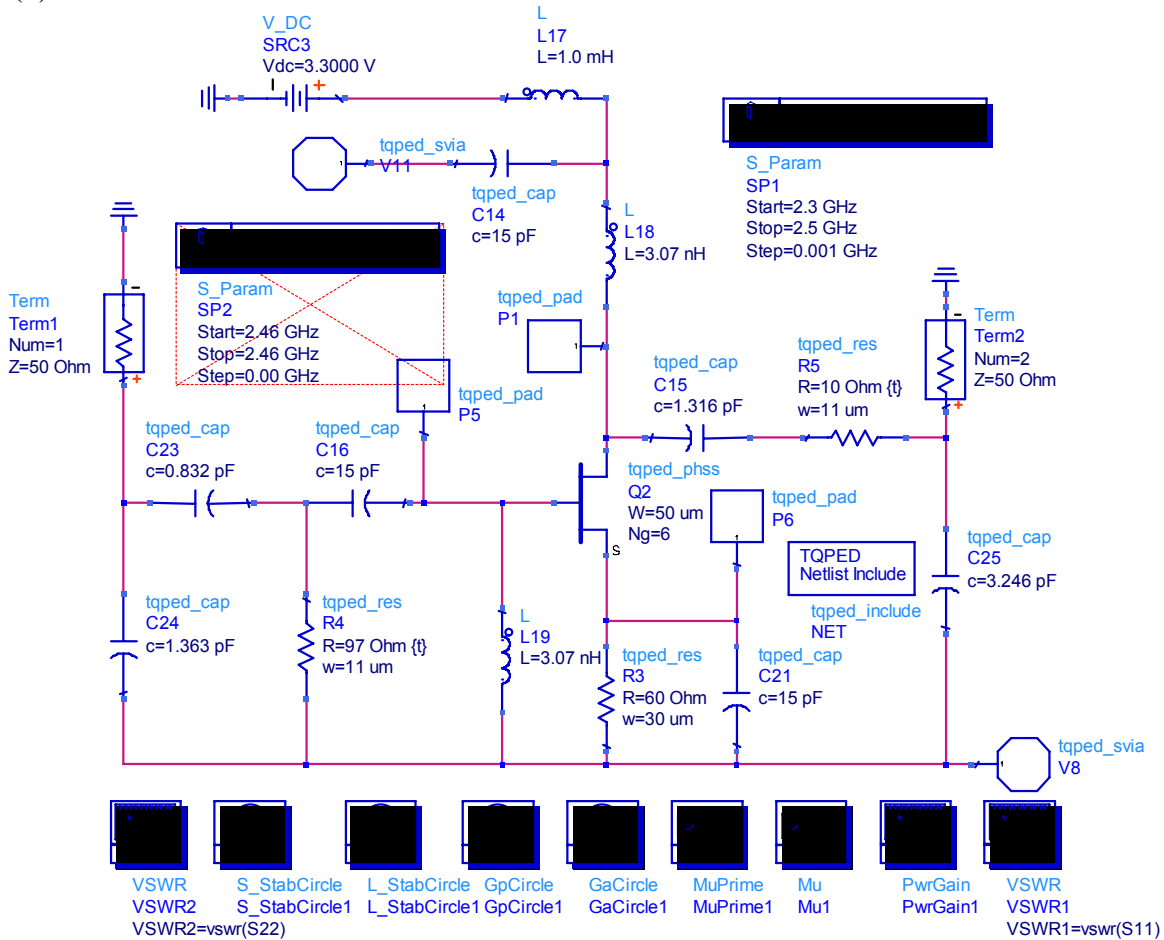
Figure 7. Driver Amp Bias

### 3.2.3. Stabilize

We will use two different stabilizing topologies. In the first topology a drain feed back consisting of a 15 pF capacitor and a 270 Ω resistor to stabilize the driver from 2.3 to 2.5 GHz. In the second a topology a 97 Ω shunt resistor on the gate and a 10 Ω series resistor on the drain.

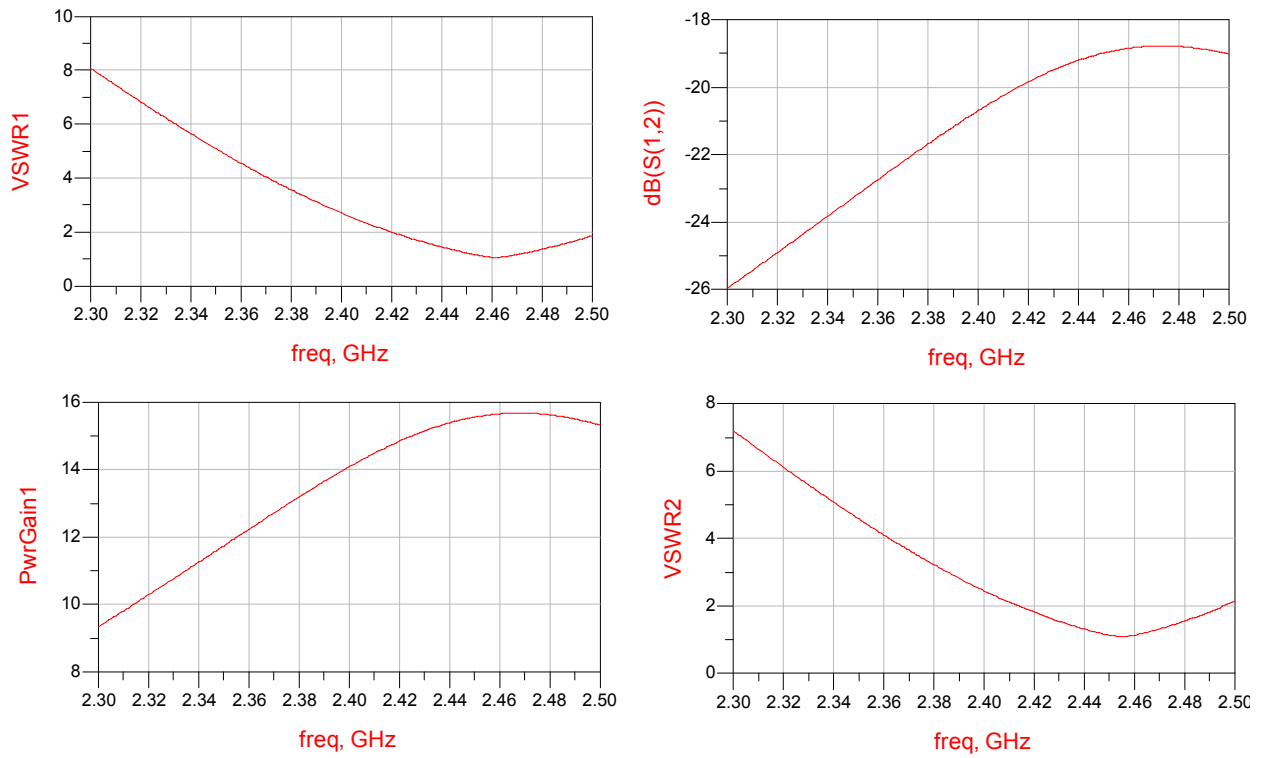
### 3.2.4. Matching Network

Notice that the gain for the power amp peaks at approximately 2.34 GHz. So we will design the driver amp to have peak gain at 2.46 GHz. The combined gain will then have less ripple over the band. As we are designing for maximum gain, we will conjugate match the input and output. For the input we will match the conjugate the center of the available gain circle to 50  $\Omega$ . For the output we will match the conjugate the center of the power gain circle to 50  $\Omega$ . The resulting circuit is illustrated in Figure (8).



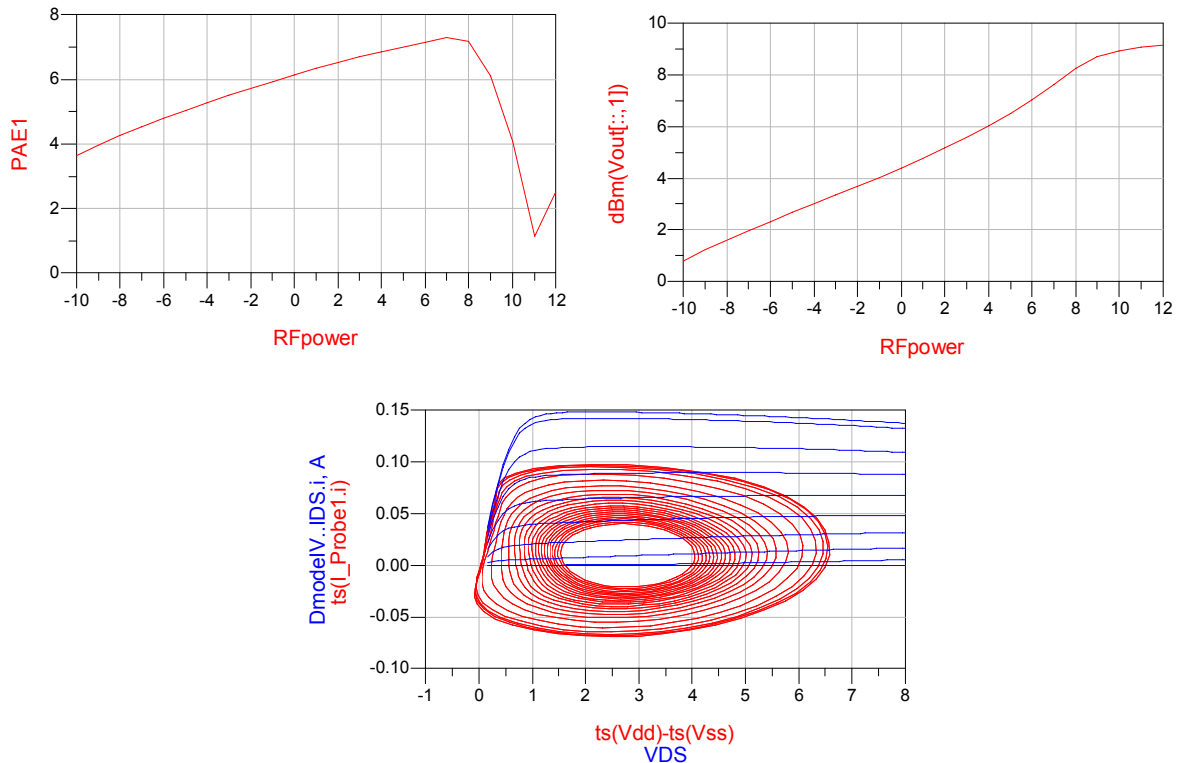
**Figure 8.** Drive Amp Schematic

Note that this is the second stabilizing topology. It turns out that the first topology had approximately the same VSWR, but 5 dB less gain. The voltage domain performance for our driver amp is provided in Figure (9).



**Figure 9.** Voltage Domain Performance for the Driver Amp with R3 Equal 60  $\Omega$

VSWR is larger than desired, but as we said above, we'll have to live with it. The peak power gain is at the correct frequency. The power domain performance is provided in Figure (10).



**Figure 10.** Power Domain Performance for the Driver Amp with R3 Equal 60  $\Omega$

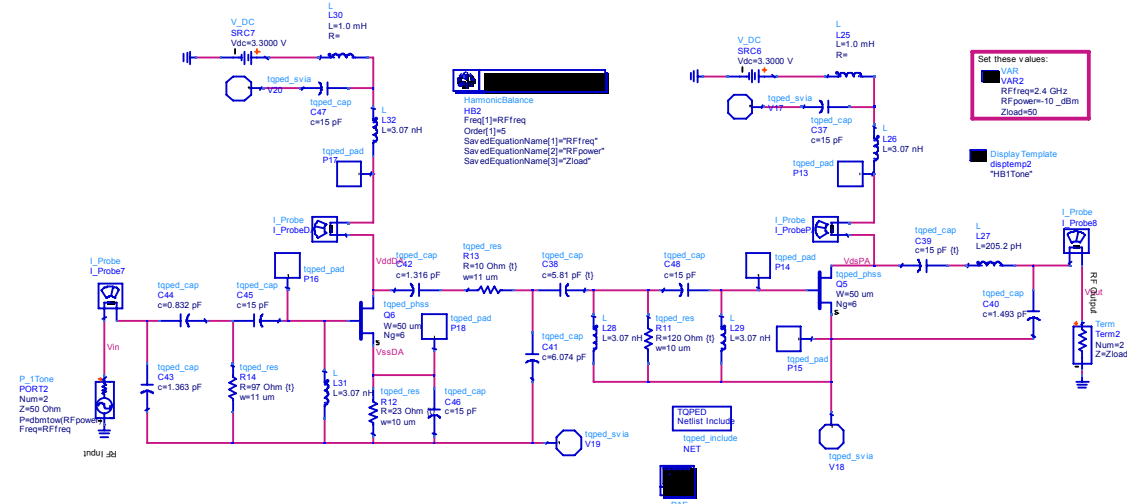
Note that we don't get into compression until beyond 8 dBm. This can be adjusted by changing R3. It was found that while the power domain performance was greatly affected by the value of the source resistor, R3, the voltage domain performance was not. Hence, this will be the major parameter for tuning the composite, 2-stage amplifier. I'm not sure that this load line is as healthy as it could be. I was expecting it to be more linear. I'm not sure what affects this will have on the two-stage performance.

#### 4. High Efficiency, Medium Power Amplifier

We put the driver amp before the power amp in a schematic and simplify. We add together the two parallel intermediate capacitors. When we try to remove the power amp's gate blocking capacitor we encounter stability problems so we'll leave it in. We experiment with the driver amp's source resistor to ground in order to maximize the PAE. We find the 28  $\Omega$  performs the best.

### 4.1. Schematic

The schematic for the final design is given in Figure (11).

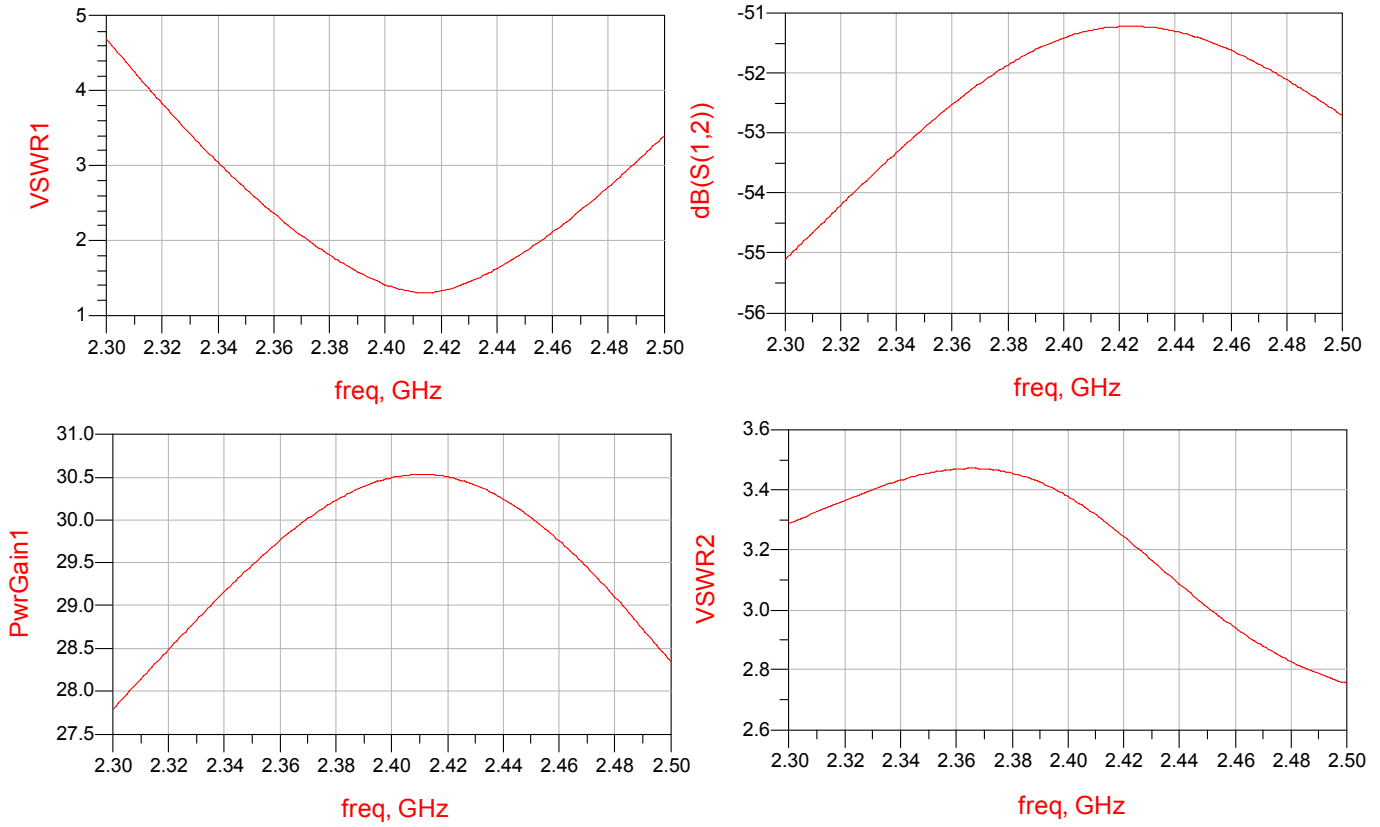


**Figure 11. Two Stage Power Amp Schematic**

In the next stage of development we'll combine the two DC sources into one DC source. Currently, when I do this, the design becomes extremely unstable. Even if the shunt capacitor is increased to 60 pF and the series inductor is increased to 1 H. Note that the PAE DC current is the sum of both sources.

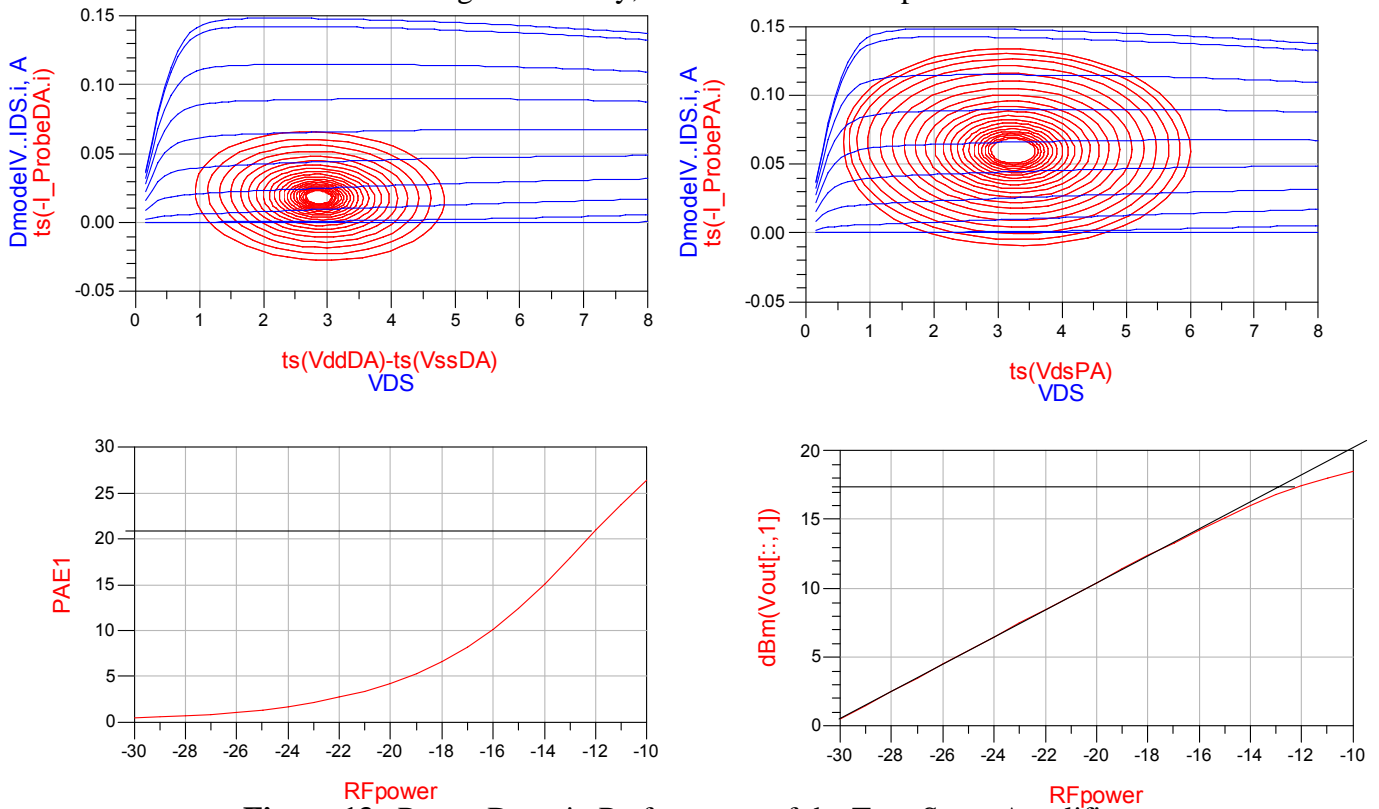
## 4.2. Simulations

The voltage domain simulation is provided in Figure (12).



**Figure 12.** Voltage Domain Performance of the Two Stage Power Amplifier

The VSWRs are out of the desired performance bounds. There is more than enough gain now. There is 2.5 dB of ripple instead of the desired 0.5 dB. The power domain performance is provided in Figure (13).

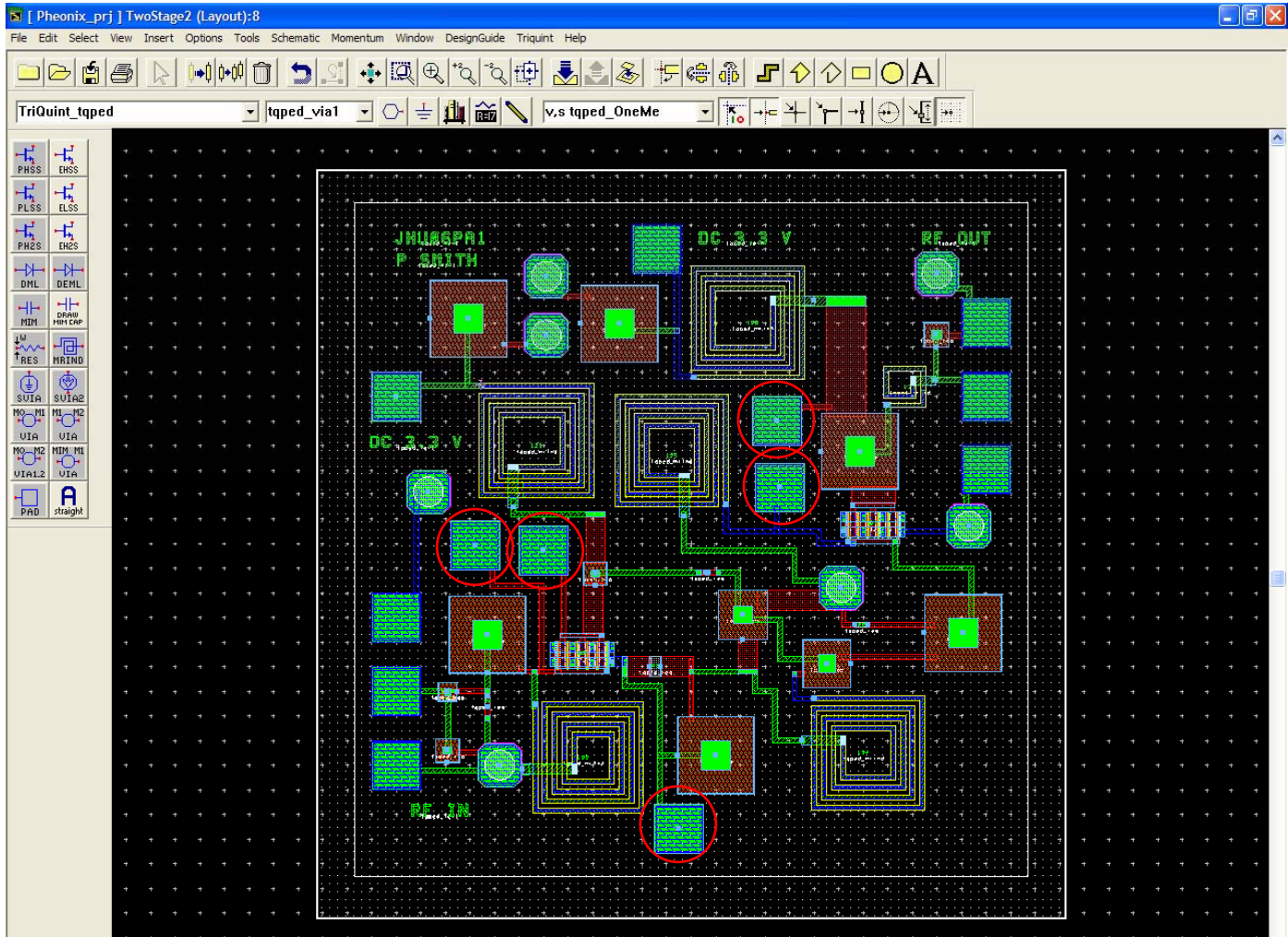


**Figure 13.** Power Domain Performance of the Two-Stage Amplifier

Note that the driver stage is not compressing. This performance produced the best ratio of RF power out to DC power in, through tuning the source resistor to ground on the driver amp. The output power at the one dB compression point is 17 dBm. The PAE 21%.

### 4.3. Layout

The layout is illustrated in Figure (14).



**Figure 14.** Two Stage Power Amp Layout (The bias checking pads are circled in red.)

### 4.4. Test Plans

Assuming that I can acquire suitable matching circuitry I will proceed as follows. First I will set the DC inputs to 3.3 V with no input RF power and measure the VSWRs. Next, I will use the extra pads to check the bias to see if it is correct. Then I will slowly increase the input RF power while measuring the power out and gain to see how closely, if at all, it matches the expected power out and gain.

## 5. Lessons Learned and Things I Would Have Done If I Had More Time

1. In the next stage of development we'll combine the two DC sources into one DC source. Currently, when I do this, the design becomes extremely unstable.
2. I need to consider another method of minimizing gain ripple.
3. I would like to vary the various parameters, such as input voltage, capacitance values, inductance values, resistance values, in order to test for sensitivity.
4. I would like to implement the microstrip to get a better estimate of performance.
5. I would like to try the Emode transistor.
6. I would like to find a better biasing scheme.

## 6. Conclusion

A high efficiency, medium power amplifier was designed using TriQuint 6x50 0.5 $\mu$ m Dmode PHEMTs (TQPED PHSS). On chip drain and gate bias networks, output matching network, and input matching networks were implemented. The goal was maximum efficiency to get the most RF output power for a given DC consumption (i.e. battery life). The resulting performance is summarized in Table (1).

<b>Table 1. Summary of Two Stage Power Amp Performance</b>		
	Desired	Attained
REQUENCY	2.305-2.497 GHz	2.305-2.497 GHz
GAIN	threshold 18 dB, objective 20 dB	30.5 dB peak, 28.8 dB min
GAIN RIPPLE	0.5 dB	2.5 dB
OUTPUT POWER	TBD	17 dBm, 1 dB compression
PAE	threshold 20% @ 1 dB, objective 25% @ 1 dB	21%
VSWR, 50 $\Omega$	1.5:1 input & output	4.8 max input, 3.5 max output
SUPPLY VOLTAGE	+3.3 V signal voltage supply at, goal (3 to 3.6 V range)	+3.3 V