

S-Band Power Amplifier MMIC

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Abstract

This report describes the design, simulation and layout of a two-stage GaAs MMIC power amplifier, operating at S-band from 2.305 to 2.497 GHz as the final pre-radiator element of a transmit chain which forms part of a wireless communications (WCS) transceiver system. The power amplifier design was a class project for Johns Hopkins University's MMIC Design Course (525.787), Fall 2006. The GaAs process used was Triquint Semiconductor's TQPED process.

1. Introduction

Typical modern RF and microwave transmitter designs feature an integrated-circuit power amplifier directly behind the radiating element (whether single-antenna or phased-array element), for maximum RF power output and efficiency. For the power amplifier design described here, the power output specified was 20 dBm with 18 dB of stage gain and > 20% power-added efficiency (PAE).

The initial circuit design was carried out in Agilent's Advanced Design System software. The designers at first hoped to use a single TQPED 50um x 6 gain stage. It became apparent, however, that while the 18 dB gain spec could be met with a single stage, it was not possible to simultaneously achieve 20 dBm of output power, 20-25% PAE at 1dB compression, and maintain unconditional stability in this way. Therefore the designers shifted to a two-stage topology, a 25um x 6 pre-driver followed by a 50um x 6 power output stage, which was the final choice of DFET transistor selection.

2. Circuit Design

Turning to the details of the design, the designers considered a single bias voltage input but ultimately rejected this option in order to avoid complications in the layout. Both stages' drains are biased at +5.2 V and both gates at -0.1 V.

To meet the power-output and PAE specifications, the designers traded against output matching, resulting in an output VSWR of 4:1-6:1 (S22 of 3-4 dB), which though exceeding the input and output VSWR spec of 1.5:1, did not present a significant system performance risk since the PA output will "see" only the transmit radiator, which can be matched to a specific impedance more easily than other system components. A load-pull analysis of the power-amp output is included with this report, which illustrates where on the Smith Chart the best Pout and PAE performance was achieved in terms of impedance seen by the design.

Once the designers settled on the two-stage configuration, they created ideal input and output stabilization and matching networks in ADS for each stage, using TriQuint's models. Stringing the stages together and verifying the gain and PAE performance, the

designers noted that the interstage matching (pre-driver OMN, power stage IMN) totaled two inductors and two capacitors but provided a relatively small impedance transform in terms of the Smith chart. Eliminating both inductors and retaining one small interstage capacitor, they obtained a significant layout area savings.

With the ideal-element circuit created, the designers began the process of inserting TriQuint TQPED inductors, capacitors and resistors while at the same time initiating the layout on a 60 mil x 60 mil ANACHIP die. Large-value RF choke inductors on the bias lines, and DC blocking capacitors at the input and output, consumed the most real estate. Fortunately, the designers had been able to use relatively small capacitors and inductors for input, interstage and output matching, allowing for compaction of the active stages in the center of the layout.

Working iteratively between ADS's Schematic and Layout windows and making use of its design synchronization feature, the designers completed the layout in the 60 mil x 60 mil area with relatively few DRC and LVS errors. Some issues that the designers corrected included: drain voltage traces that needed to be widened for current-handling capacity (changed from metal0 to metal1) and making sure that all substrate vias matched up between the schematic and layout.

Table 1: Simulated Design Performance

Spec	Spec Value	Simulated (TQPED)
Operating Band	2.305 – 2.497 GHz	2.3 to 2.5 GHz
Bandwidth	0.8 GHz	“ “ “
Output Power	20 dBm	21.6 dBm
Gain	18 dB	~ 28 dB over band
PAE	> 20% @ 1dB compression, goal 25%	23.2% @ 1 dB compression
VSWR	< 1.5:1, input and output	Input ~ 1.05:1, output ~ 5:1
Supply Voltage	+5 / -5 V	+5 V, -0.1 V
Size	60 x 60 mil	60 x 60 mil

Design is unconditionally stable, 0.5 to 5 GHz.

Full charts for all simulated parameters are attached to this report.

Schematic

A schematic of the final design is shown below in Figure 1. The first stage consists of a 150um periphery. Two stabilizing resistors are used on the input so as to minimize loss in power. Single L-C network stage is used on the input, while on the output, an interstage match was adopted to improve bandwidth and reduce components. The second stage consists of a 300um periphery part. Again, two stabilizing resistors are used on the input and an L-C matching network on the output of the transistor.

For both parts, approximately 5V is connected to the drain and -0.1V on the gate.

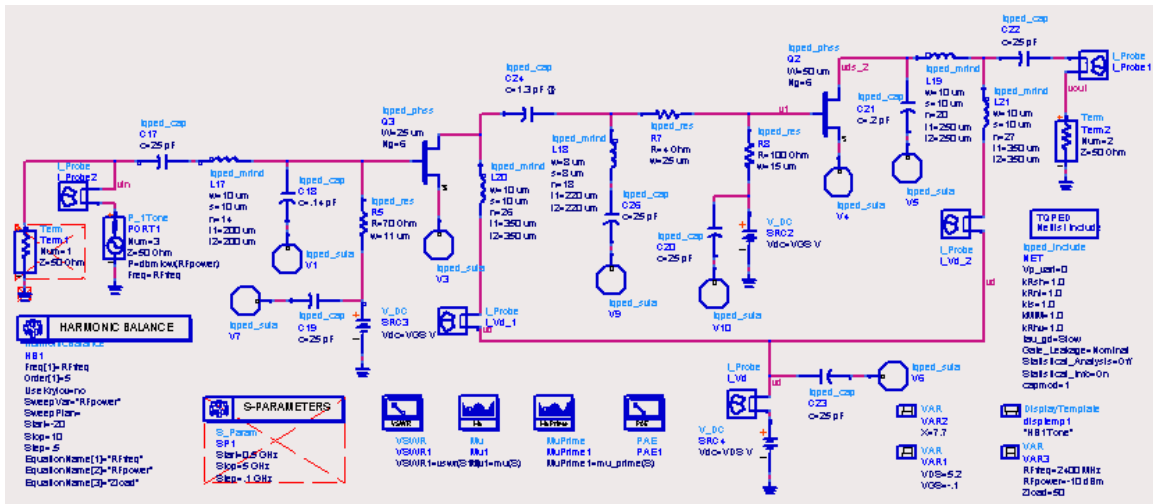


Figure 1. Final Schematic with Triquint Elements

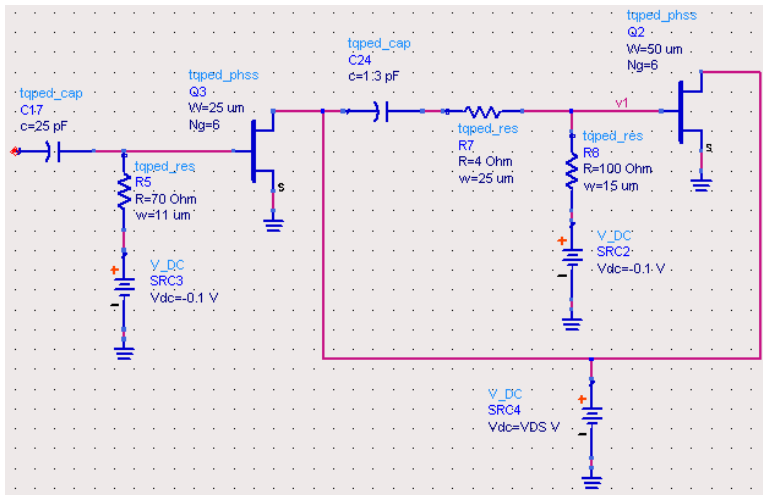


Figure 2. DC Schematic

Simulations

The second stage is critical as far as getting maximum power out. The first stage as mentioned before is really just for meeting the gain requirement. Since the heart of this design is the power amplifier, special attention is given to the second stage of this power amplifier MMIC. We will start by looking at this second stage, show in the schematic above.

We matched the output of the power amplifier using Cripps method. That is, we determine the Cripps resistance from the DC load line. We find this to be around 70Ω . The real part of our output match needs to match this resistance and we must resonate out the imaginary part. Upon doing so, we obtain values similar to what's in the schematic.

A simulation of the second stage verifies that we are achieving the maximum power out of the part. The require output power is at 21.3dBm with ideal parts and 20.5dBm after the power amplifier is complete with real components.

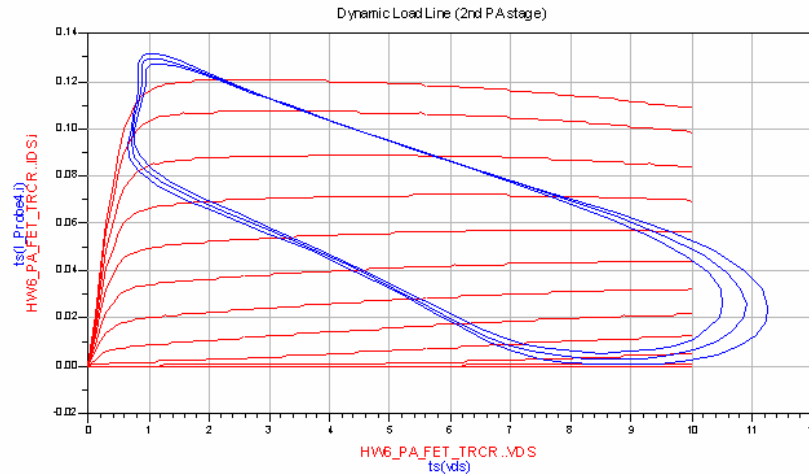


Figure 3. Second Stage's Dynamic Load Line showing maximum power out

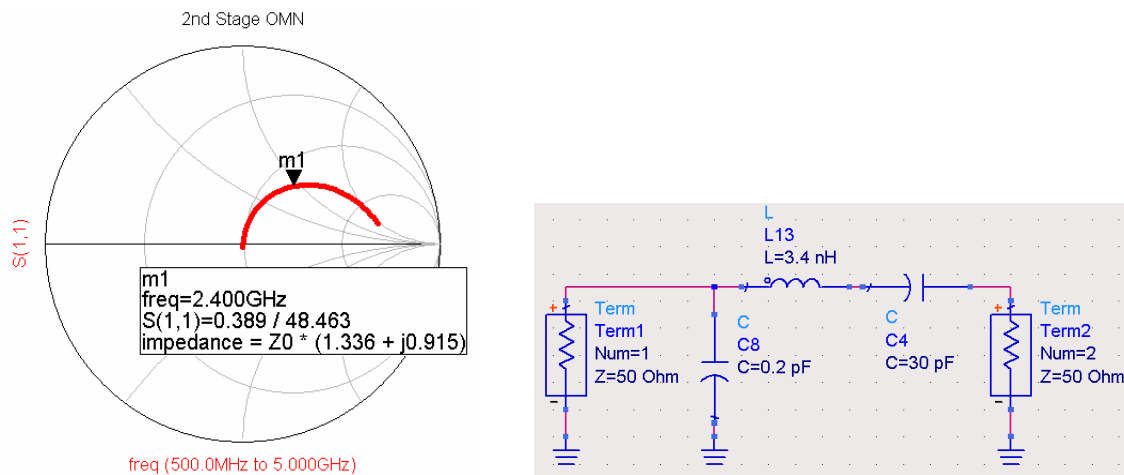


Figure 4. Stage 2: OMN obtained using Cripps method

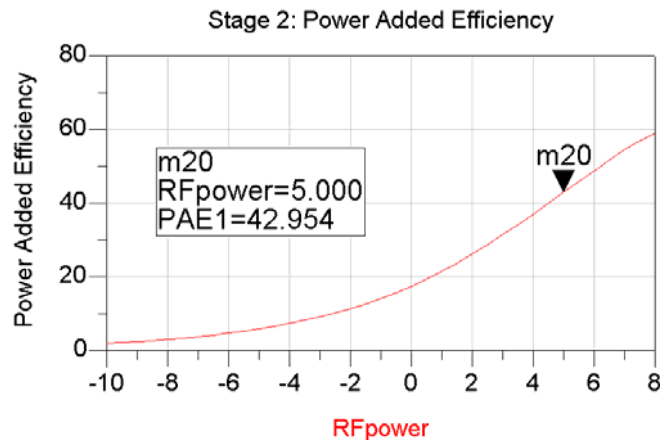


Figure 5. Second Stage's PAE

With some spare time we wanted to demonstrate ADS's Load Pull Analysis capability and see how close our match using Cripps method was to it. In previous design courses, the designers had use G-CAD, a design/layout software which allowed one to look at contours of constant power on the Smith Chart. A similar attempt is made here with ADS. We start out with the schematic shown below, which can be obtained from ADS's Design Examples.

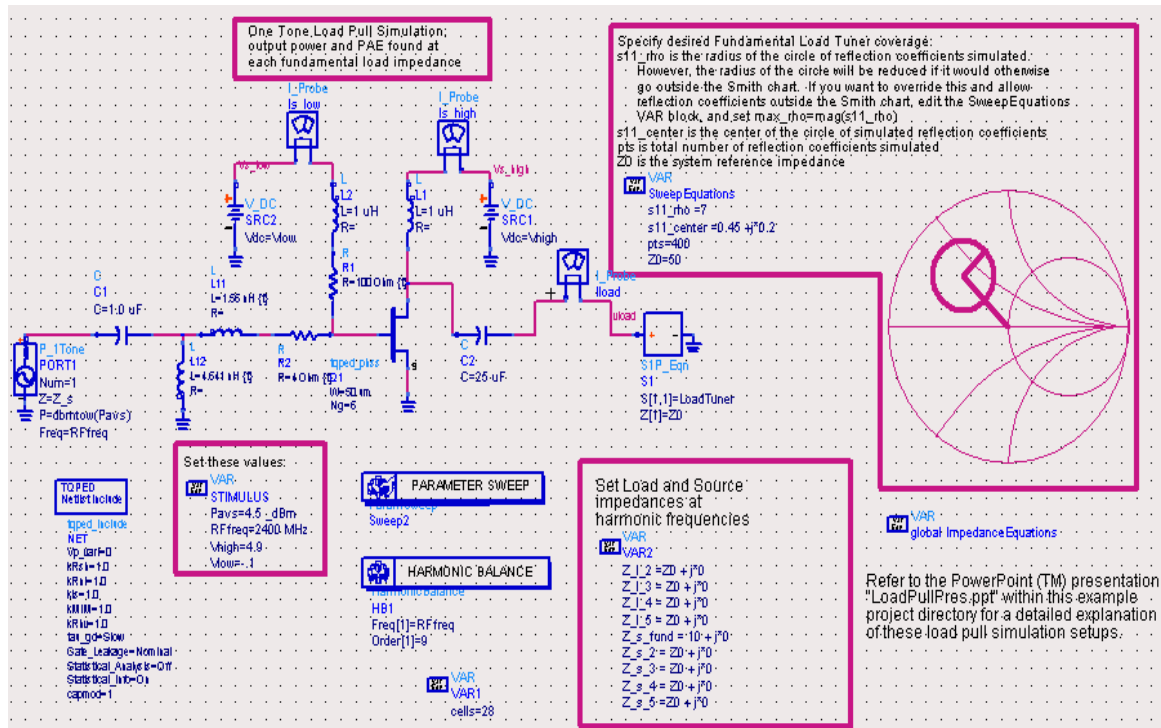
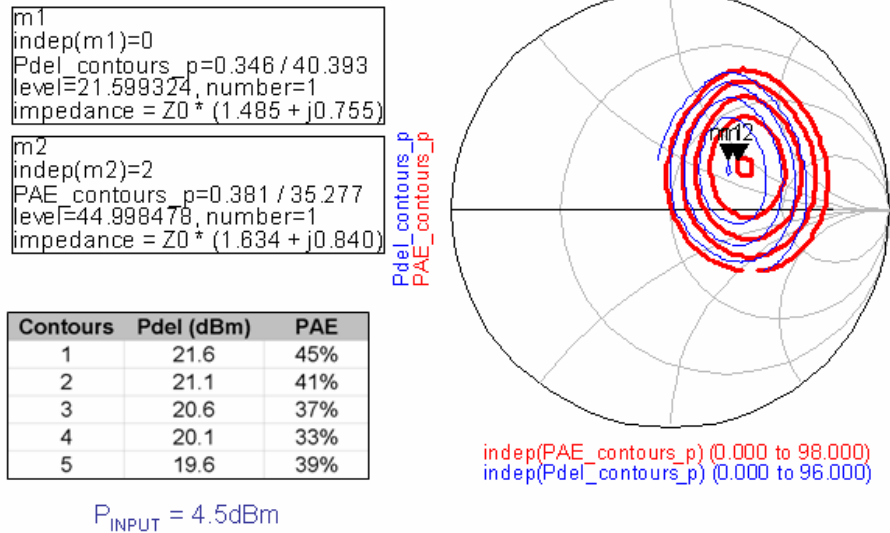


Figure 6. ADS Load Pull Schematic Modified from Design Examples



$$P_{\text{INPUT}} = 4.5\text{dBm}$$

Figure 7. *2nd Stage Match from Load Pull Simulation*

We show that both methods of matching for maximum output power correlate reasonably well in ADS software. The load pull shows a power match at normalized impedance of $1.49+j0.76$ ohms, and the Cripps method showed a power match at normalized impedance of $1.34+j0.92$ ohms. The PAE is off slightly, since it is very sensitive to power level, as evident for the slope of the curve. While plotting the contours is a quicker method in terms of the number of steps and the amount of time needed to synthesize a match, they are both useful in verifying performance. However, since the Cripps method is more of an approximation, if the models were correct, the load pull analysis would probably be more trustworthy.

Now that we have completed giving an overview of the highlights of the power amplifier design, we will present the final simulations verifying the power amplifier design.

We show from the below simulations, the 1dB compression is at an output power of 20.5dBm, as hoped to be over 20dBm. The PAE here is 28%, which shows we passed the goal of 25%.

The overall performance is expected since we are using a part that just meets the needs of our power requirements. If DC power usage is not a critical parameter, one can certainly use larger parts. However, the designers found large VSWR issues with a larger part.

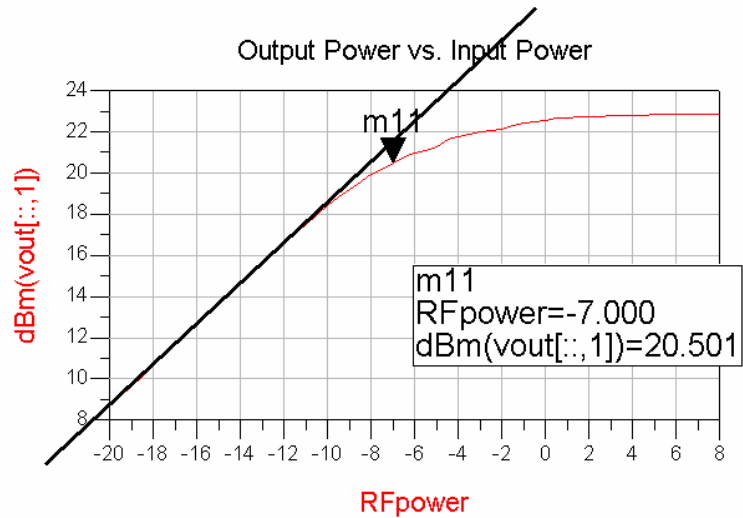


Figure 8. Final Power Amp-Output Power curve

Figure 8 shows the challenge of achieving the 1.5:1 VSWR spec on the output. For a power amplifier this is expected. With more matching components, this can be improved or made closer to 50ohms. Using a larger part to improve match and gain can be done, however this is at the expense of maximum power, which is not always desirable, but is certainly an option based on system needs.

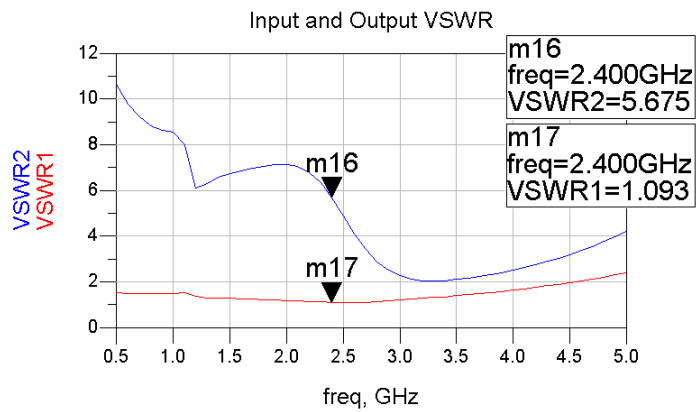


Figure 9. Input and Output VSWR

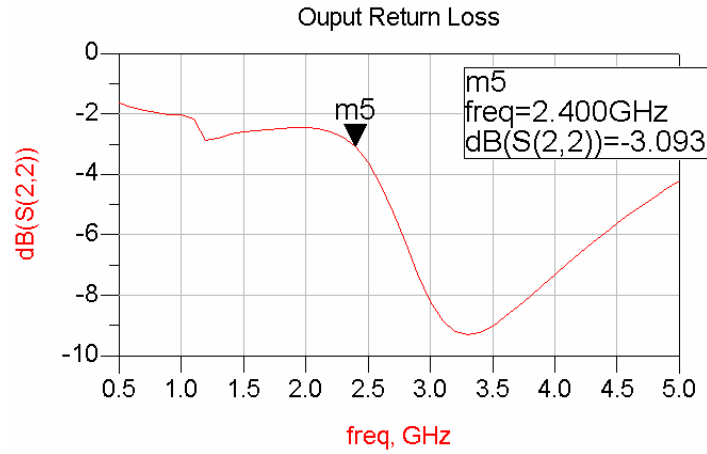


Figure 10. Output Return Loss

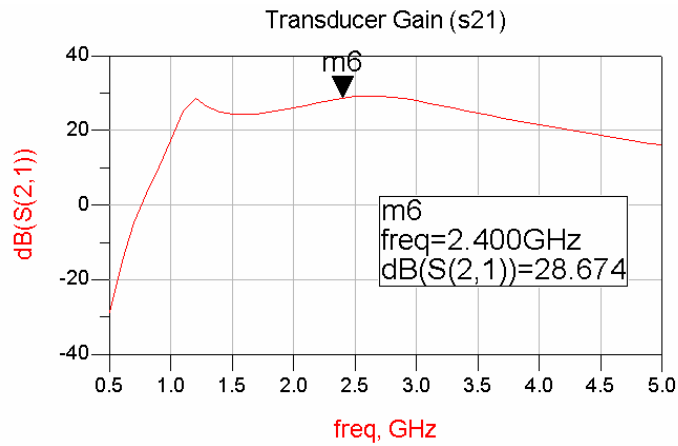


Figure 11. Amplifier Gain

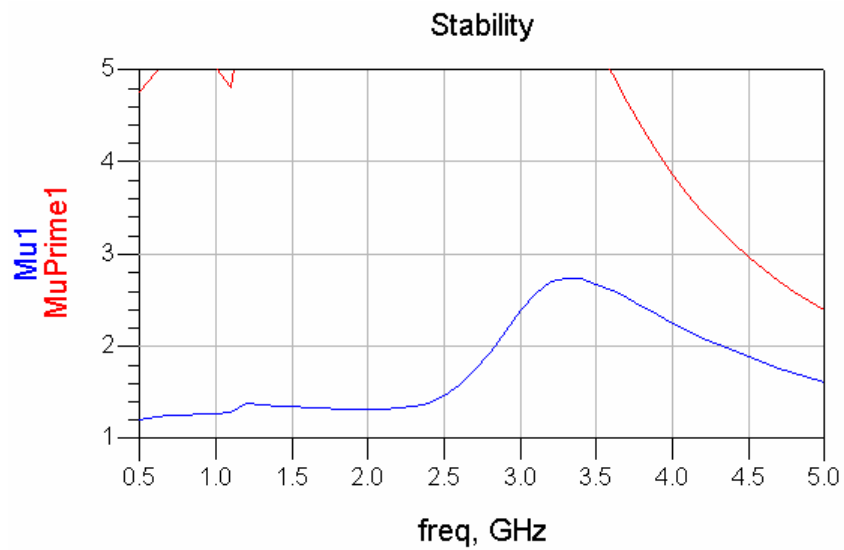


Figure 12. Stability Analysis showing unconditional stability

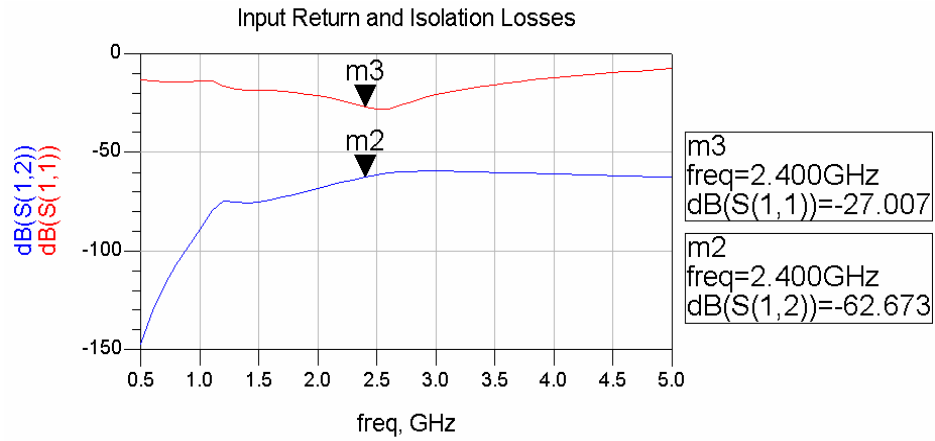


Figure 13. Input Return Loss and Isolation

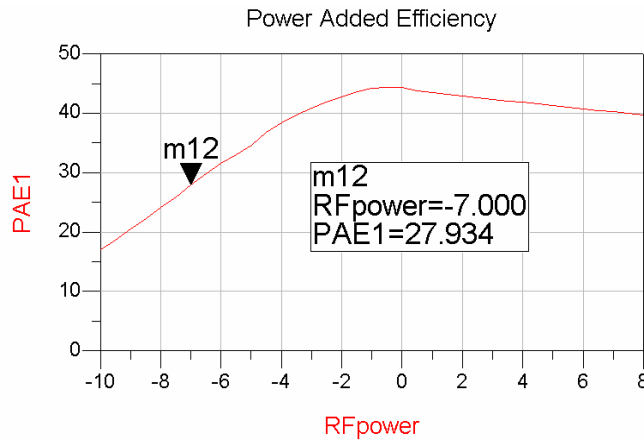


Figure 14. Power Amplifier PAE

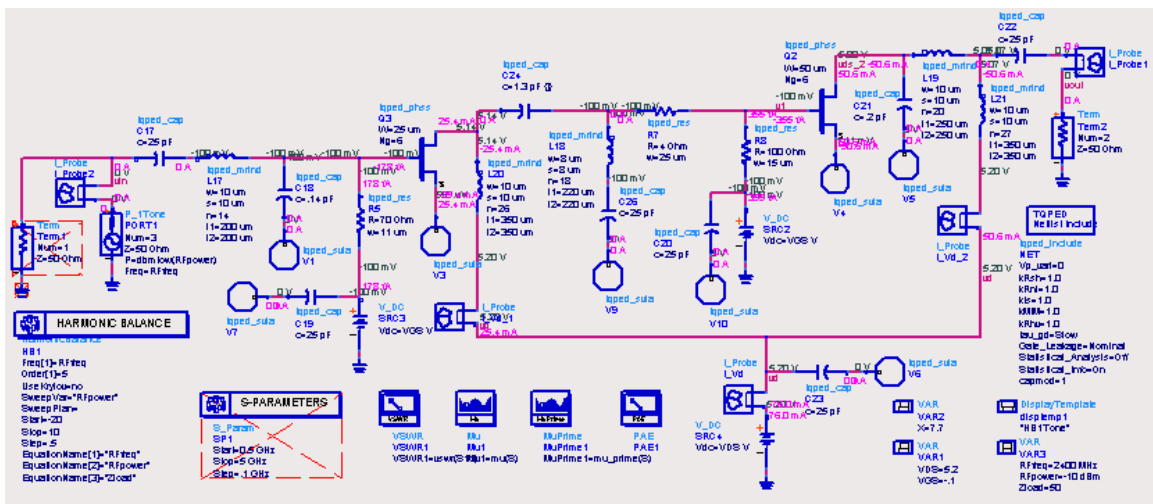


Figure 15. Final Schematic showing DC currents and voltages

Table 2.0. Summary of Performance

	I _{5V} (mA)	V _d (V)	DC power (mW)	RF _{IN} (dBm)	RF _{OUT} (dBm)	Gain (dB)	PAE
Stage 1	25.4	5.14	131	-7	5	12	2%
Stage 2	50.6	5	253	5	20.5	15.5	44%
Total	76	5.2	395	-7	20.5	27.5	28%

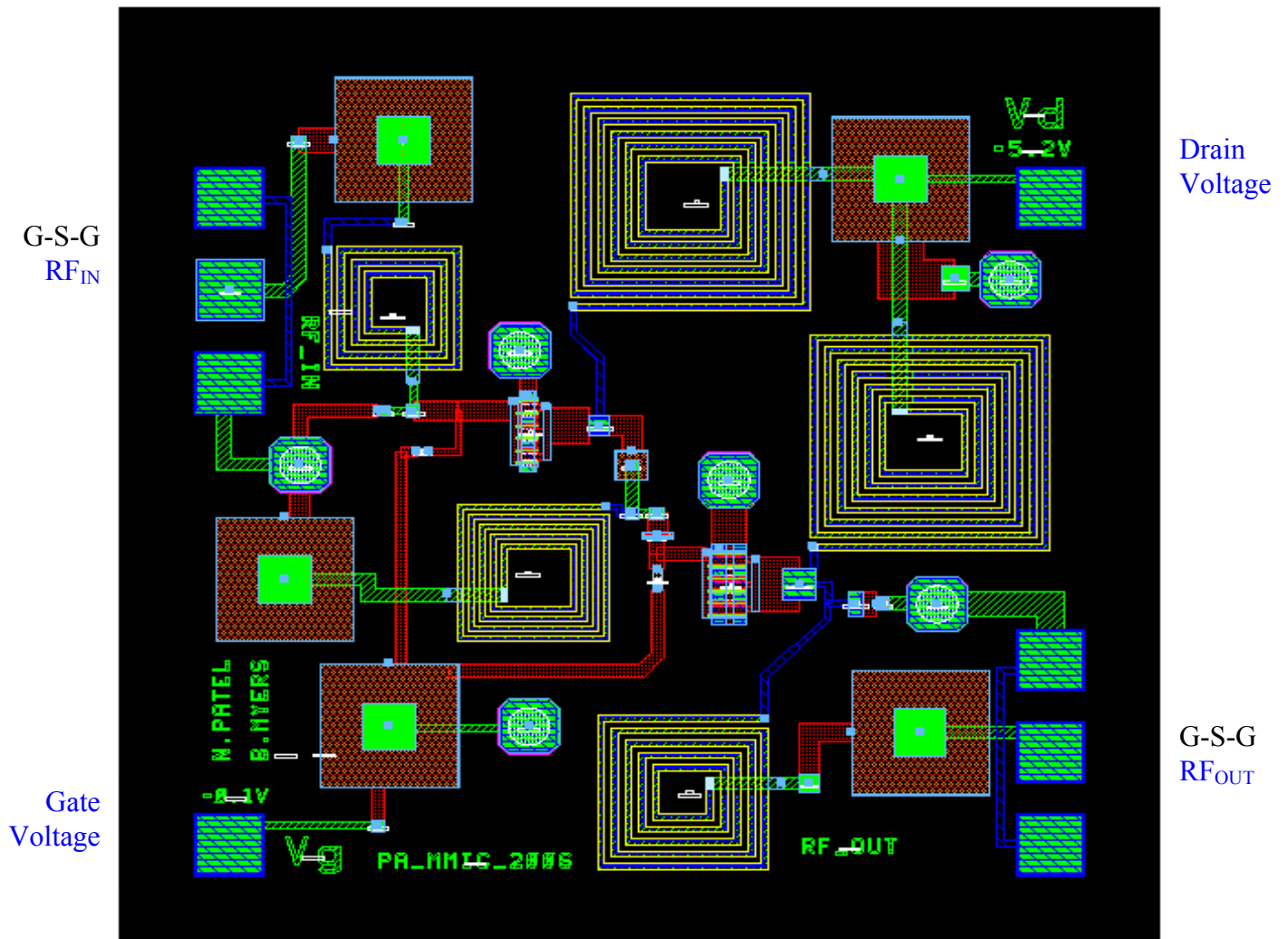


Figure 16. Layout

Test Plan

After MMIC chips are fabricated by Triquint, laboratory testing will begin.

The Ground-Signal-Ground pads for RF_{INPUT} and RF_{OUTPUT} should be compatible with the test probe leads. We will make our measurements using the Cascade probe station and the HP8510 network analyzer.

DC bias pads are labeled with the appropriate voltages required: +5.2V for drain voltage and -0.1V for gate voltage.

Test Equipment

2 Power Supplies ($V_{\text{DRAIN}}=5.2\text{V}$, $V_{\text{G}}=-.1\text{V}$)
Agilent 8510 Network Analyzer
Cascade Model 43 wafer probe station
Spectrum analyzer

Test Procedure

It is safe practice to terminate RF ports before DC power up

Power up device in proper sequence

Calibrate network analyzer to desired range (including 2.3-2.5GHz) using proper calibration standards (SOLT: short, open, load, thru). Note that attenuation may be needed for output port. Network analyzers can be damaged with high power inputs

Measure S-parameters.

Use spectrum analyzer to look at power level of fundamental and harmonics

Conclusion

In summary, we were able to design and lay out on a 60mil x60mil chip, a 2 stage power amplifier with 20.5dBm output power (at 1dB compression) and 28dB gain. Some areas to look out for are process variation shifts. Not a lot of margin is available if one truly needs a minimum of 20dBm output power. However, gain should not be a problem. Also, output match was a significant struggle and neglected in this design since we did not want to stray for an ideal match for maximum power out. To solve some of these troubles, a larger transistor can be used

Other than this, we the power amplifier should work as expected and performance should be solid across the band. The design was shown to be unconditionally stable from .5-5GHz.

There were some lessons learned and things to try out if more time were available. If we had to do this again, here are a few things to look into:

- Create match from load pull and compare performance
- 1st stage was treated more as a gain stage
 - We could have done more of a power match than a match for 50ohms.
 - This would have helped efficiency while maintaining gain requirements
- Improve OMN
 - Reconfigure layout
 - Add more components/matching stages to improve VSWR
- Look at performance variation due to process variation

- Sensitivity of performance on component changes
- Is the design robust?

All in all, we were able to learn a lot in MMIC design and layout and many issues of consideration when laying out a circuit. Also, very useful was the load pull analysis, which is something we would recommend this powerful technique to use in the Power Amplifier homework for future students to take advantage of.