

Power Amplifier MMIC

Ben Myers
Niral Patel

MMIC DESIGN
Prof. Penn – Dr. Reece
12-11-06

Design Overview

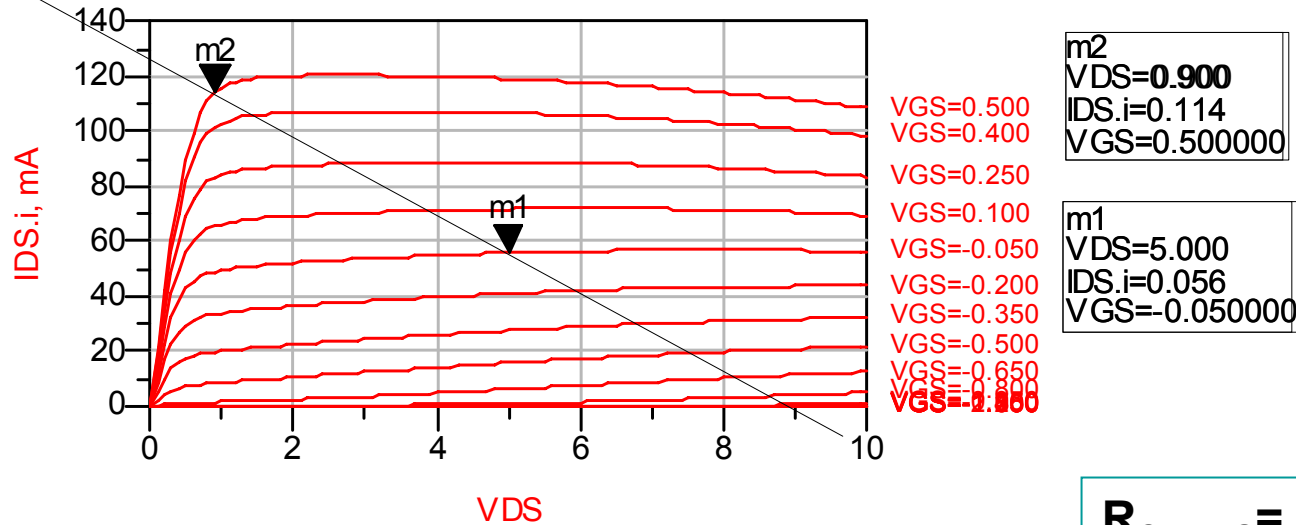
Table 1: Simulated Design Performance

Spec	Spec Value	Simulated (TQPED)
Operating Band	2.305 – 2.497 GHz	2.3 to 2.5 GHz
Bandwidth	0.8 GHz	“ “ “
Output Power	20 dBm	21.6 dBm
Gain	18 dB	~ 28 dB over band
PAE	> 20% @ 1dB compression, goal 25%	23.2% @ 1 dB compression
VSWR	< 1.5:1, input and output	Input ~ 1.05:1, output ~ 5:1
Supply Voltage	+5 / -5 V	+5 V, -0.1 V
Size	60 x 60 mil	60 x 60 mil

Gate Bias Level for $I_{DS}=55\text{mA}$

FET Bias Characteristics

Use with FET_curve_tracer Schematic Template

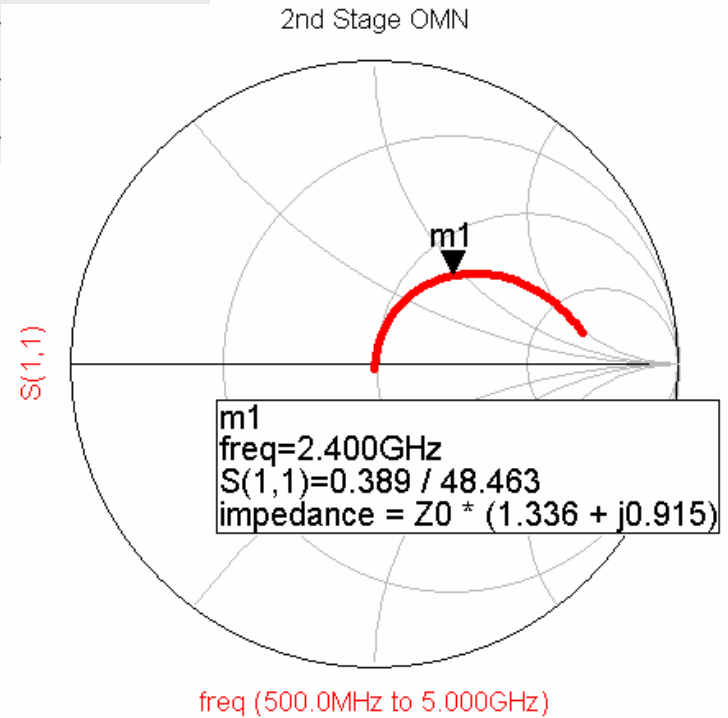
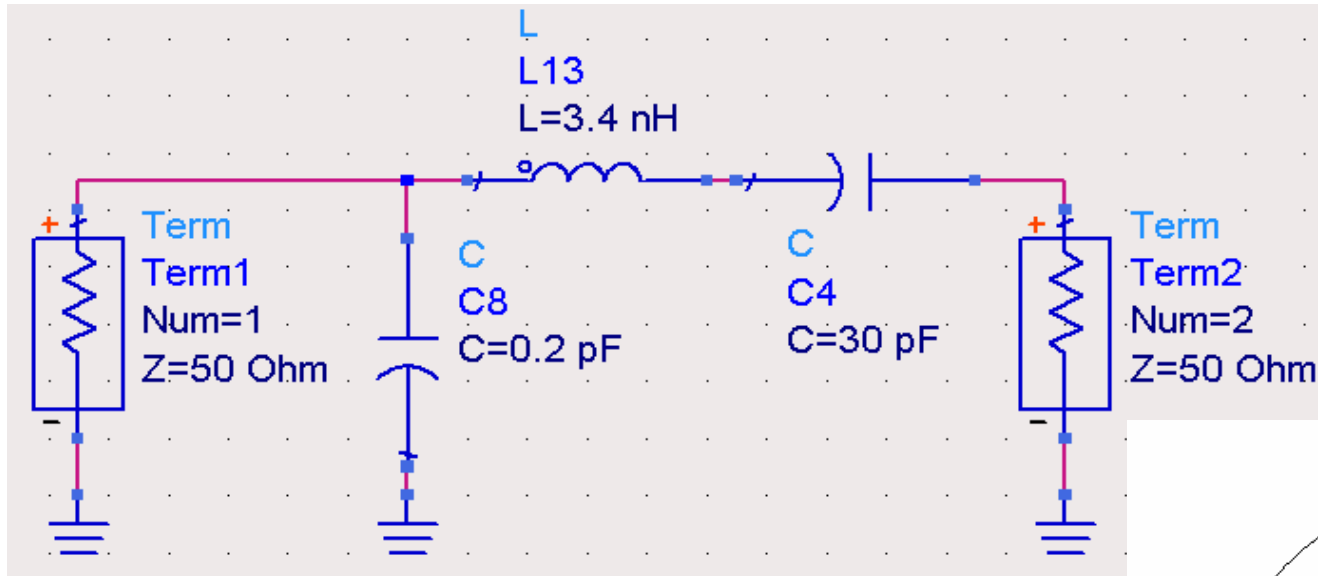


$$R_{CRIPPS} = (9V - 0.9V) / 0.114A = 71.05 \Omega$$

Values at bias point indicated by marker m1.

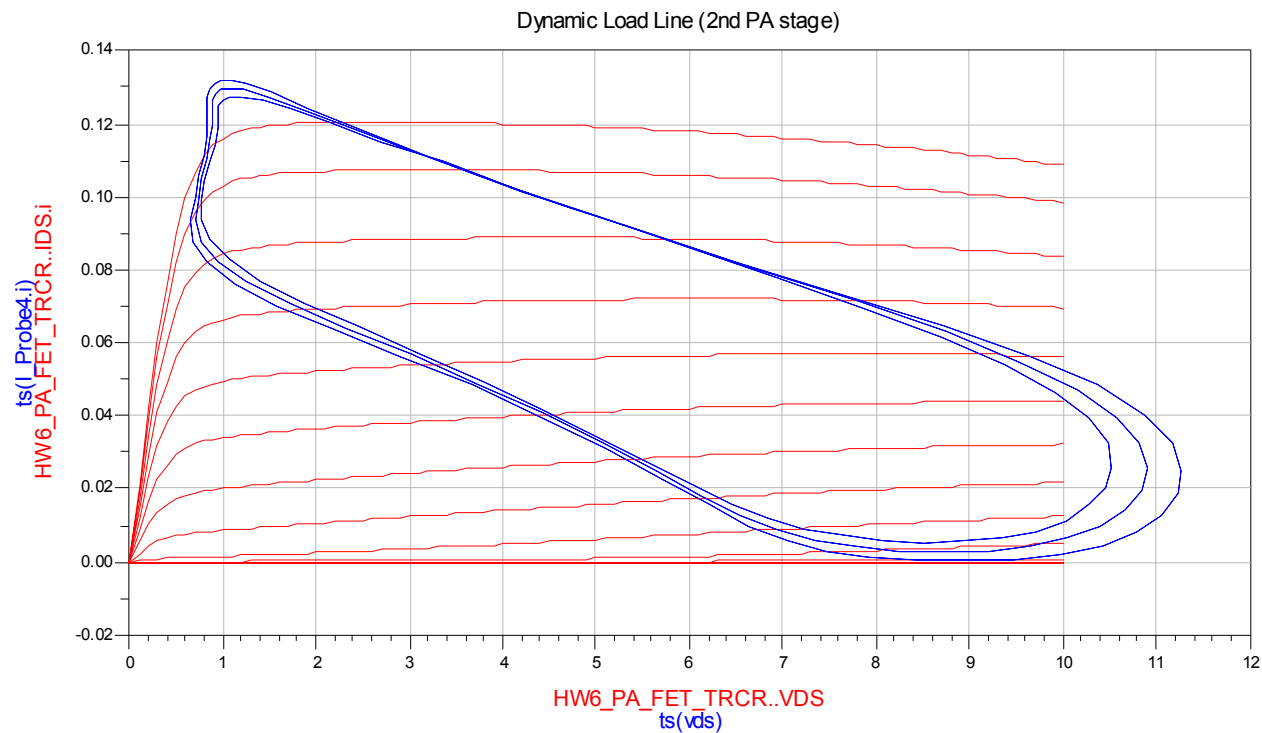
VDS	Device Power Consumption, Watts
5.000	0.279

2nd Stage OMN



2nd STAGE

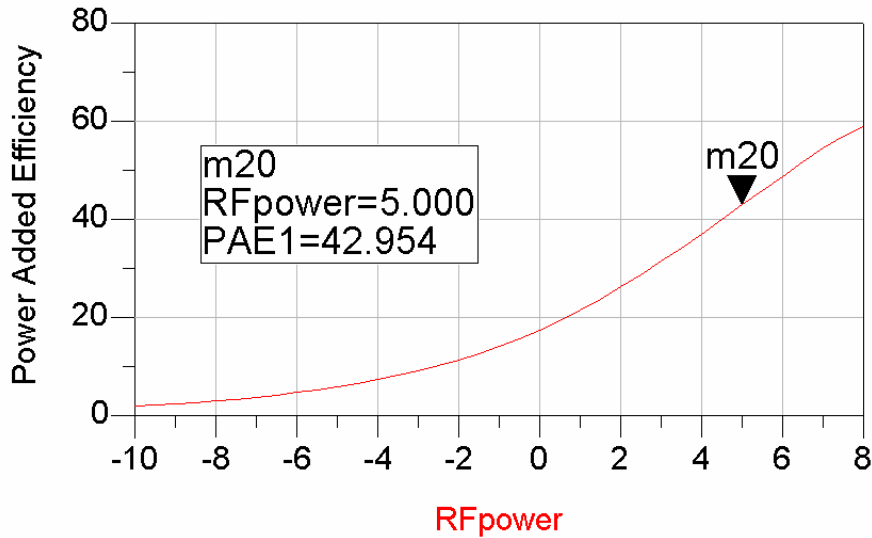
Dynamic Load Line



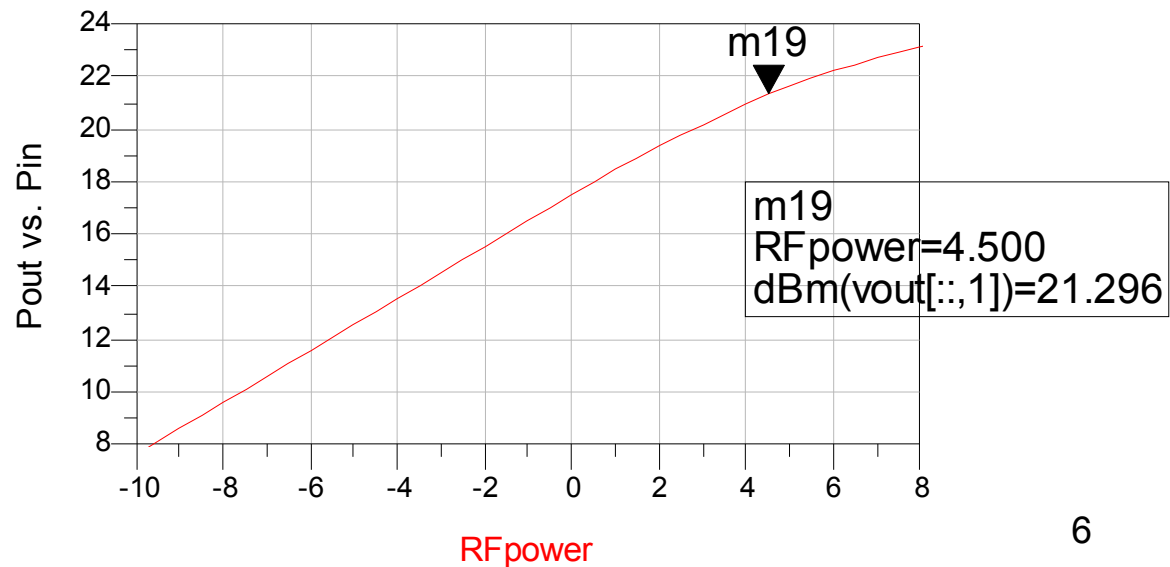
$P_{\text{INPUT}} = 4\text{-}5\text{dBm}$

Ideal Non-Linear Simulations For 2nd stage

Stage 2: Power Added Efficiency



Pout vs. Pin



2nd Stage

Load Pull Analysis

One Tone Load Pull Simulation; output power and PAE found at each fundamental load impedance

Specify desired Fundamental Load Tuner coverage:
s11_rho is the radius of the circle of reflection coefficients simulated.
However, the radius of the circle will be reduced if it would otherwise go outside the Smith chart. If you want to override this and allow reflection coefficients outside the Smith chart, edit the SweepEquations VAR block, and set max_rho=mag(s11_rho)
s11_center is the center of the circle of simulated reflection coefficients
pts is total number of reflection coefficients simulated
Z0 is the system reference impedance

VAR
Sweep Equations
s11_rho = 7
s11_center = 0.45 + j*0.2
pts = 400
Z0 = 50

Set these values:
VAR
STIMULUS
Pavs=4.5_dBm
RFfreq=2400_MHz
Vhigh=4.9
Mow=-1

PARAMETER SWEEP
Parameter Sweep
Sweep2

HARMONIC BALANCE
Harmonic Balance
HB1
Freq[1]=RFfreq
Order[1]=9

VAR
VAR1
cells=28

Set Load and Source impedances at harmonic frequencies
VAR
VAR2
Z[1_2]=Z0 + j*0
Z[1_3]=Z0 + j*0
Z[1_4]=Z0 + j*0
Z[1_5]=Z0 + j*0
Z_s_fund = 10 + j*0
Z_s_2 = Z0 + j*0
Z_s_3 = Z0 + j*0
Z_s_4 = Z0 + j*0
Z_s_5 = Z0 + j*0

VAR
global Impedance Equations

Refer to the PowerPoint (TM) presentation "LoadPullPres.ppt" within this example project directory for a detailed explanation of these load pull simulation setups.

2nd Stage

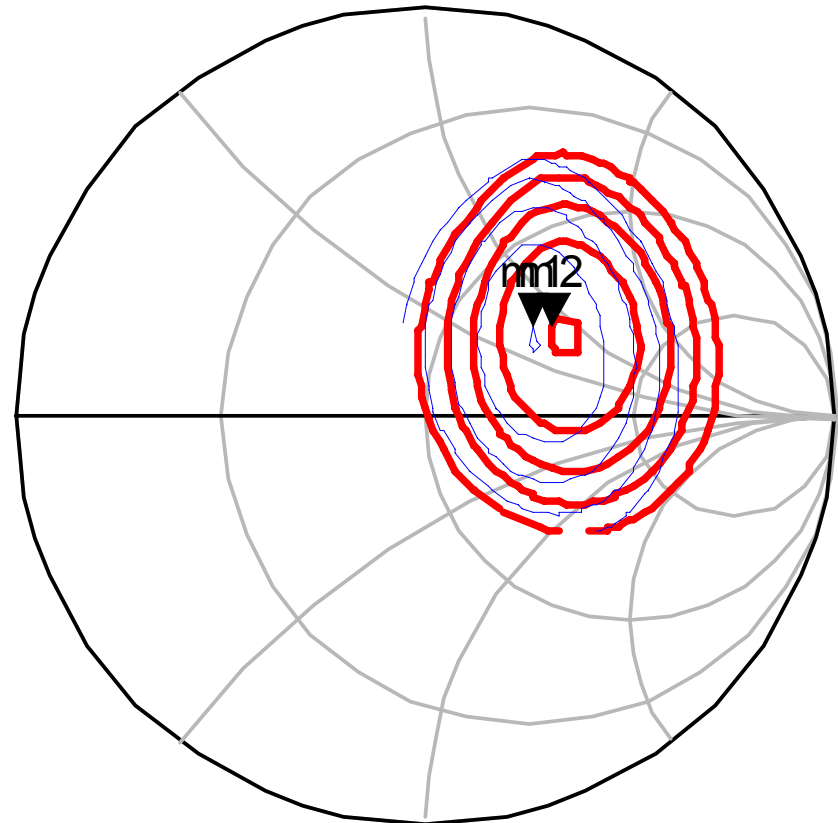
Load Pull Simulation

Plot contours of constant Output Power and PAE

m1
indep(m1)=0
Pdel_contours_p=0.346 / 40.393
level=21.599324, number=1
impedance = Z0 * (1.485 + j0.755)

m2
indep(m2)=2
PAE_contours_p=0.381 / 35.277
level=44.998478, number=1
impedance = Z0 * (1.634 + j0.840)

Pdel_contours_p
PAE_contours_p



indep(PAE_contours_p) (0.000 to 98.000)
indep(Pdel_contours_p) (0.000 to 96.000)

Contours	Pdel (dBm)	PAE
1	21.6	45%
2	21.1	41%
3	20.6	37%
4	20.1	33%
5	19.6	39%

$P_{\text{INPUT}} = 4.5\text{dBm}$

Comparison of Matching Methods

- Cripps method

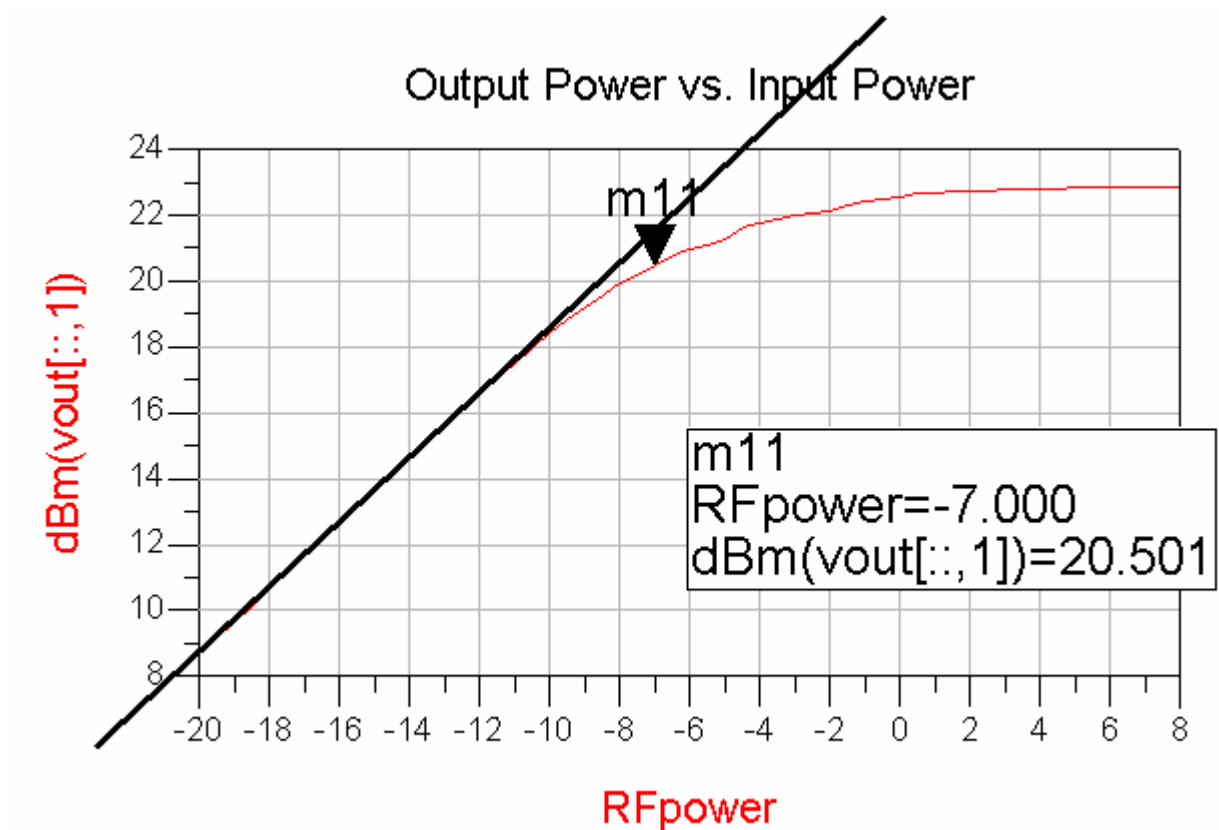
- Use dynamic load line on FET IV curves to maximize/optimize voltage and current swing, and determine RCRIPPS
- Match output of FET to R_{CRIPPS} , cancel reactance, match input to 50Ω
- $z = 1.34 + j0.92 \Omega$
- $P_{OUT} = 21.3\text{dBm}$

- Load Pull analysis

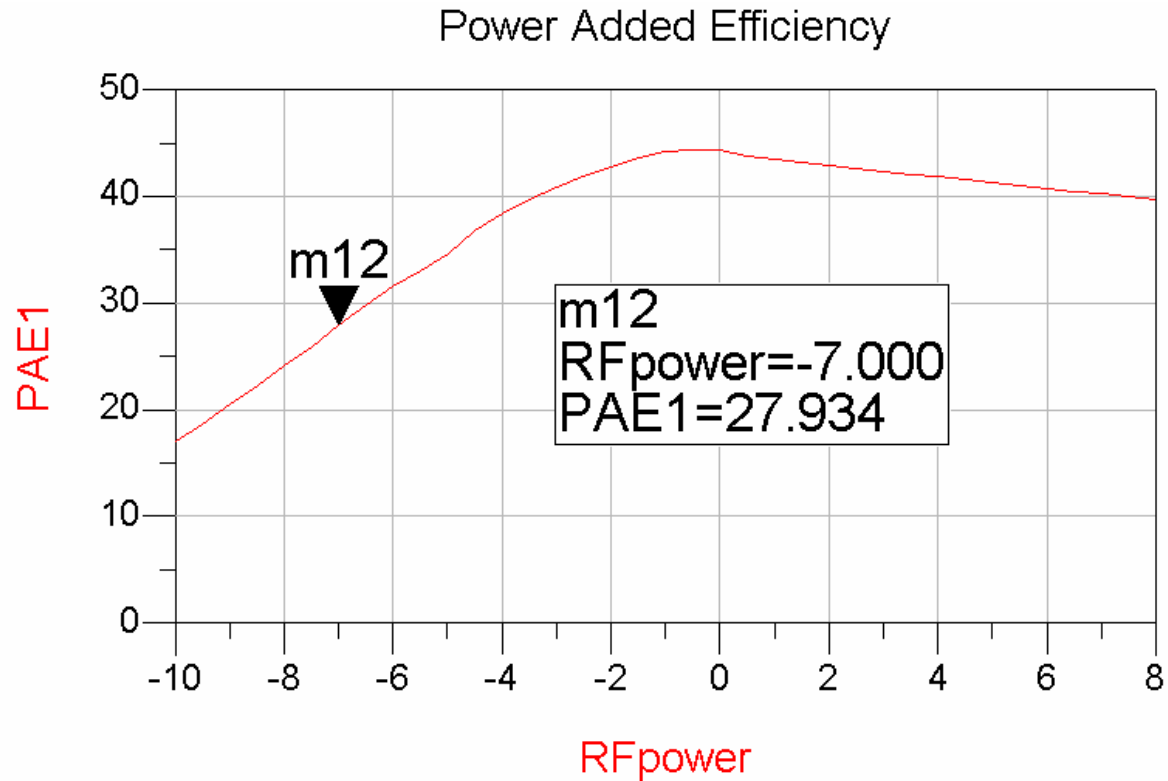
- Use contours of constant power(/PAE) on Smith chart do directly determine impedance needed
- Match output of FET to this impedance, match input to 50Ω
- $z = 1.49 + j*0.76 \Omega$
- $P_{OUT} = 21.6\text{dBm}$

Final Simulations

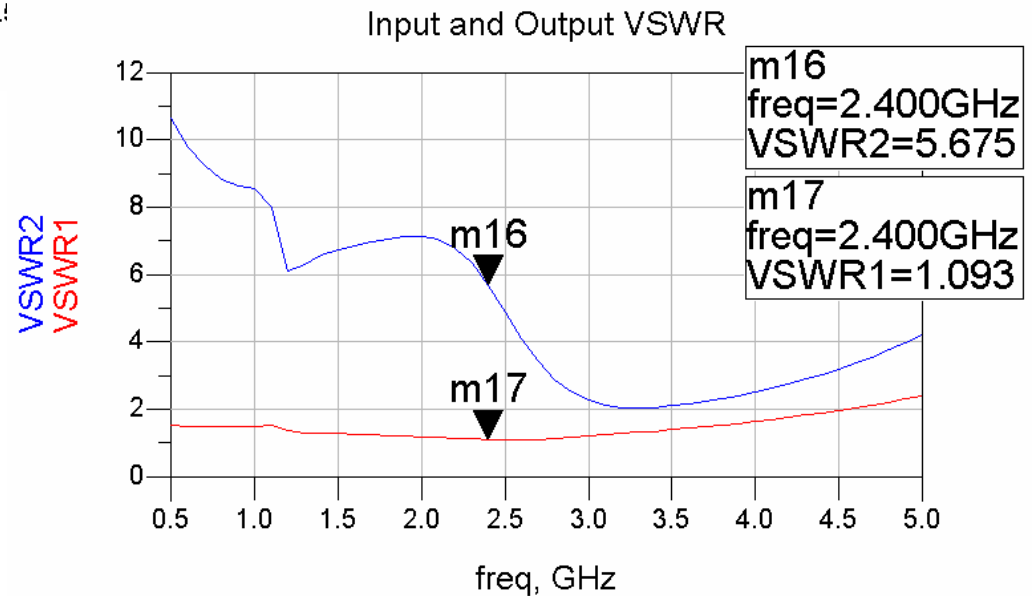
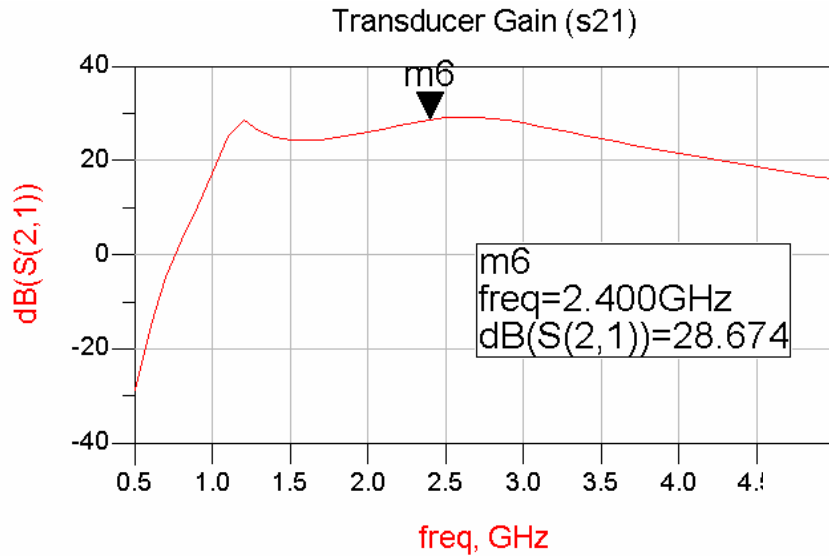
1dB compression point



Efficiency (Power-Added)

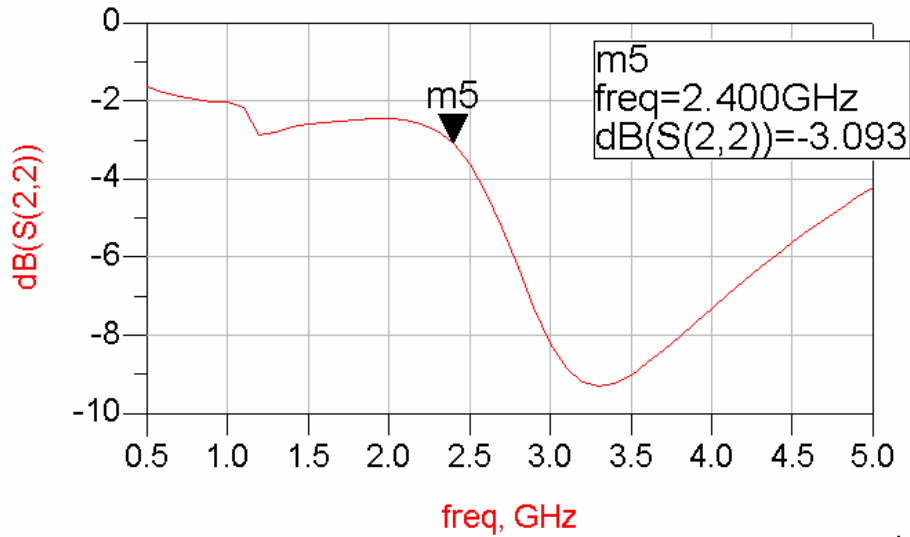


S-Parameters

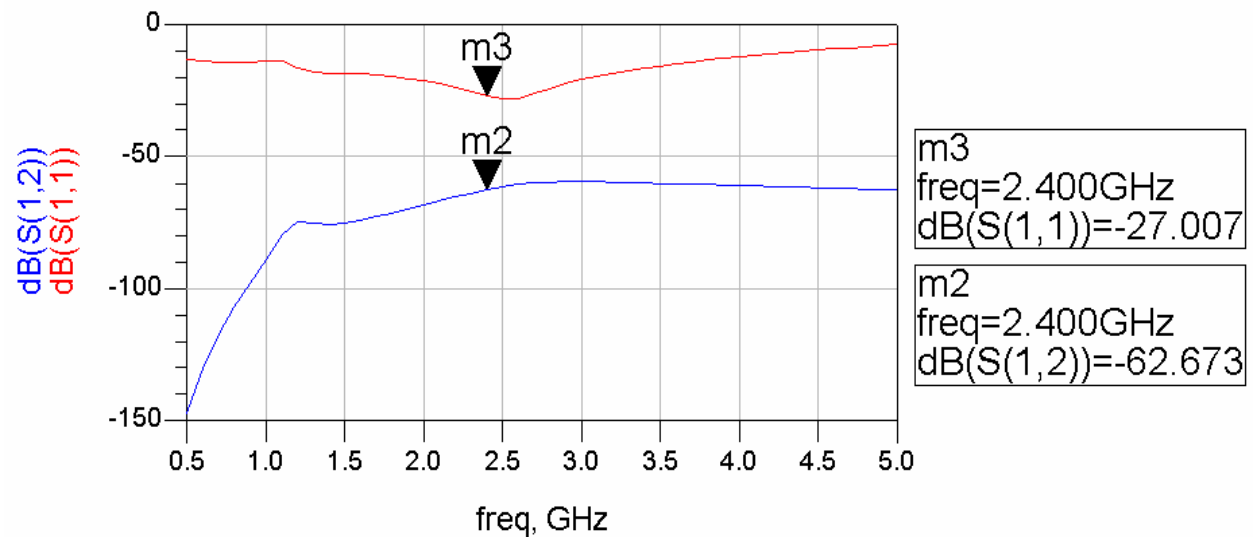


S-Parameters

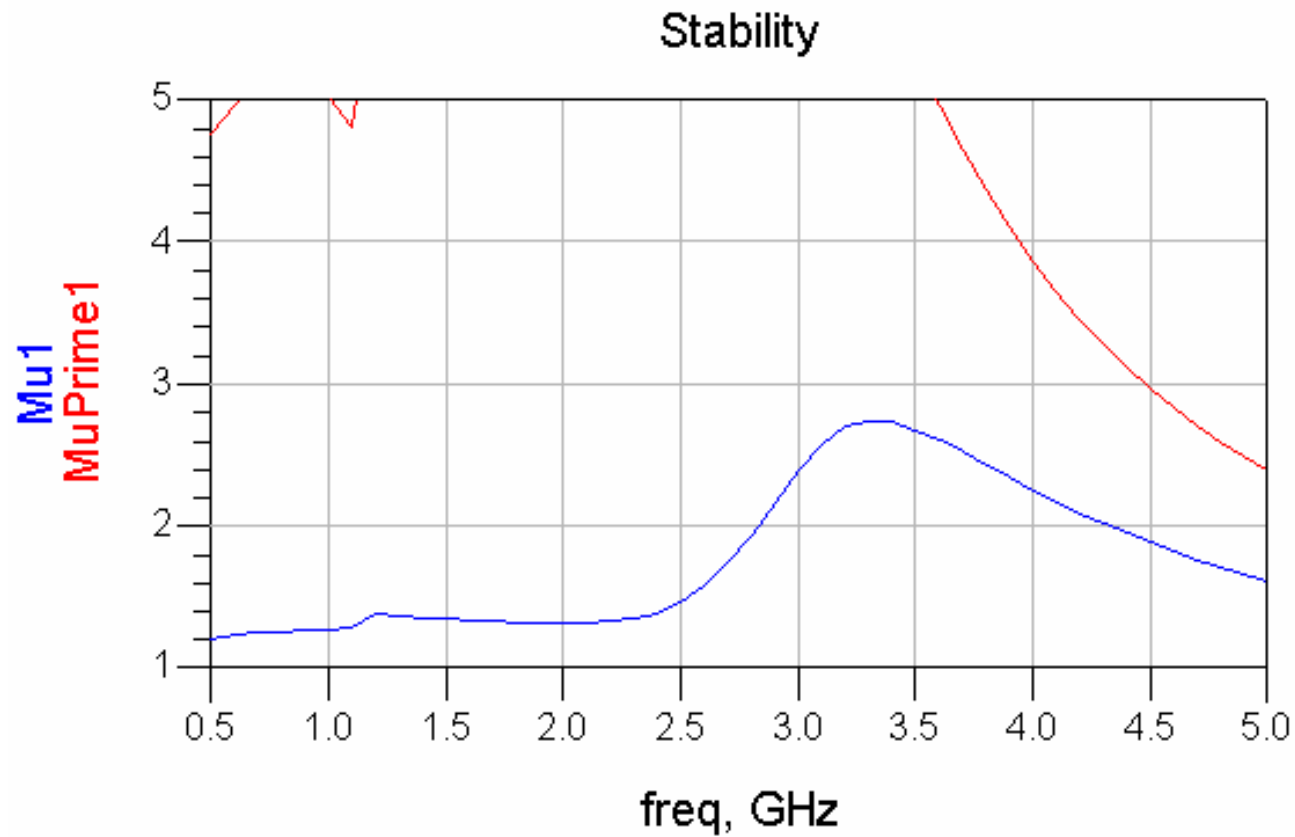
Output Return Loss



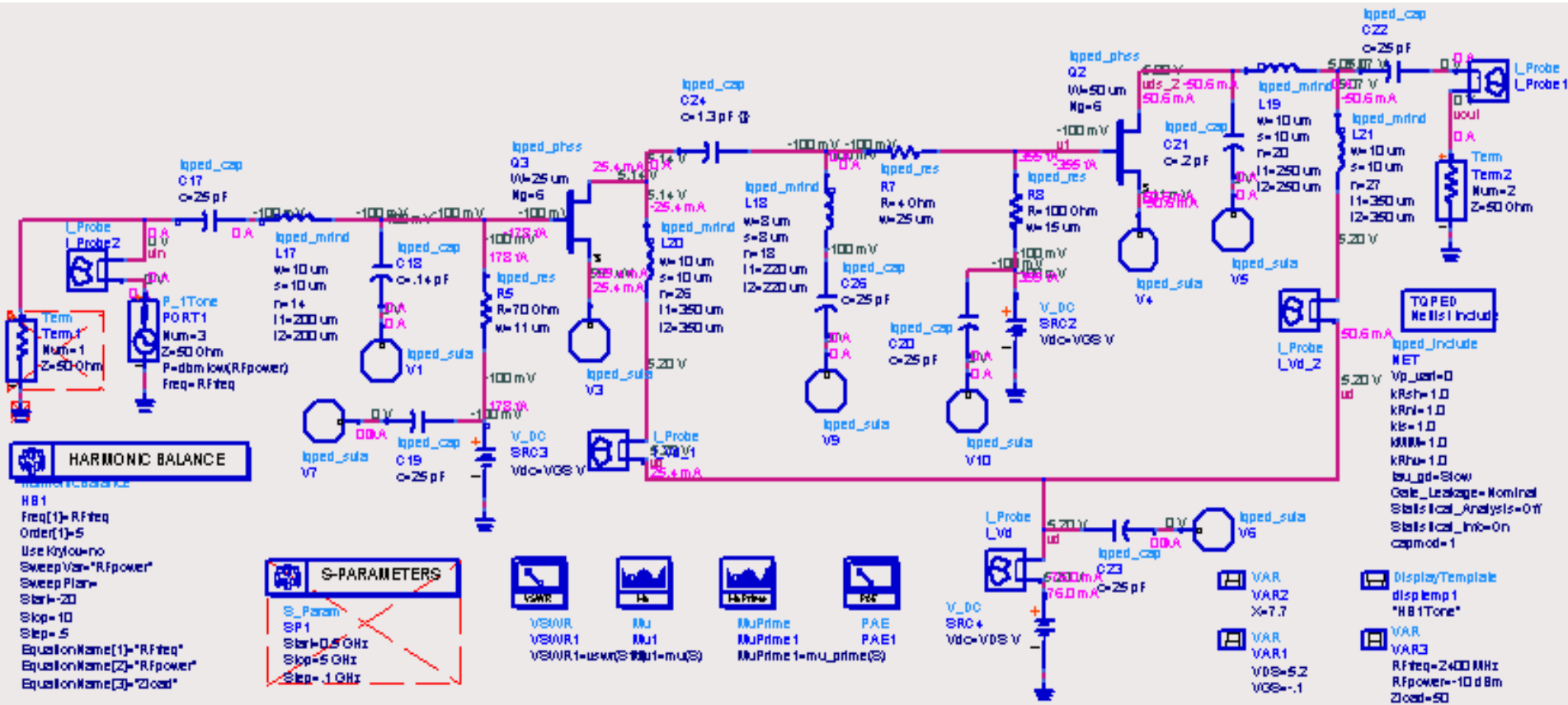
Input Return and Isolation Losses



Stability

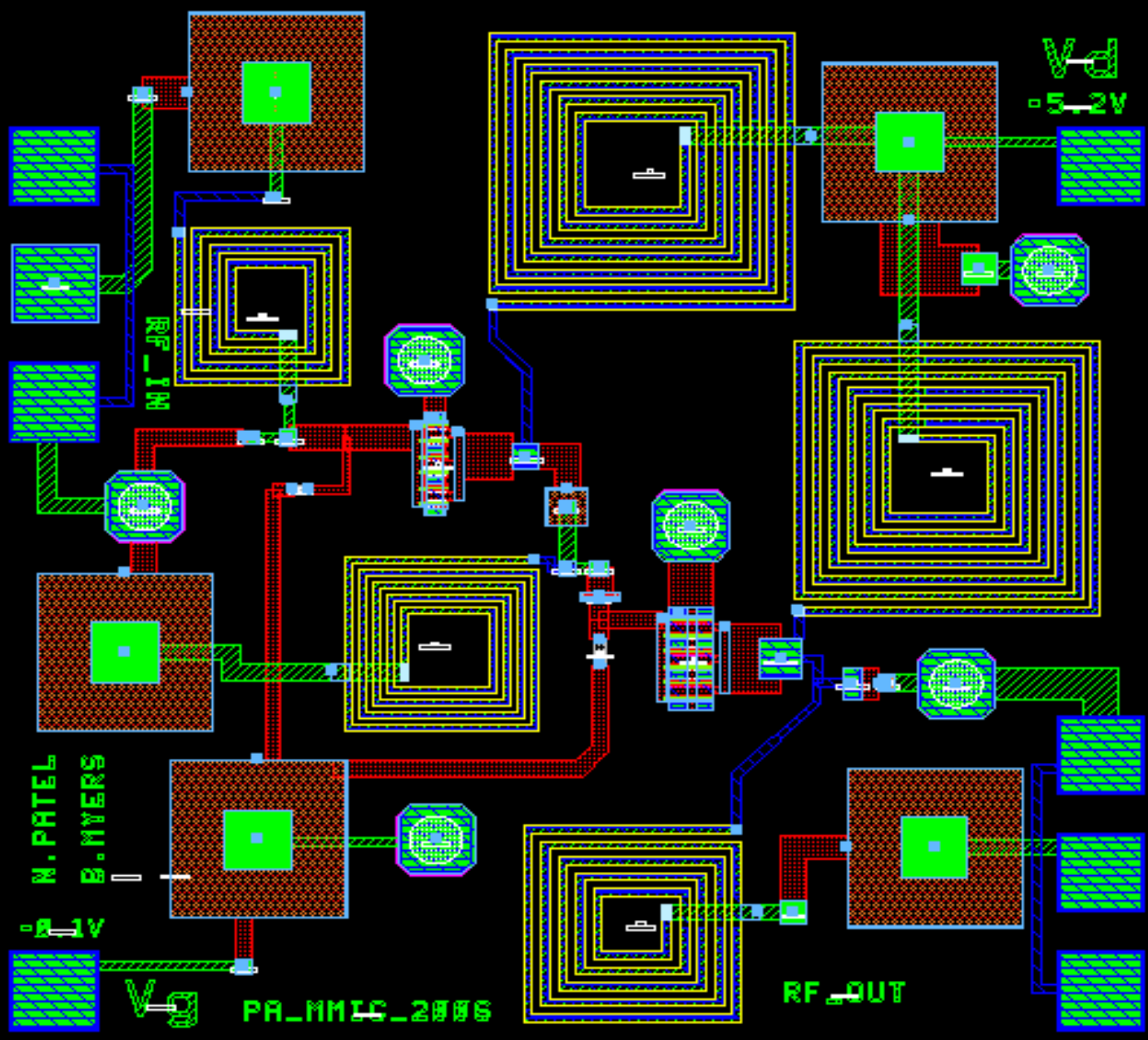


Final Schematic with Current and Voltage Annotation



	I _{5V} (mA)	V _d (V)	DC power (mW)	RF _{IN} (dBm)	RF _{OUT} (dBm)	Gain (dB)	PAE
Stage 1	25.4	5.14	131	-7	5	12	2%
Stage 2	50.6	5	253	5	20.5	15.5	44%
Total	76	5.2	395	-7	20.5	27.5	28%

Layout



N. PATEL
B. MYERS

Conclusion and Future Work

- Create match from load pull and compare performance
- 1st stage was treated more as a gain stage
 - We could have done more of a power match than a match for 50ohms.
 - This would have helped efficiency while maintaining gain requirements
- Improve OMN
 - Reconfigure layout
 - Add more components/matching stages to improve VSWR
- Look at performance variation due to process variation
 - Sensitivity of performance on component changes
 - Is the design robust?