

2.4 GHz MMIC LNA Design Project

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1 Abstract

This report describes the design of a 2.4 GHz monolithic microwave integrated circuit (MMIC) low noise amplifier (LNA). This amplifier is the first stage of a receive array for the S-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies.

2 Goals

The purpose of this project was to design a 2.4 GHz MMIC LNA based on the following performance criteria:

Center Frequency: 2.4 GHz

Noise Figure: 2dB

Gain: 20dB

DC Voltage Supply: single +5V

VSWR: <1.5:1 input and output (-14dB)

Input IP3: >+5dBm

The layout must also fit on a TriQuint 60 mil by 60 mil die with a substrate thickness of 100 microns. The circuit must be designed and simulated using the ADS with the TriQuint TQPED component library.

3 Specifications

The circuit, as designed, will operate with the following specifications:

Center Frequency: 2.4 GHz

Noise Figure: 1.868dB

Gain: 25.9dB

DC Voltage Supply: single +5V

VSWR: better than -17dB

Input IP3: >+5dBm

4 Tradeoffs

Gain and stability are traditionally the tradeoffs in any microwave amplifier design. Also, the noise figure may be increased, depending on the DC resistance configured at the input for DC biasing.

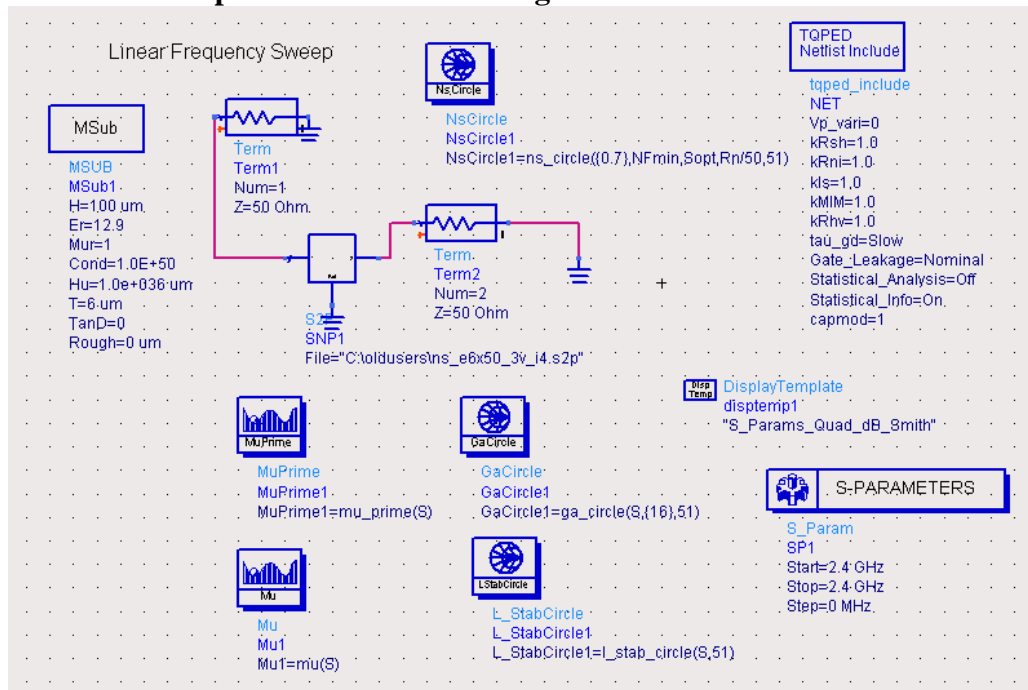
5 Design Approach

The E-mode (EHSS) FET topology was chosen because of the single, positive voltage design criterion. The D-mode FET topology, which is the only other choice, would have required both a positive and negative voltage supply. The E-mode FET topology was also

chosen due to the lower noise figure and higher gain when biased under comparable conditions, as compared to the D-mode FET topology.

The primary parameter of interest is achieving a low noise figure and, secondarily, a high gain. The following graphic (Figure 1) illustrates the circuit used to determine the appropriate input matching reflection, S_{11} , to attain these amplifier characteristics:

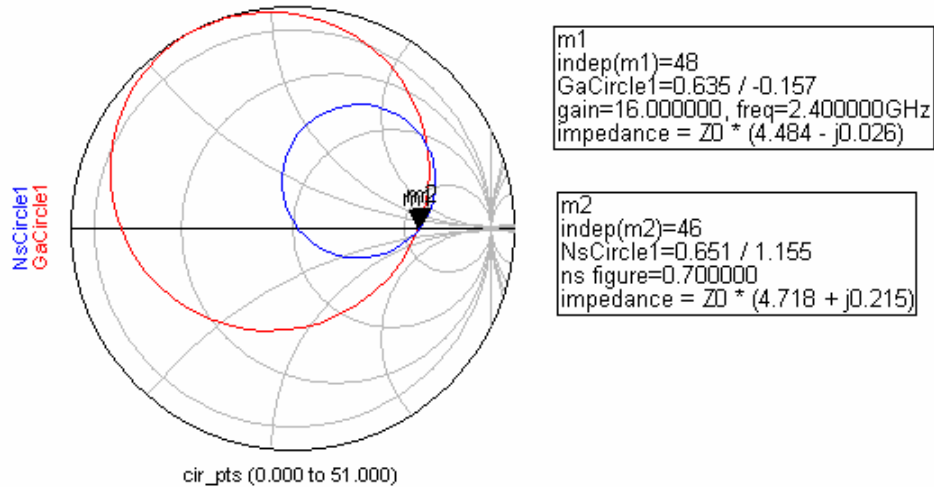
FIGURE 1 – Optimum Gain / Noise Figure Simulation Circuit



The following graphic (Figure 2) illustrates the results of the noise figure/gain simulation:

FIGURE 2 – Optimum Gain / Noise Figure Circles

Gain and Noise Figure Circles - Emode FET - Single Stage

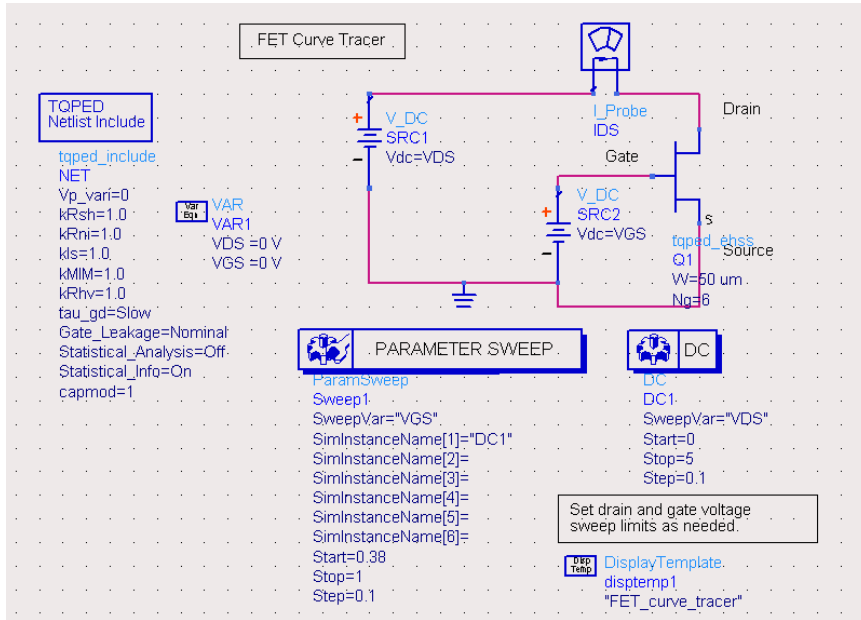


The optimum trade-off between low noise figure and gain occurs when the input matching circuit matches the impedance near the two markers listed above. It is shown that we will expect a gain of 16 dB or 39.8 and a noise figure of 0.65 dB or 1.16 for a single stage implementation. In cascade, the theoretical gain and gain of the cascade of two identical stages would be 32 dB and $1.16 + [(1.16 - 1) / (39.8)] = 0.66$ dB. The replacement of ideal components with real components will increase the noise figure of the circuit.

Clearly the design goals will not be met for the gain criterion with a single stage. Therefore, a two-stage design will be designed and implemented.

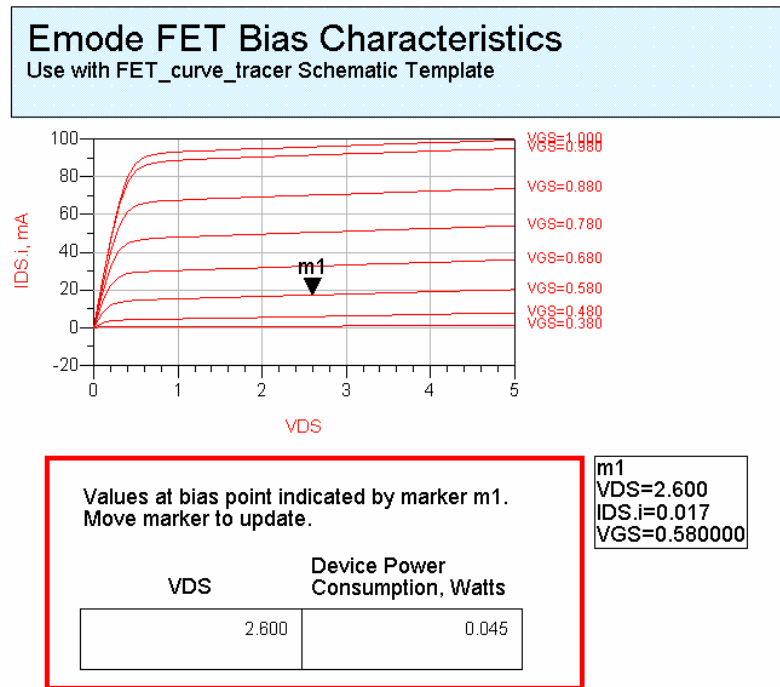
The IV curves for the E-mode FET were simulated using ADS. These curves gave insight into the current and voltage swings typical of these FETs usage in an amplification scenario. The following graphic (Figure 3) illustrates the ADS circuit used to test the FET's IV mode characteristics:

FIGURE 3 – E-mode FET IV Curves Schematic



The following graphic (Figure 4) illustrates the results of the IV simulation:

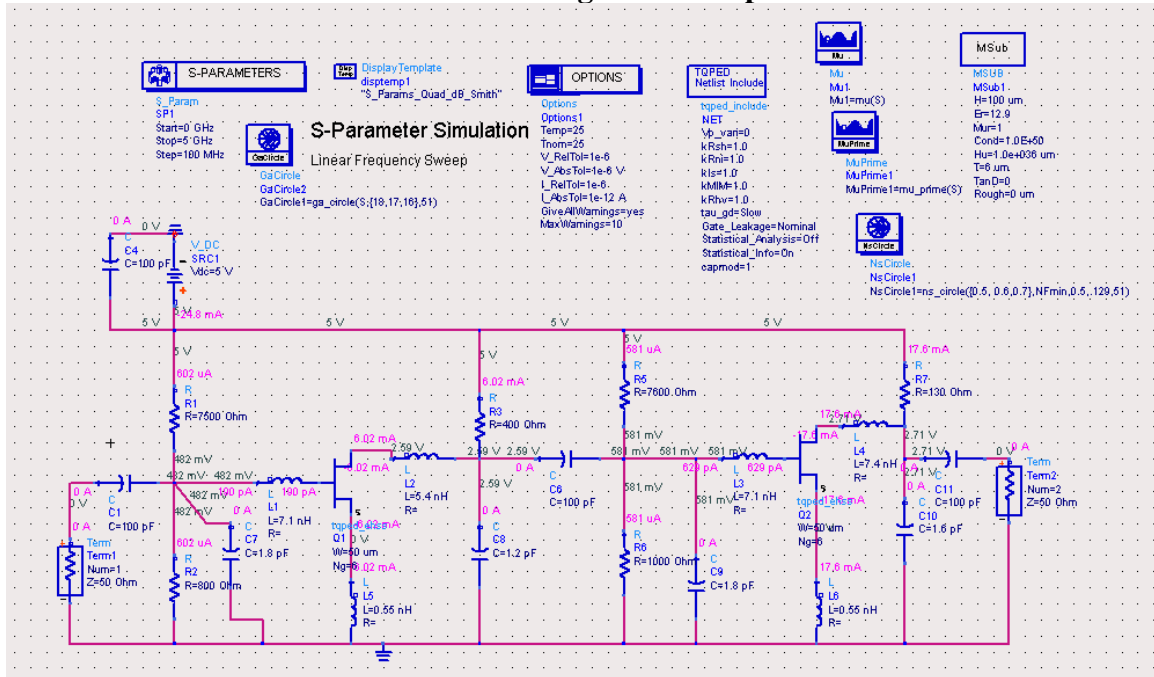
FIGURE 4 – E-mode FET IV Curves



These results show that a drain-to-source voltage (VDS) of 2.6V with a gate-to-source voltage of 0.58V would be a good choice to allow the FET to operate in the saturation region – a necessary condition for amplification. Typical drain-to-source currents would be around 0.017 A at the operating point. These values allow the DC characteristics of the LNA to be known for design purposes.

With an understanding of the input matching characteristics of the LNA design and the DC voltage characteristics needed to operate the amplifier, a two-stage design was implemented. The following graphic (Figure 5) illustrates the two-stage design:

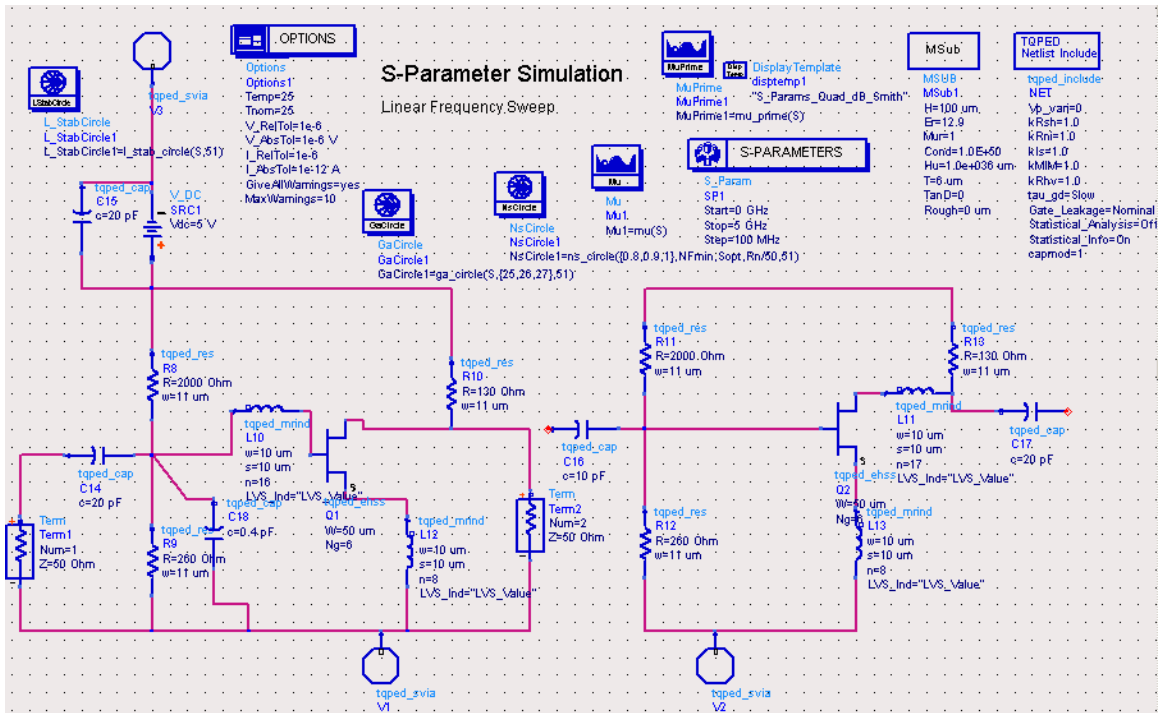
FIGURE 5 – MMIC LNA Schematic Using Ideal Components



The EHSS (E-mode) FETs employed in the circuit are the standard 300 μm (6x50 μm) package. A 100pF capacitor was used to isolate DC between the two stages. An output matching circuit was also designed to match the conjugate of the output reflection coefficient for each stage. With further analysis, the output matching network of the input stage, the input matching network of the output stage and the 100pF blocking capacitor were replaced with a single 20pF blocking capacitor to reduce the complexity of the circuit.

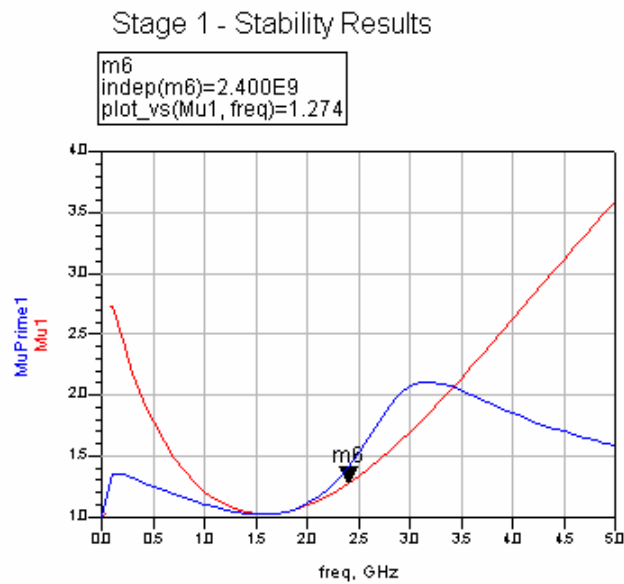
The source inductors connected to both sources were replaced with TriQuint spiral inductors and tuned such that unconditional stability was insured for each individual stage. Therefore, the cascade of the two stages would be unconditionally stable. The following graphic (Figure 6) illustrates the test circuit:

FIGURE 6 – Input Stage Stability Schematic



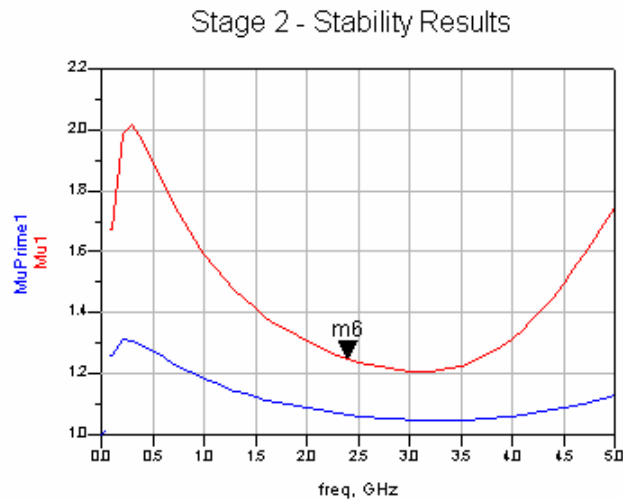
Note that the second stage has been disconnected and the 50 ohm termination placed at the output of the first stage. The following graphic (Figure 7) illustrates the results when a 100 x 100 micron, 8-loop spiral inductor was used as the source inductor:

FIGURE 7 – Input Stage Stability Simulation Results



The input stage circuitry is therefore shown to be unconditionally stable when using this source inductor. The same inductor was used for a stability analysis of the second stage. The following graphic (Figure 8) illustrates the results:

FIGURE 8 – Output Stage Stability Simulation Results

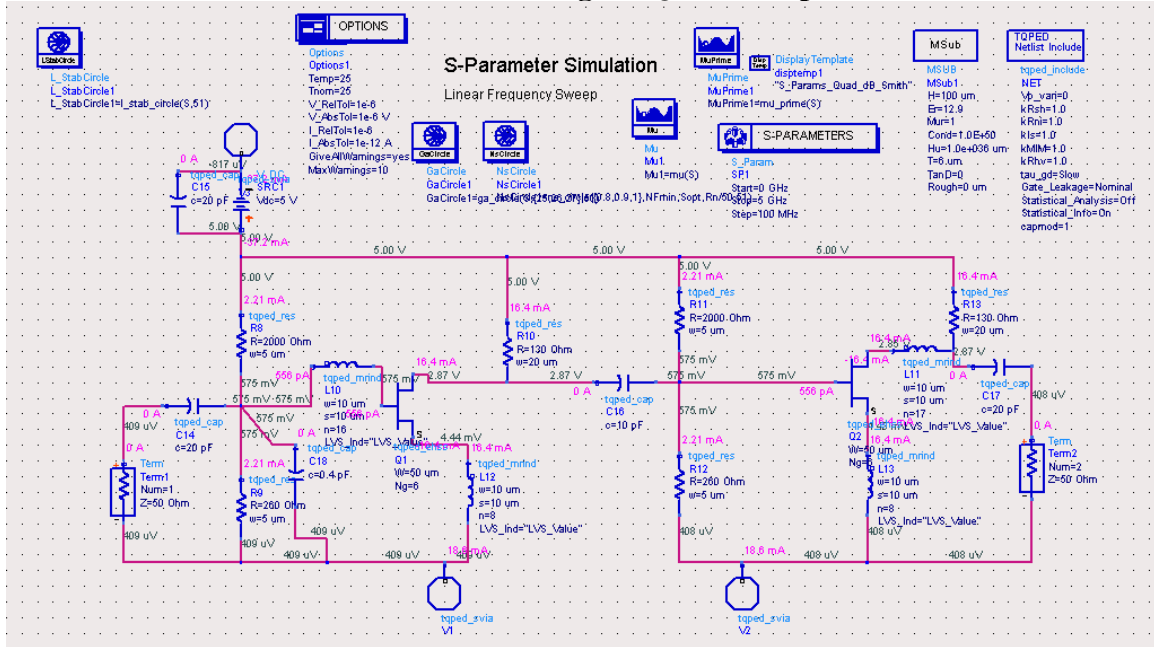


The output stage circuitry is also shown to be unconditionally stable with the 100 x 100, 8-turn spiral inductor connected at the source of the FET.

While the resistor divider networks at the input of each stage produced a minimal noise figure of 1.6 dB overall, an initial layout of the circuit showed that the 7800 Ohm resistors would cause placement of the other components to be difficult. The 7800 and 800 ohm resistors were replaced with 2000 and 260 ohm resistors at the input. This can be seen in the previous single-stage stability simulations. Also note that the drain resistor was reduced from 400 ohms to 130 ohms to maintain the DC current through the drains, as noted in the IV curves.

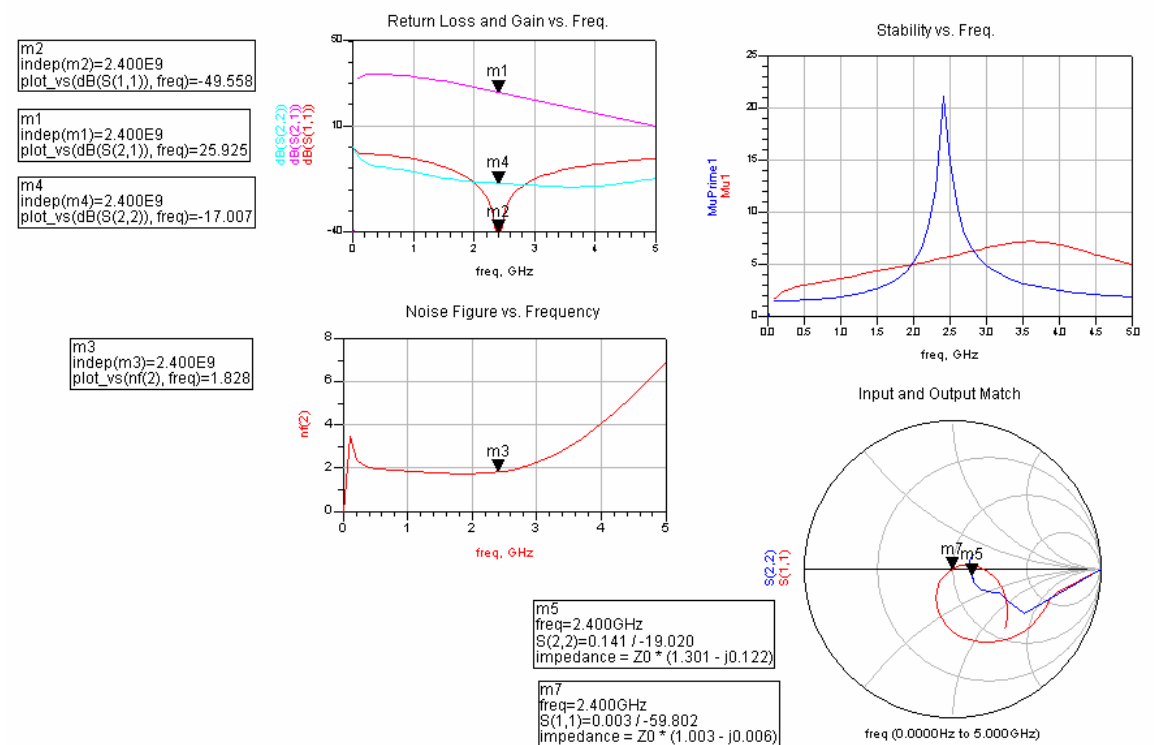
The next graphic (Figure 9) shows the final two-stage LNA circuit with the previous enhancements implemented:

FIGURE 9 – MMIC LNA Schematic Using TriQuint Components



To conserve space, the blocking capacitors were reduced to 20pF and the inter-stage matching capacitor was also reduced to 10pF. The shunt capacitor was reduced to 0.4pF for input matching purposes. The following graphic (Figure 10) illustrates the return loss (S11 and S22), gain (S21), stability, noise figure and input/output match:

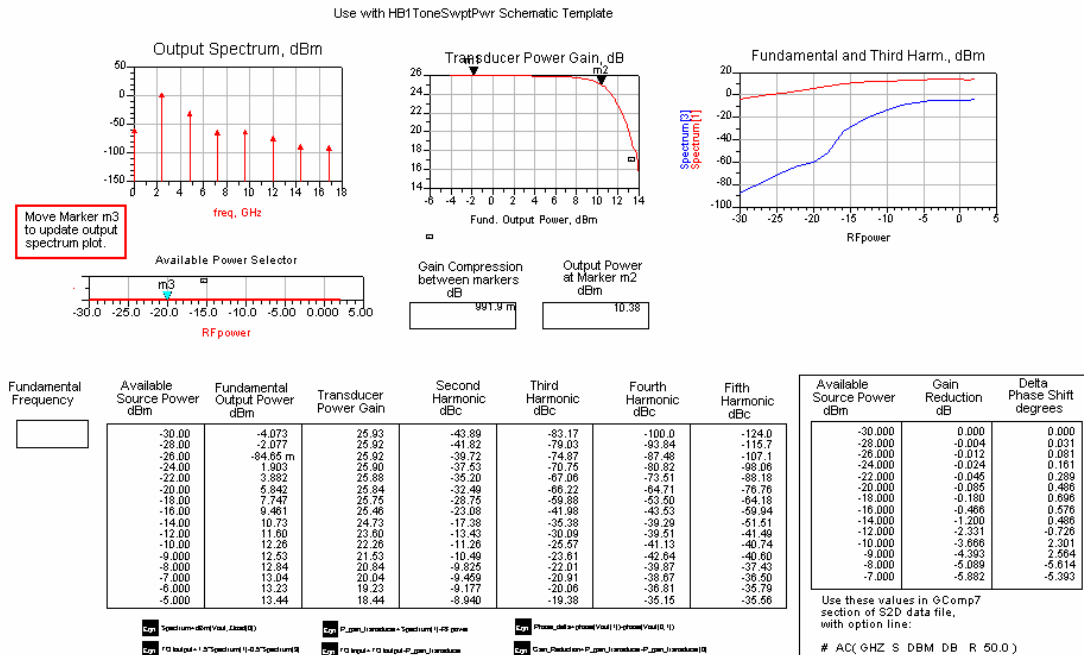
FIGURE 10 – MMIC LNA Simulated Return Loss, Gain, Noise Figure and Stability



It can be seen that with real TriQuint components used, the previous circuit will meet both the noise figure (1.828 dB) and gain (25.9 dB) requirements of the project. The circuit will also have an input VSWR of -49.6 dB and an output VSWR of -17 dB. The optimal input VSWR was obtained by adjusting the shunt capacitor size at the input. It is also shown that the circuit will also be unconditionally stable across the frequency band from 2 to 3 GHz.

The input power of the LNA circuit was swept from -30 to 2 dBm while the output was terminated with a 50 ohm resistance. The following graphic (Figure 11) illustrates the results of the sweep:

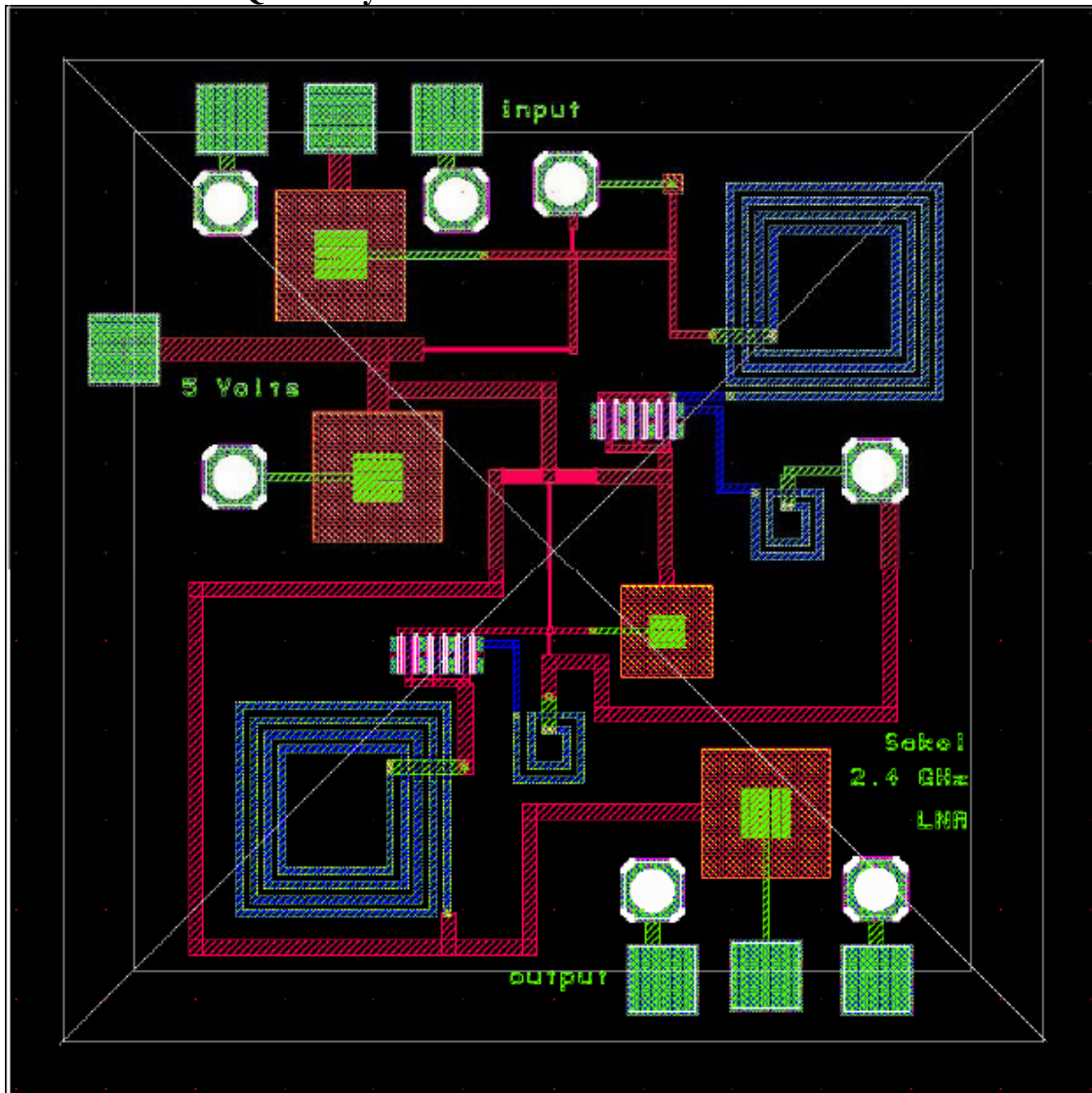
FIGURE 11 – Swept Power Response of MMIC LNA



It can be seen the input third order intercept point will be greater than +5dBm. The results from +2 to +5dBm could not be simulated as the simulation did not converge, however the trend in the chart in the upper right-hand corner indicates that the convergence point will be beyond +5dBm.

The following graphic (Figure 12) illustrates the final layout of the aforementioned two-stage LNA design:

FIGURE 12 – TriQuint Layout of MMIC LNA



The line widths for the Metal0 layers (appearing in red) were increased to allow for the current levels predicted in the DC annotation of the simulated circuit. +5 Volts is applied to the green pad labeled “5 Volts” in the upper left-hand corner of the circuit. The input to the LNA is the green ground-signal-ground pad area shown in the upper left-hand corner of the circuit. The output of the LNA is the green ground-signal-ground pad area in the lower right-hand corner of the circuit.

6 Test Procedure

The input frequency should be swept from 2.0 to 3.0 GHz. The input power level should be kept between -30 and -8dBm to assure that the higher order harmonics do not overtake the strength of the fundamental. Within this frequency band and input power level, the gain should be between 20 and 25dB, as simulated. After the network analyzer is calibrated, the S11, S22 and S21 parameters should be measured when the frequency is

swept from 2 to 3 GHz. The noise figure should also be measured across this frequency band to corroborate the design.

7 Conclusion

The previously described MMIC LNA circuit should meet the requirements specified at the beginning of the report. One source of improvement would be if the input bias circuits' impedances could have been increased. This would effectively improve the noise figure of the circuit without any noticeable degradation in any of the other performance parameters. These resistor values were optimized so that the circuit could fit within the die region.