



MMIC VCO Design

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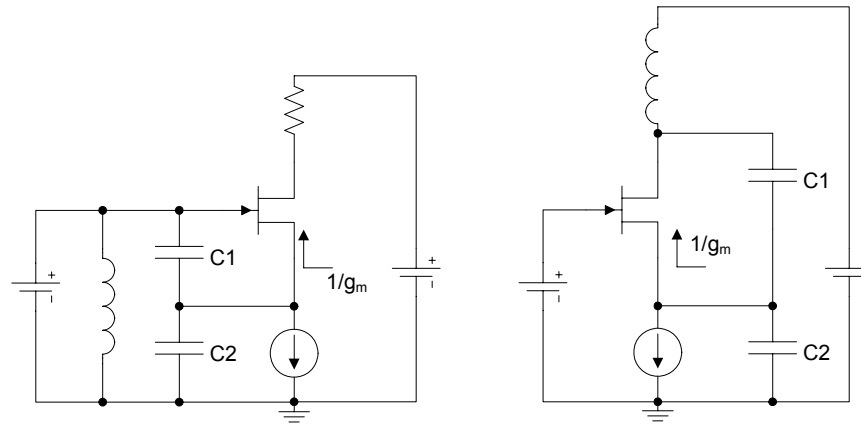
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Mr. John Penn

Goals and Specifications

- Frequency: 2305 – 2497 MHz
- Output Power: $>+7\text{dBm}$; 10dBm goal
- Control Voltage: 0 to 0.4V
- Supply voltage: $\pm 5\text{V}$; +5V only goal
- Output impedance: 50Ω nominal
- Size: 60x60 mils ANACHIP

Step 1: Choose Topology

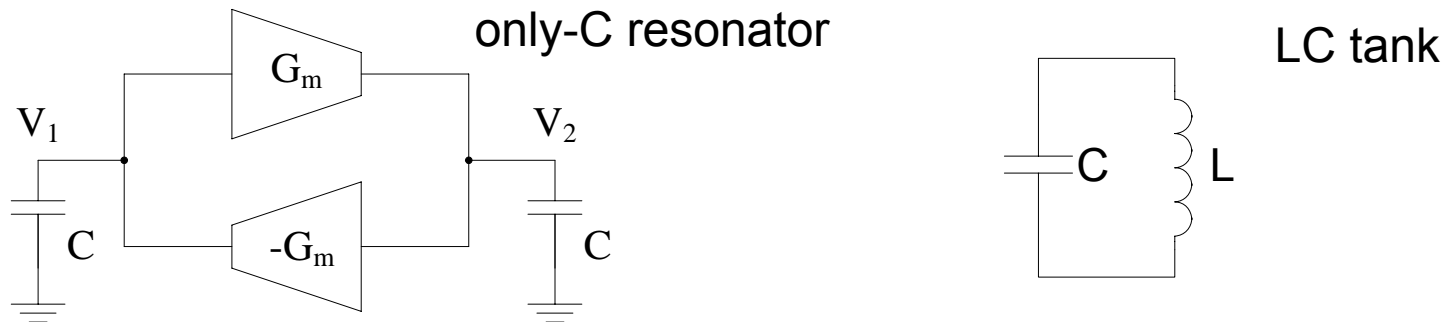
- Simple architectures using only one transistor are the Hartley and Colpitts topologies.
- Hartley employs more inductors.
- Two possible Colpitts configurations:



- Due to power specification, the configuration with the output at the drain was chosen

Step 2: Choose Resonator

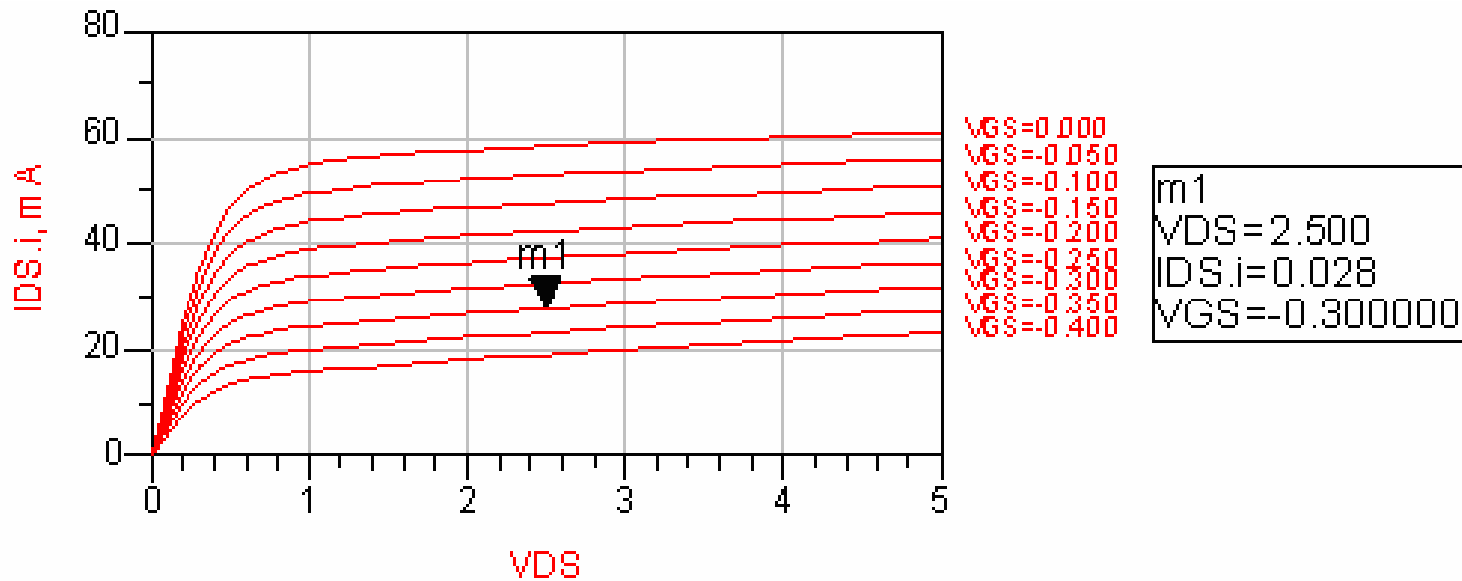
- The type of resonator in an oscillator is probably the most important part since it defines phase noise.
- Excellent phase noise can be achieved by crystal oscillators, ceramic resonators and other external devices.
- For on chip implementation, there are two basic configurations:



- Better phase noise achieved using the LC tank

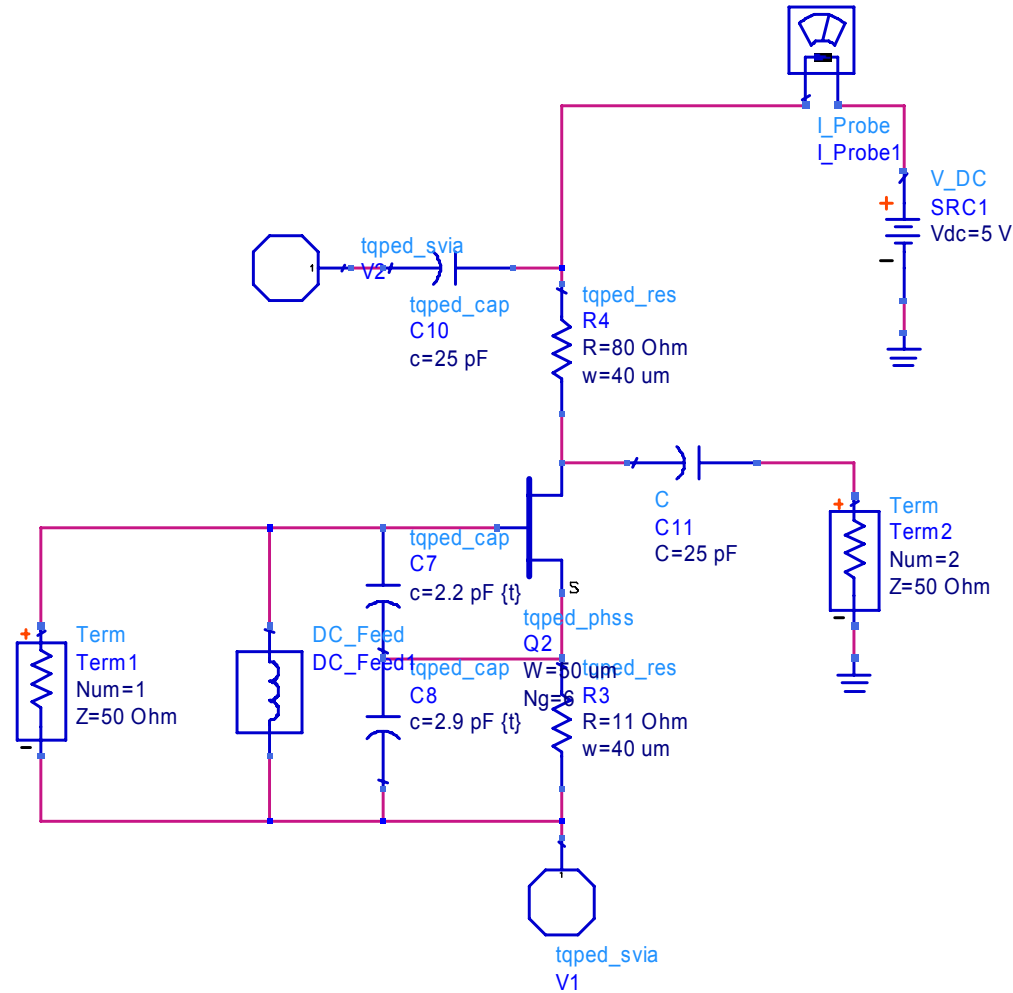
Step 3: Choose Biasing

- To reduce the number of resistors, and therefore noise, the D-mode pHEMT was used.
- For higher (output power) / (phase noise) ratio, the FET was biased at $IDSS/2$ and $VDS=V_{supply}/2$



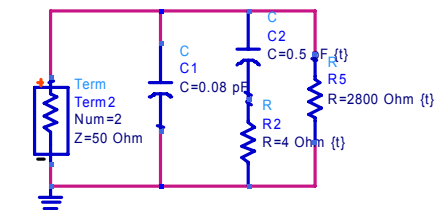
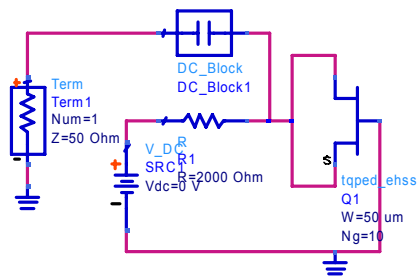
Step 4: Maximize output mapping circle (1)

- Instability can be quantified using as a figure of merit MaxMP2, the farthest point of the output mapping circle.
- MaxMP2 is the inverse of the load stability factor μ' .
- The first step in maximizing MaxMP2 was to start from the basic Colpitts topology and tweak capacitors C1 and C2.



Step 5: Choose varactor

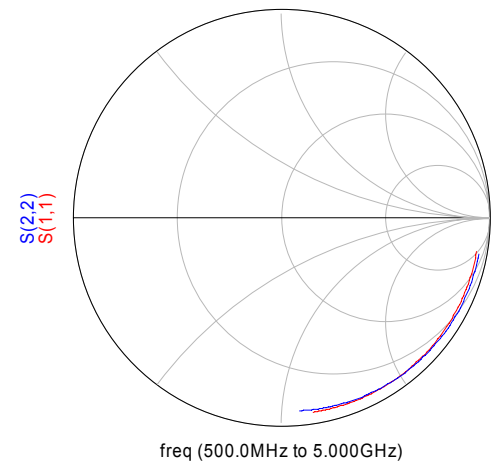
- As an on-chip varactor, a simple, diode-connected FET, reversely biased can be used.
- Goal is to find which of the FET devices has the lowest losses and capacitance.



S_Param
SP1
Start=0.5 GHz
Stop=5 GHz
Step=0.05 GHz

TQPED
Netlist Include

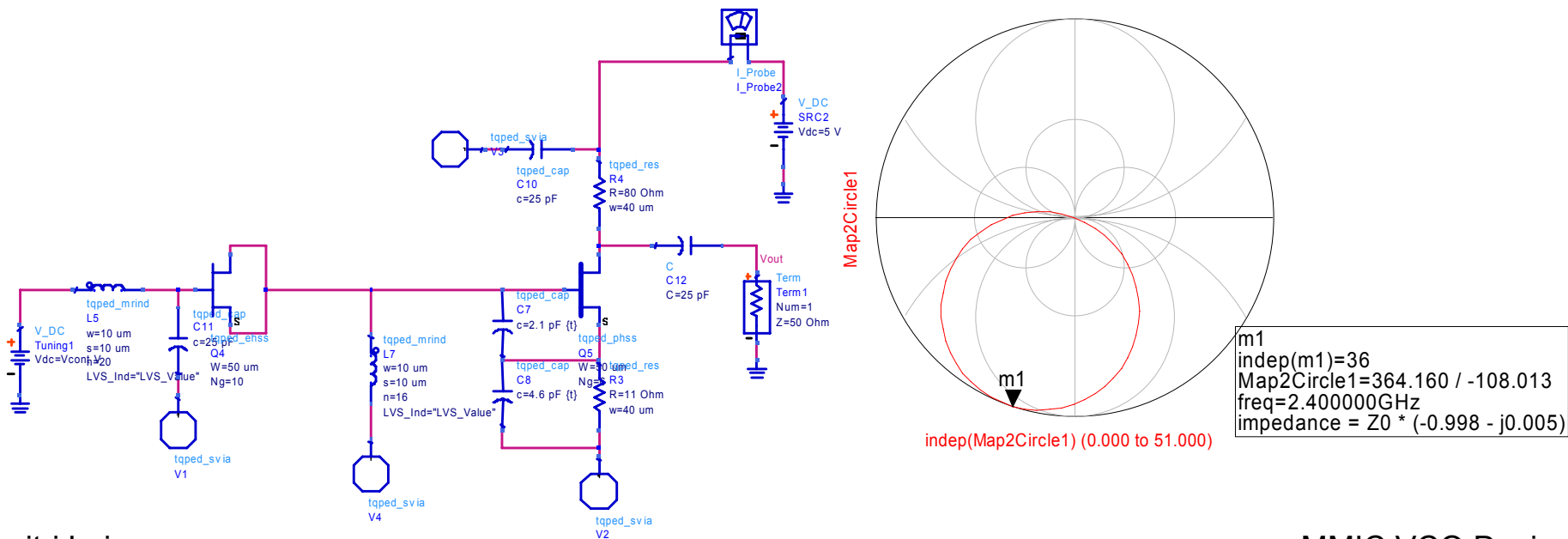
```
tqped_include  
NET  
Vp_vari=0  
kRsh=1.0  
kRni=1.0  
kls=1.0  
kMIM=1.0  
kRhv=1.0  
tau_gd=Slow  
Gate_Leakage=Nominal  
Statistical_Analysis=Off  
Statistical_Info=On  
capmod=1
```



- The E-mode pHEMT with 10 fingers of 50 μ m was found to be best.

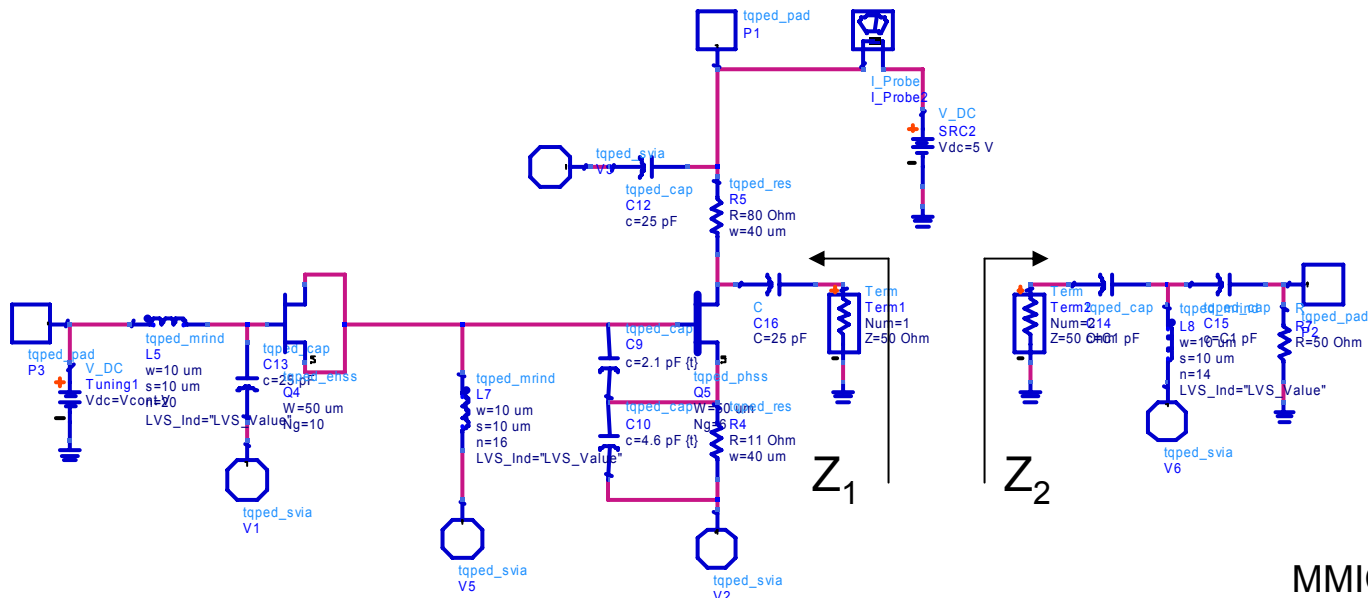
Step 6: Maximize output mapping circle (2)

- After having added the varactor and inductor, and biased the varactor at mid-range, the values of C1, C2 and L of the inductor were tweaked so as to achieve maximum MaxMP2.
- Maximum MaxMP2 led also to a maximum reflection coefficient at the drain of the FET.



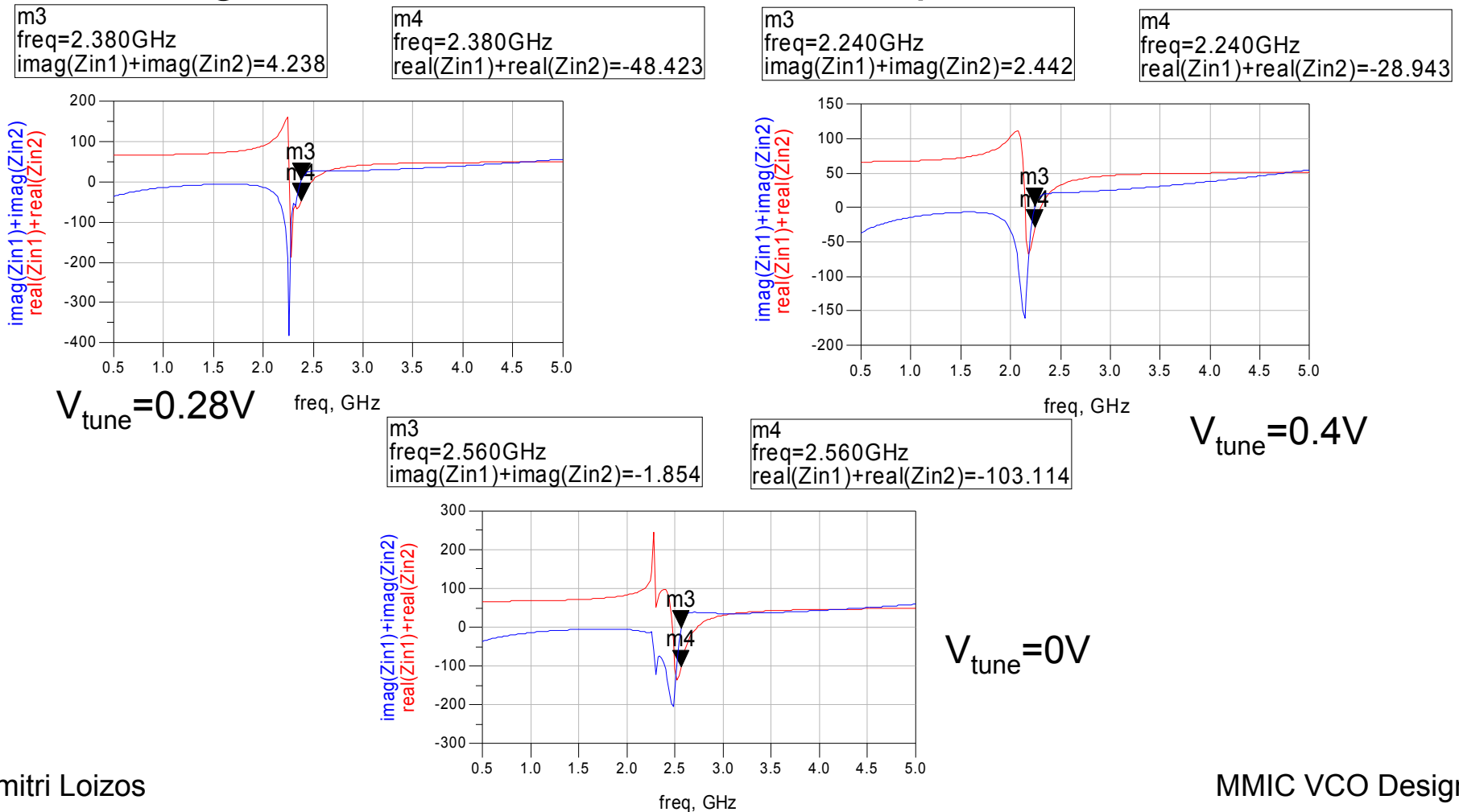
Step 7: Choose the output matching network

- Conditions for oscillations to start:
 - $\text{imag}(Z_1 + Z_2) = 0$
 - $\text{real}(Z_1 + Z_2) < 0$
- In order to reduce the real part of the load resistance, an output matching network is needed. Assuming that the load is 50Ω , a simple T-network, equivalent to a $\lambda/4$ transmission line can be used.



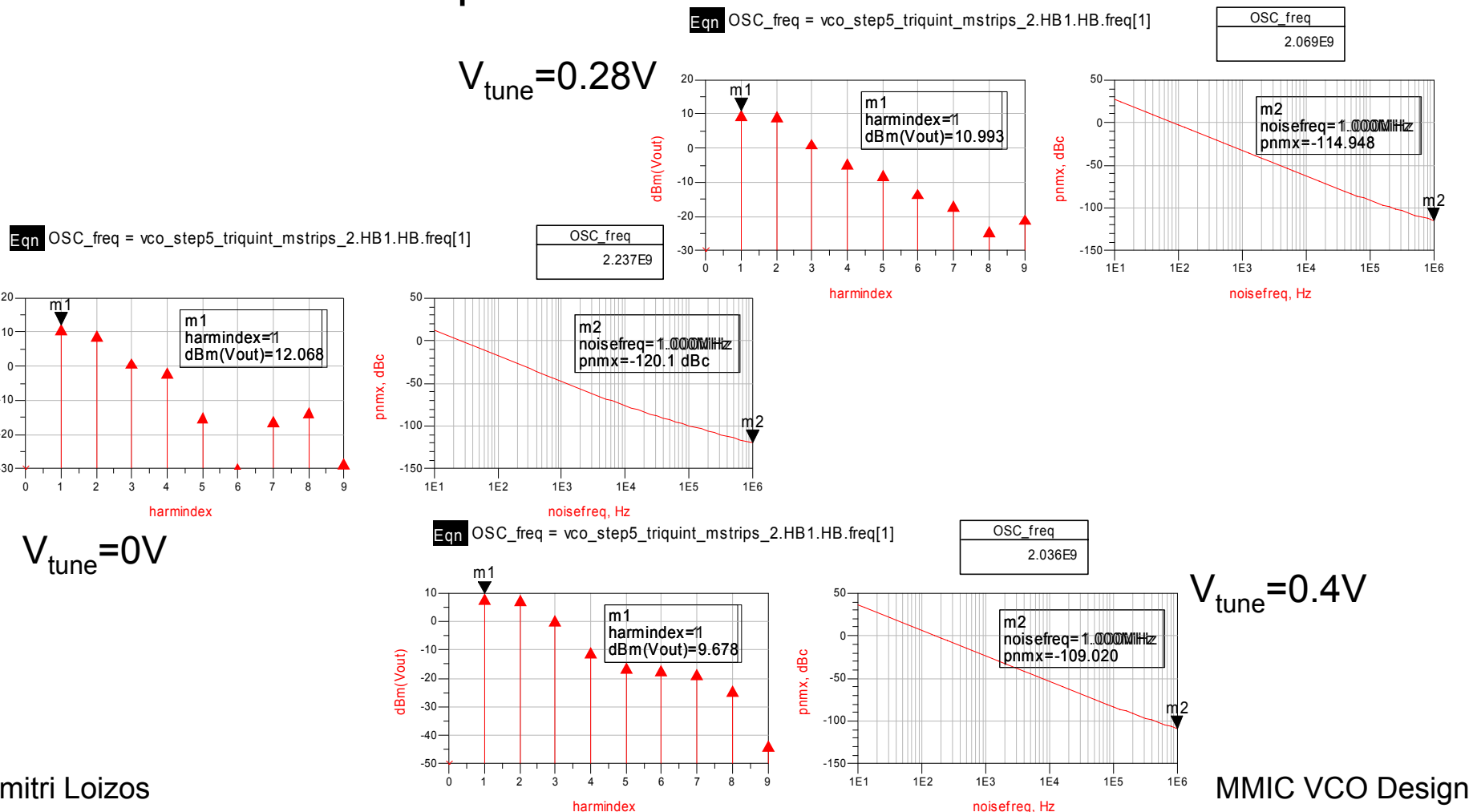
Simulation results (nonlinear solver)

- Using the previous architecture simulations for different voltage biases of the varactor were performed:



Simulation results (Harmonic Balance solver)

- Using the harmonic balance simulator, output power, harmonics and phase noise can be calculated



Nonlinear vs Harmonic Balance solver

- Comparing the simulation results between the nonlinear and HB solver, we can see differences in the predicted frequency of oscillations.
- Possible reasons:
 - The nonlinear simulator determines the frequency at which oscillations can start, but this can be different than the actual frequency of oscillation.
 - The HB solver makes some assumptions and simplifications in order to determine the describing functions of the nonlinear elements in the loop.
- Measurements will reveal which simulation method is best and how close simulation results are to the actual observed values.

Layout

