Vector Modulator

Final Report

MMIC Design EE787
Fall 2006

Design Name: jhu06vmd

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1. Abstract

A 2.4 GHz vector modulator using TriQuint's 0.5µm PHEMT process was designed and simulated. This MMIC vector modulator is capable of outputting a QPSK modulated signal with as low as 6dB of insertion loss. Two voltage supplies, one for in-phase (I) and one for quadrature (Q), are used to modulate the signal. The device is able to handle an input power greater than 0dBm. It has a VSWR of less than 1.4:1.

2. Introduction

The vector modulator that is described in this paper provides a compact, low power, and moderate loss way to QPSK modulate a signal. It is designed to operate in the S-band using wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies (2.305 – 2.497 GHz). The states of the vector modulator are achieved by changing the voltage of the I and Q inputs to different combinations of +0.5V and -0.7V. For example by setting the I and Q inputs both to +0.5V there will be a 45° phase shift. Though any point inside the four corners can be obtained as well. The corner points fall at ±45° and ±135° with a constant amplitude for QPSK.

The design was done on GaAs using TriQuint's 0.5µm PHEMT process. The simulations and layout were done using Agilent's Advanced Design System (ADS). All the data presented in this paper is simulated using TriQuint's design kit components. All the components in the design are lumped elements, because of the size of a wavelength relative to the chip dimensions. Much more detail will be provided including expected performance plots throughout the paper.

3. Design Approach

The goal for the vector modulator design was to QPSK modulate a signal to be transmitted. The basics of the design came from a paper written by J. Penn, see references. The design uses a 90° hybrid at the input to split the signal in I and Q with the isolated port terminated. Then a variable attenuator is used to adjust the amplitude of the I and Q signals independently. As described in Penn's paper, the variable attenuators are reflective attenuators using a 90° hybrid and two FET transistors as the variable resistors. Then the two signals are added together yielding a phase and amplitude shifted signal. Though for QPSK the amplitudes are the same, but the phases are 90° apart starting at 45°.

I started the design by creating a simulation of the basic building blocks of the vector modulator. I used ADS system passive components for the 90° hybrid and Wilkinson splitter as is similar to the simple schematic shown in section 5. I used this to explore the learn how to operate the vector modulator. I discovered that the vector modulator can be used for any amplitude and phase based modulation schemes, since any point inside most extreme points can be used. The downfall of using point closed to the origin than the corners is the loss is very high. This is explained in more detail in the following paragraphs.

From there I designed the blocks using ideal lumped elements. Because of the limitation of space and the small size of a MMIC, transmission lines could not be used. So I converted the design of the 90° hybrid and Wilkinson splitter to lumped elements using the Pi network model.

At this point I chose a transistor size that was a compromise between resistance and capacitance for the variable attenuator. The transistor acts as variable resistor using the gate voltage to tune it.

The reflective attenuators are key to changing the amplitude and phase of the signal. They work by adjusting the amount of mismatch-induced reflection caused by the variable resistors. The signal enters the 90° hybrid then splits equally with a 90° phase shift on the one port. When the resistor is an open circuit or a short circuit all the power is reflected back to the hybrid. It is then combined at the isolated port, theoretically having no loss. When the resistors are 50Ω, assuming this is a 50Ω system, none of the power is reflected the resistor dissipates it all. Therefore there is maximum attenuation when the resistors are 50Ω. In the case of this design the transistors have a nominal resistance and a maximum resistance. This is why the insertion loss of this design is a minimum of 6dB. Also the capacitance of the transistors causes the insertion loss to vary with frequency. The balance of resistance and capacitance in the transistors is explained in section 3.2.

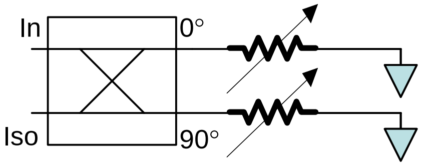


Figure 3-1: A diagram of a reflective attenuator using a 90° hybrid and two variable resistors.

I then replace the ideal components with TriQuint models and converted ideal inductors to spiral inductors. I then optimizing each piece of the design for insertion loss, return loss, and phase in the case of the 90° hybrid. I paid special attention to the phase flatness of the 90° hybrids, because the accuracy of the phase is important to avoid excess loss in the reflective attenuators. If the two signals are not 90° apart they will not complete combine at one port and completely cancel at the other.

When adding interconnect, I used metal 2 where ever I could. Because of metal 2's thickness it would be the lowest loss metal without stacking two layers. Since the frequency is only 2.4GHz the skin depth is quite large relative to the metal thickness. Metal 2 would give the maximum amount of skin depths to avoid excess attenuation. Also when connecting the pieces of the design together I used 35µm wide line, where possible, to reduce loss and lower inductance.

At this point in the design I decided to add capacitors between the reflective attenuators and the Wilkinson splitter. These caps simply, rotate the phase of the constellation so that the corners are at ±45° and ±135°.

Finally I made modifications required to properly layout the design to fit on the 60 x 120 mil chip. During layout I chose to share some vias to conserve space. I chose to keep the layout symmetric putting the input and output on the 120µm sides of the chip and the I and Q on the 60µm sides. I also needed to put vias at the ground pads at the edge of the chip for the input and output. This is described further in section 3.2.

3.1 Specifications vs Goals

All specifications are met or the expected performance is better.

	Specified Performance		Expected Performance
Specs	Goal	Max	from Simulation
Frequency	2.305 - 2.497 GHz		> 2.305 - 2.497 GHz
Isolation	16dB	10dB	> 20dB
Loss	7dB	10dB	10dB Max
RF Input Power	0dBm		0dBm Min
VSWR	1.5:1	2.5:1	1.4:1
Supply Voltage	0 - 5V Variable		+0.5V, -0.7V

3.2 Tradeoffs

When picking a transistor for the variable attenuator part of the vector modulator, there was a tradeoff of the drain to source resistance and capacitance. As the size of a transistor gets larger, resistance reduces, thus lower loss, but the capacitance get larger as well. The converse is true for a small sized transistor.

Another tradeoff I dealt with was in the layout. A design rule for vias is that they can not be as close to the edge of the chip as the pads. At the input and output of the layout I did not have room to put vias on the inside of the ground probe pads. The trade off was making room by moving the input 90° hybrid and Wilkinson splitter closer together, increasing the chance of coupling of the input to the output bypassing the attenuators or running long lines from vias to the pads. I opted for the latter choice for two reasons. One is that the lines required to connect the vias to the pads are long, they are still a tiny fraction of a wavelength at 2.4GHz and since I used 50Ω line there shouldn't be any extra inductance causing a problem. The second reason is that since we have vias, when the chip is mounted in a package the ground pads do not need to be used. So the risk is coupling weighted much heavier than moving the vias.

4. Simulations

In the design of the vector modulator I ran three different simulations. One is a single 2.4GHz small single S-parameter simulation to generate a constellation digram. Two is a swept frequency small single S-parameter simulation to check the loss and VSWR of the device. The third is a harmonic balance simulation to measure the output power.

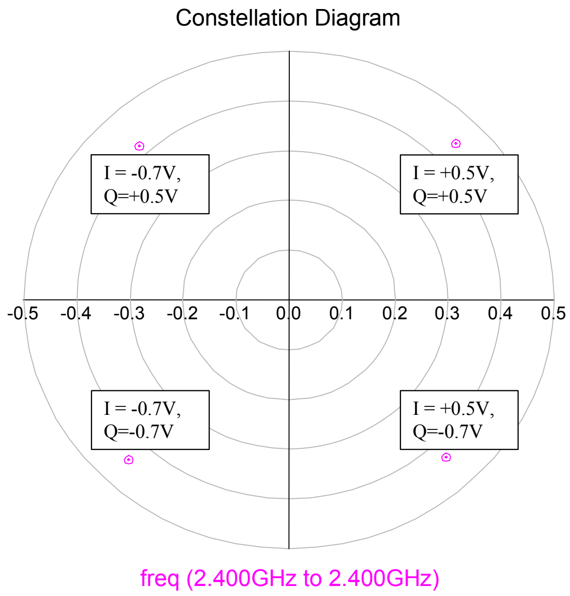

Constellation Diagram

Figure 4-1: The constellation diagram shows the QPSK modulated output signal. Displayed is S21 on a polar plot at 2.4GHz.

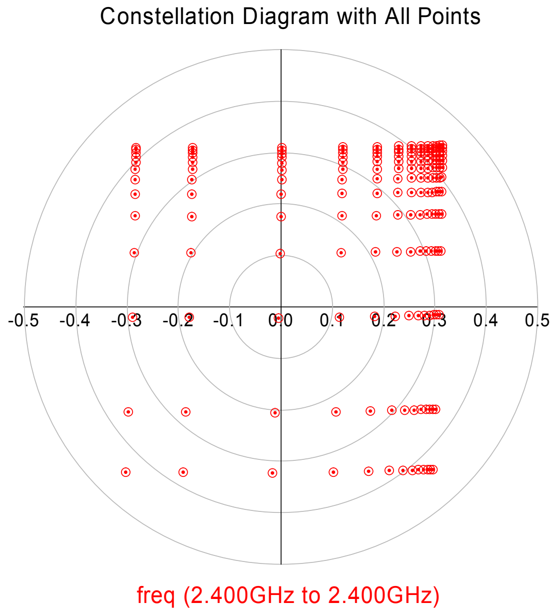

Constellation Diagram with All Points

Figure 4-2: Since the input to the I and Q ports is a DC voltage, any point inside the corners is possible.

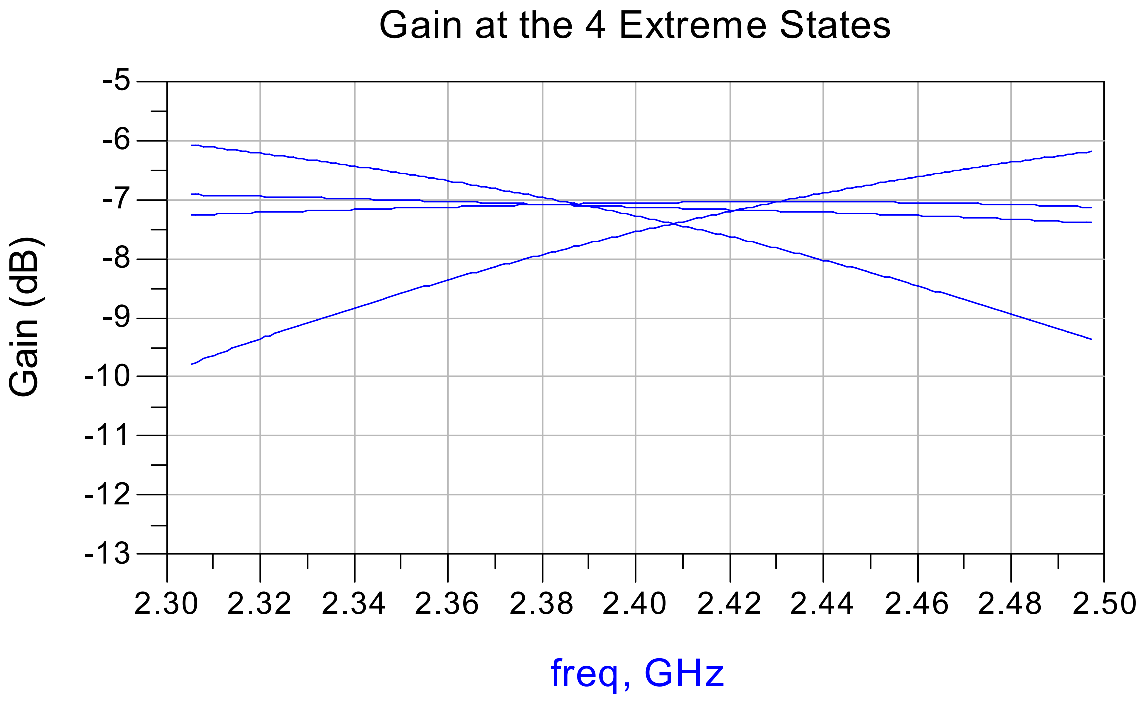


Figure 4-3: The insertion loss of vector modulator plotted over frequency shows the amplitude slope when the transistors are at a high impedance state because of the capacitance. The greatest loss is less than 10dB, which is within the spec.

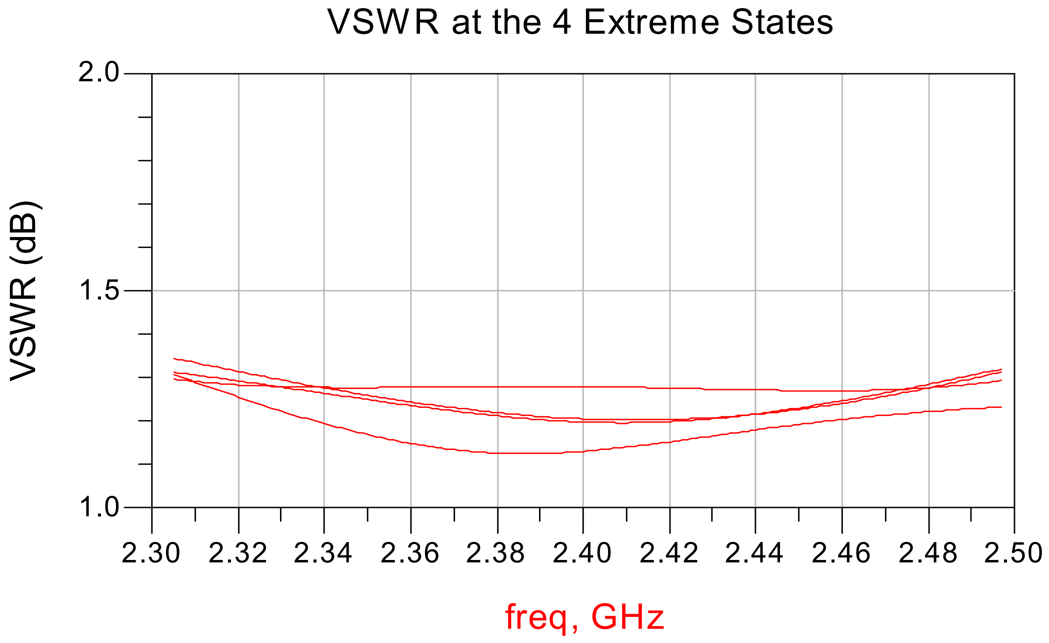


Figure 4-4: The VSWR of the vector modulator in all states is less than 1.4:1, which is better than the spec.

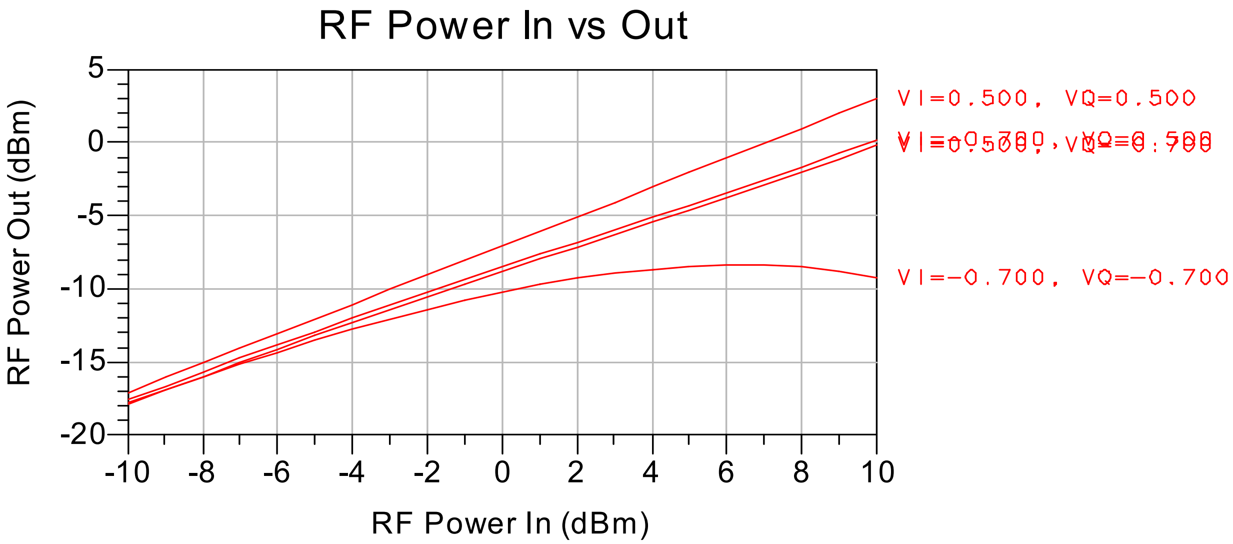


Figure 4-5: The vector modulator can handle an input power of 0dBm as stated in the spec. Only the I=-0.7V, Q=-0.7V case has any gain compression over this input range.

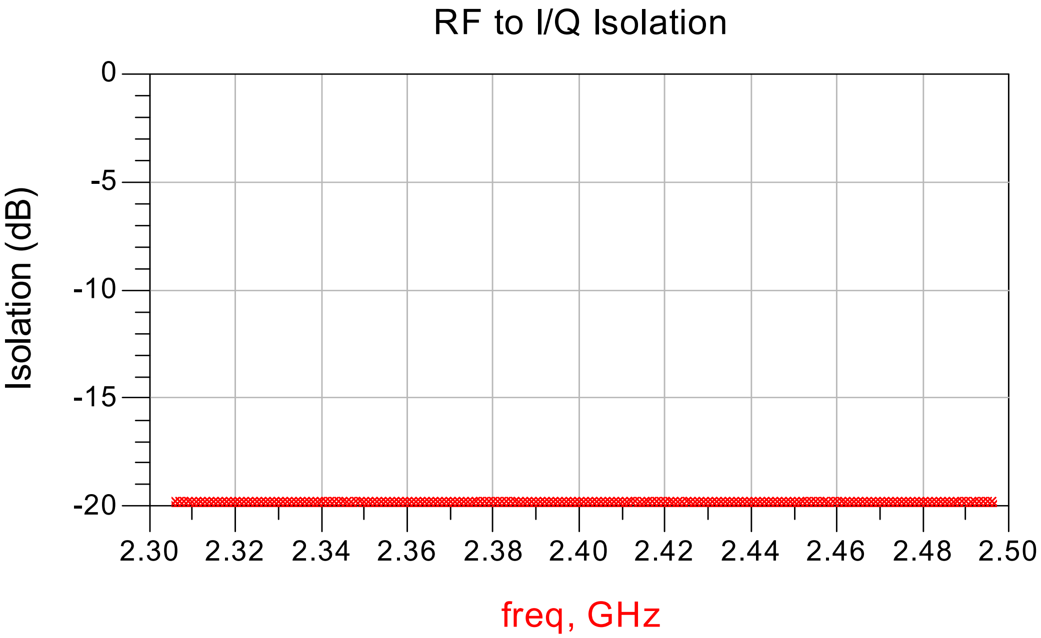
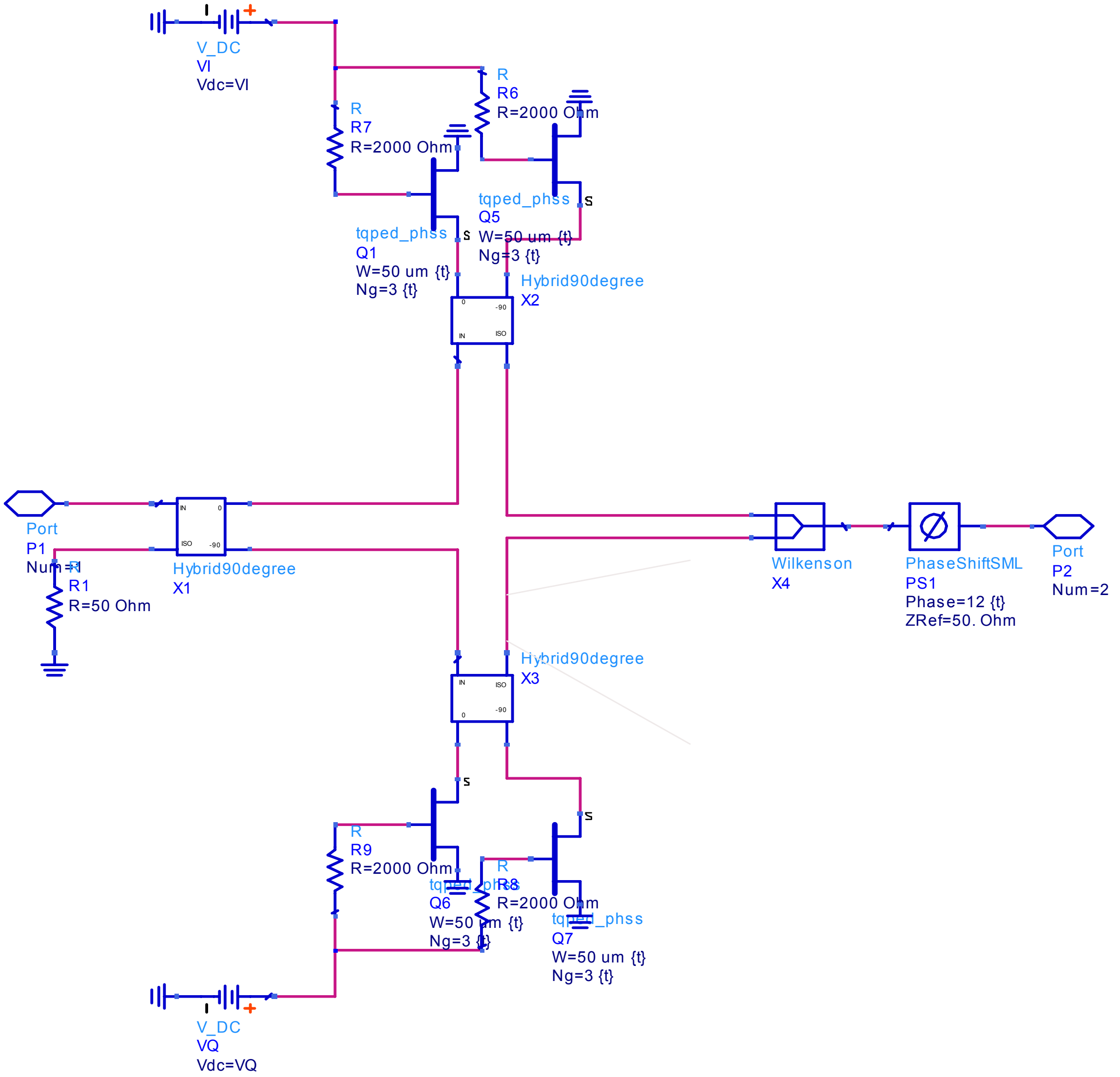


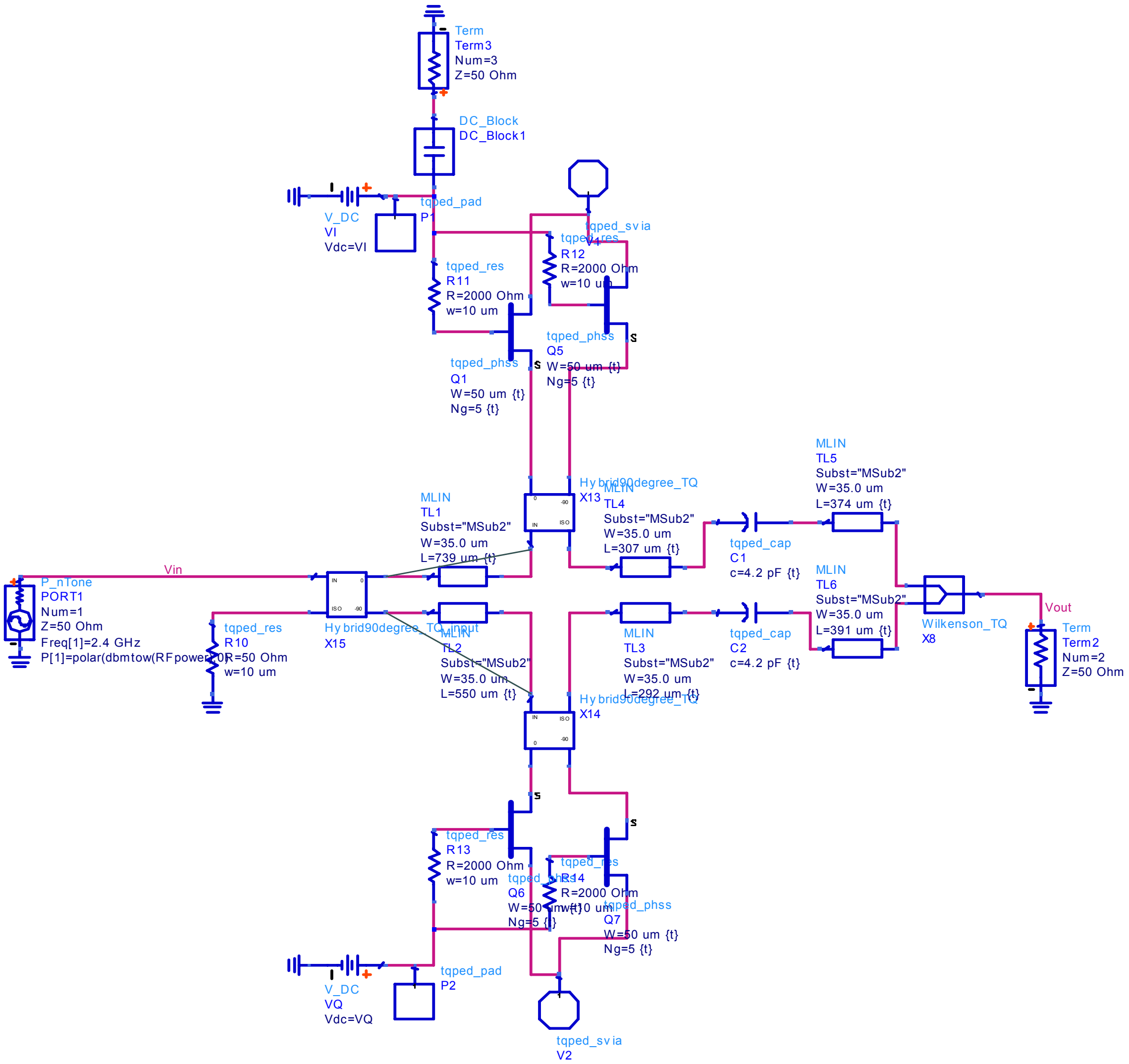
Figure 4-6: The RF to I/Q isolation is too high for ADS to calculate it. So it should be better than the spec of 16dB.

5. Schematic

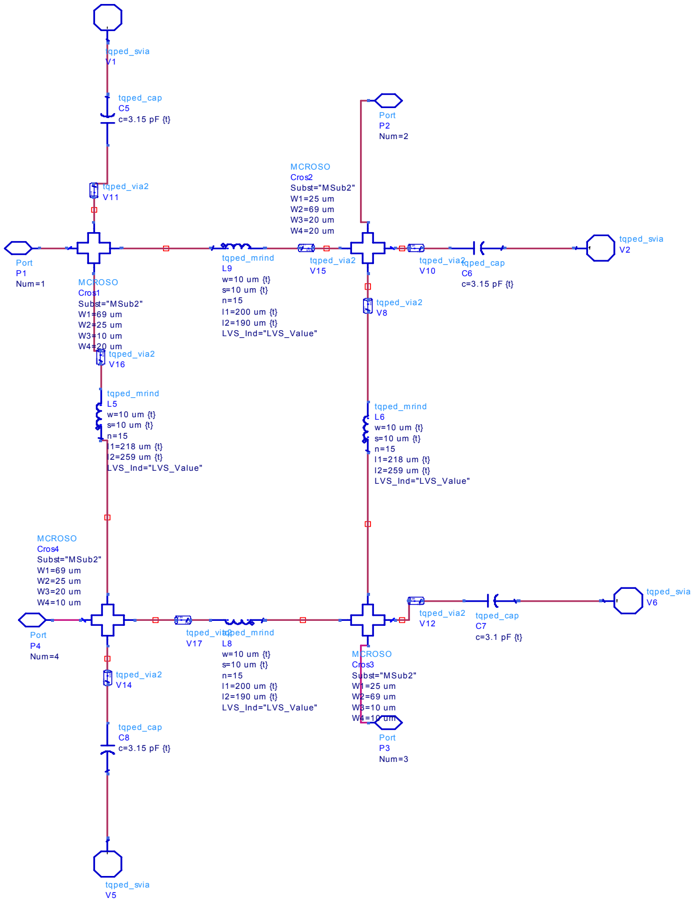
Simple Schematic



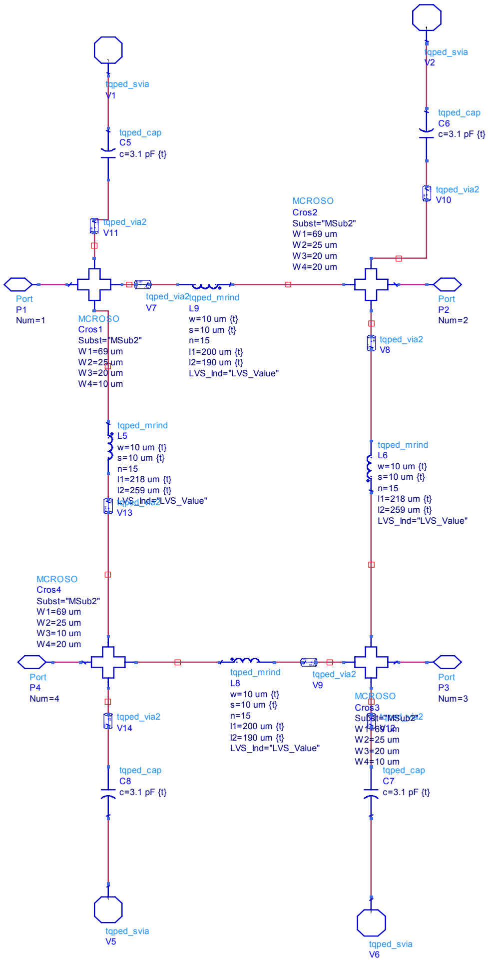
Final design schematic



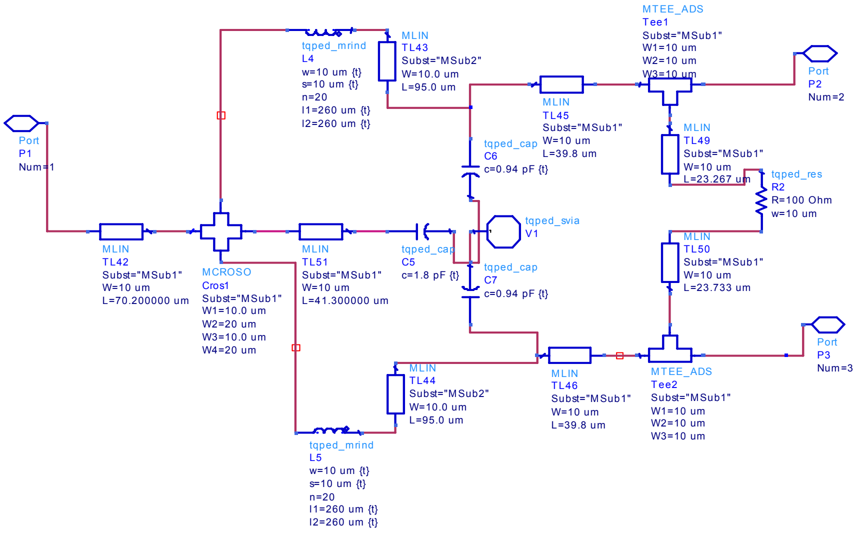
Input 90° hybrid



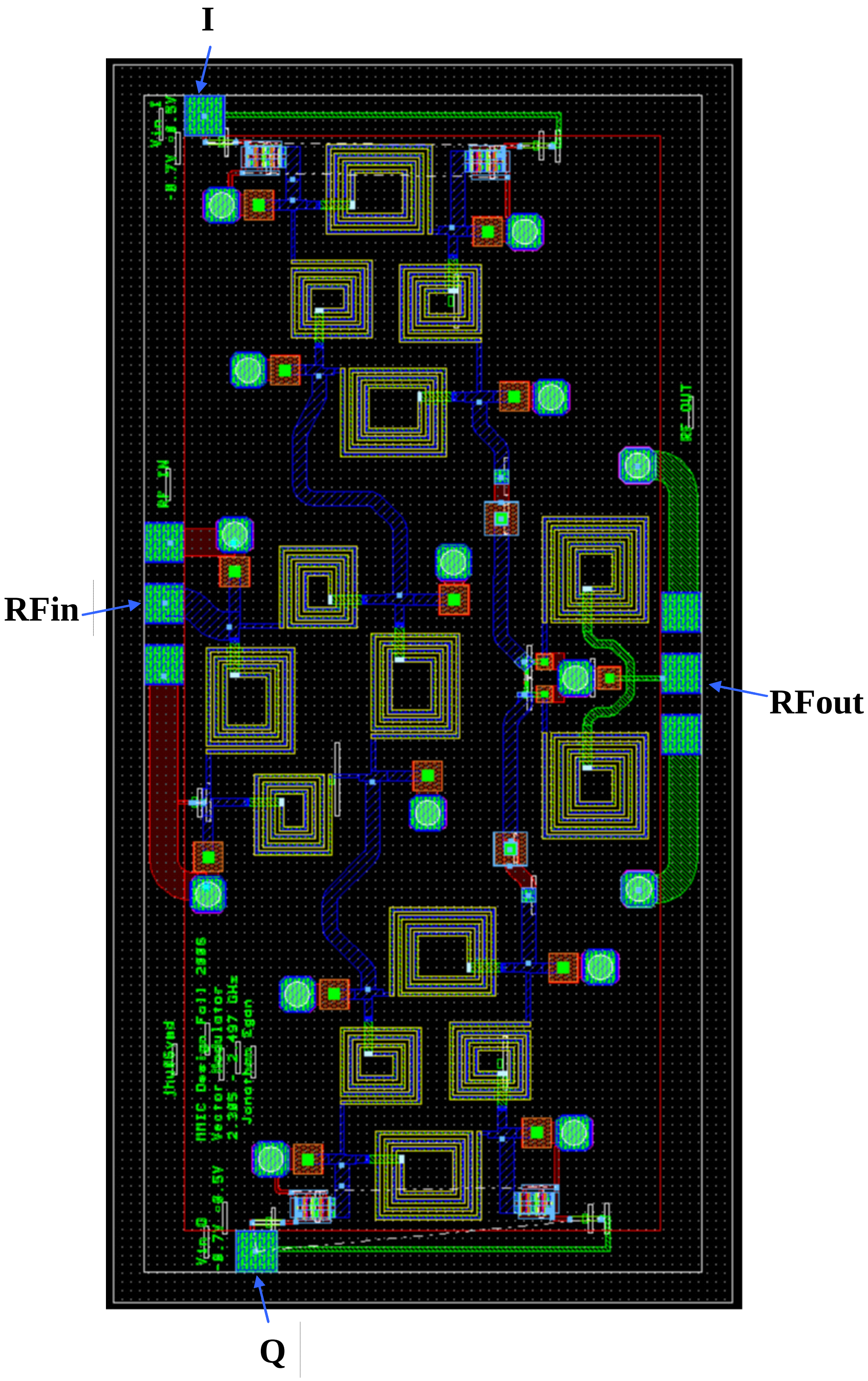
Variable Attenuator 90° hybrid



Wilkinson splitter



6. Layout


I
Vin_I
-0.7V @0.5V
RF_OUT
RF_IN
RFin
RFout
MMIC Design Fall 2006
Vector Modulator
2.305 - 2.497 GHz
Jonathan Egan
Vin_Q
-0.7V @0.5V
Q

7. Test Plan

7.1 Equipment list

Vector Network Analyzer
2 DC supplies

7.2 Test Procedure

7.2.1 Calibrate the network analyzer from at least 2.3 to 2.5 GHz with 201 points.

7.2.2 Set up the chip on the probe station using two GSG probes and two single pin DC probes. The placement of the probes is labeled on the layout see section 0.

7.2.3 Apply voltage to the I and Q ports using the table below. Other voltages, between +0.5V and -0.7V for either port, can be investigated.

Phase Table		
Voltage I	Voltage Q	Phase shift (degrees)
0.5	0.5	45
-0.7	0.5	135
-0.7	-0.7	-135
0.5	-0.7	-45

8. Summary and Conclusions

The vector modulator described in this paper is capable of QPSK modulating a signal from 2.305 to 2.497 GHz. It makes use of FET transistors to vary the phase and amplitude of the signal. The I and Q inputs to the vector modulator range from +0.5V to -0.7V. The small size and frequency range should make this a chip an important component of an S-band wireless system.

9. References

Penn, John E. “A Balanced Ka-Band Vector Modulator MMIC.” Microwave Journal, June 2005.