

MMIC Design of a Small Signal Amplifier

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Abstract

IN this design we are interested in developing a small signal amplifier (SSA). The design will encompass a two stage topology. Each stage will use 300um devices. The goal is to reach a gain 20dB. All design simulations will be accomplished in ADS 2005. In this paper there will be a step by step short discussion of the approach to the final design. Each stage will be discussed in detail. We will discuss the order of development for stage one followed by the development of stage two.

Introduction

There is a need to create a small signal amplifier that will put of a gain requirement of 20dB. It appears that our single device is capable of delivering more that 20 dB of small signal gain. It appears that the first attempt at designing an SSA for 20dB would be to use a single stage to accomplish this task. We will discuss later on in the conclusion that it is not a good idea to squeeze the life out of one device. This SSA will use two stages. We arbitrarily use a 300um triquint device that we got from school. (in a real world application the device would be measured and characterized such that the small signal gain is obvious. To start the design, the device is biased with Vgs of -0.5v and Vds at 5v. See fig1 for IV curves.

Design Approach

To start we simulate GMax of the 300um device. It appears that we can get more than enough gain for designing the first stage. A series RLC feedback network is inserted between the gate and drain to reduce the gain to a level of about 15 dB. See fig1b. In this attempt at lowering the gain, we realize that some gain will be lost when the stages are cascaded. The large resistor value (~700ohm) in the series RLC feedback helps control the level of the low frequency gain and stability of the device. See fig1c & fig1d. The there is also a resistor at the gate of stage one device. This resistor helps with stability as well as raising and lowering the high end gain. Observing figure 1d we clearly have enough gain in our frequency band of interest (10dB). Our next step is to design the matching networks.

Looking at the device drain impedance we see approximately $56+j44\text{ohm}$. We want to match to the conjugate or $56-j44\text{ ohm}$. Observing the location of the drain impedance on the smith chart we can match the drain to 50 ohm with a series inductance and some shunt capacitance. See fig 2a.

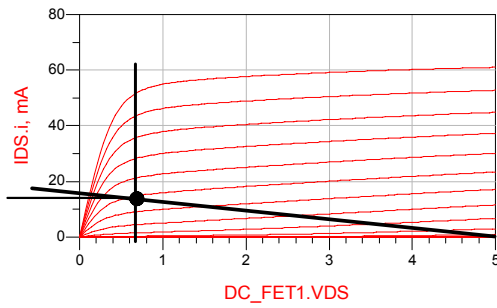


Fig1a

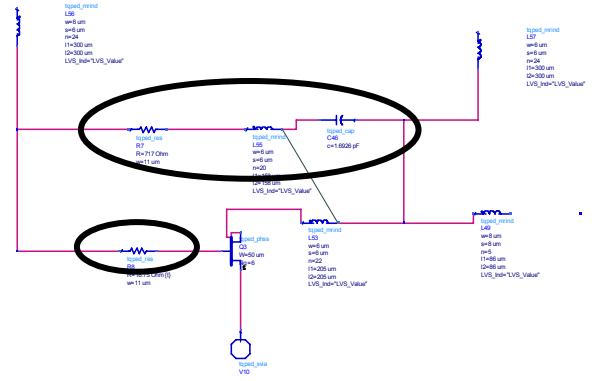


Fig1b

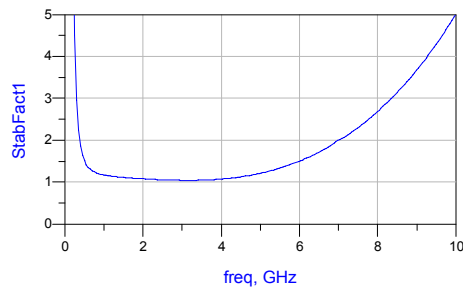


Fig 1c

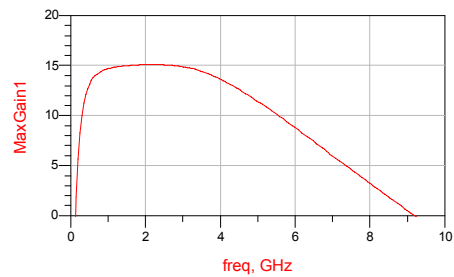


Fig 1d

The results of the series inductor can be shown in the figure below.

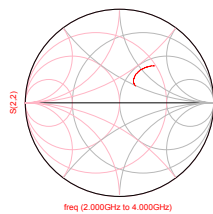


Fig 2a

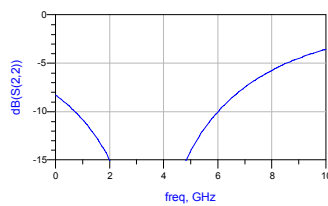


Fig2b

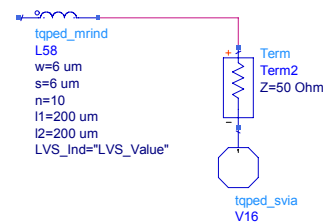


Fig2c

We are now interested in matching the input of our device to 50 ohm. The impedance of the gate with the feedback and stability resistor attached reads 39.7-j67ohm. See fig3a.

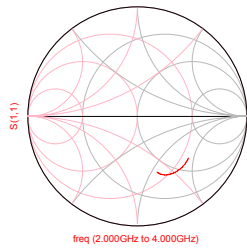


Fig 3a

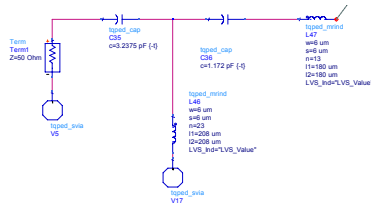


Fig3b

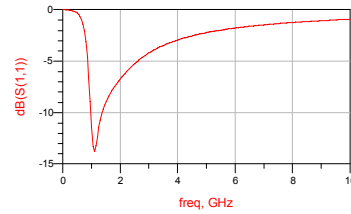


Fig3c

The conjugate impedance transformation from the gate to 50ohm can be accomplished with a series inductor and capacitor and some shunt capacitance. See fig3b. The response of the first single stage amplifier is showed in fig 4a and fig 4b.

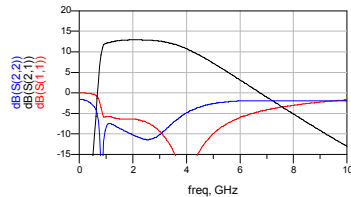


Fig 4a

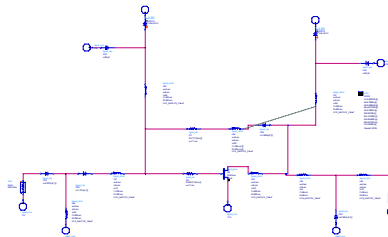


Fig4b

This first stage has a gain of approximately 12~13dB and bandwidth of 2-4GHz. At first glance the response of input and output matching networks appears to need tuning. Since the second stage will be cascaded the elements of the matching networks will be optimized as a last step. The first stage OMN needed two additional elements to facilitate the impedance match to the second stage. At this point we will begin the design of the second stage.

The second stage is treated like a new single stage amplifier design. The device is biased at the same bias points as stage one. A series RLC feedback network is employed in the second stage also. The feedback network for the second stage is used to lower the gain further to approximately 10dB. The shape of the response of the entire two stage cascaded amplifier is governed by the second stage device. The resistor in this feedback network is approximately 265ohm which lowers gain more than the 700ohm resistor in stage one feedback. There is also a series resistor at the gate of device 2. Resistor is added to the gate as an initial attempt to stabilize the device. It is observed that the resistor also helped flatten the gain response at the high end when tuned (looking at Gmax). The stability in this design is primarily controlled by the feedback. In the plot below shows the device with out any stabilizing network. Adding an RLC feedback network between the gate and drain stabilizes the device. Observing figure 5b we can see the effects of the feedback on stability.

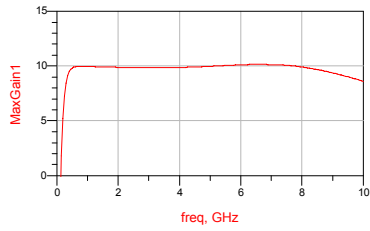


Fig5a

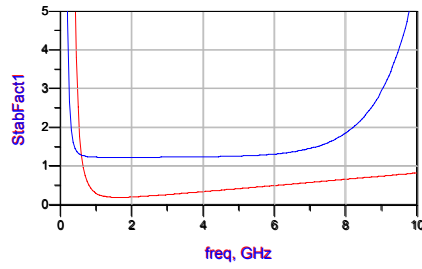


Fig5b

In designing the matching networks for stage two we follow the same procedure for stage one. The impedance is observed at the gate and drain of the device. Looking at the drain of the device the impedance is approximately $59 + j23.6$ ohms. The impedance necessary to transform the device drain to 50 Ohms can be in any combination of series inductors/ capacitors, shunt caps/inductors.

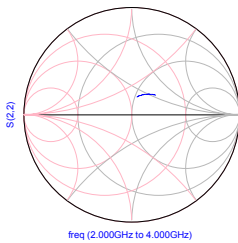


Fig6a

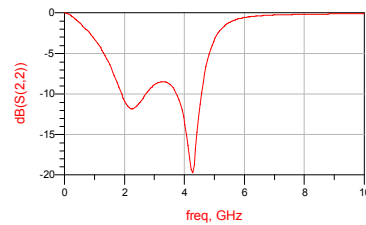


Fig6b

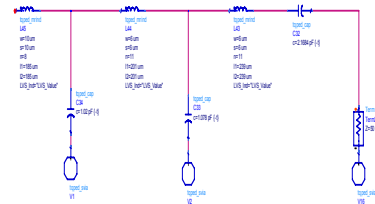


Fig6c

In this approach I chose a low pass configuration that transforms the conjugate of the drain to 50ohms. At this point the impedance at the gate is observed to read $58 + j46$ Ohm. This impedance can be viewed in fig 7a below on the smith chart.

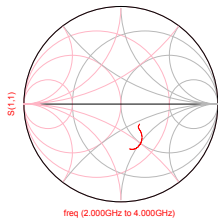


Fig 7a

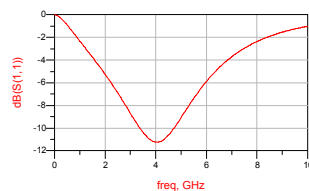


Fig 7b

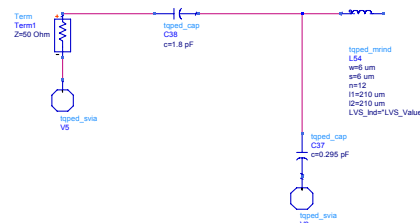


Fig 7c

To transform the conjugate of this impedance to 50ohm, a series inductance and shunt capacitance is used. The single stage as well as the results is shown in figure 8a and figure 8b. At first glance we can see that the total gain between stage one and stage two will give us the gain and bandwidth that we need.

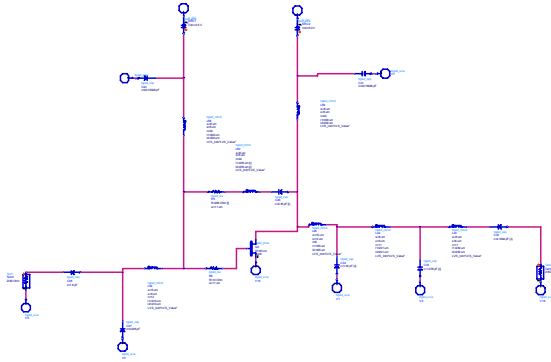


Fig 8a

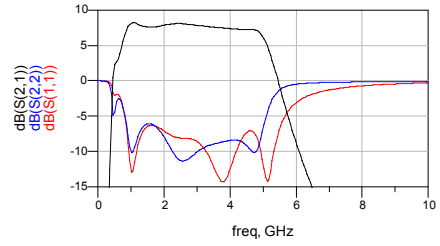


Fig8b

In order to meet our design specification the stage one and stage two amplifiers are cascaded. The final two stage circuit is optimized to improve on the overall response.

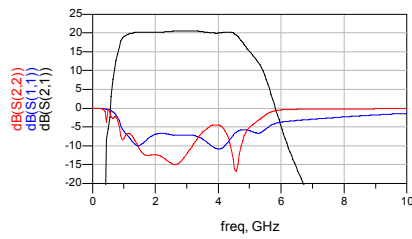


Fig 9a

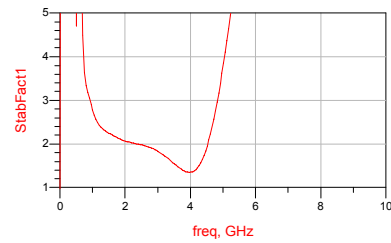


Fig 9b

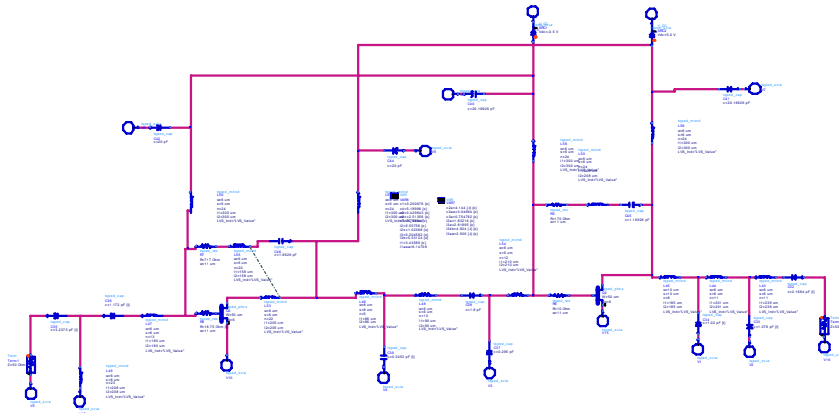
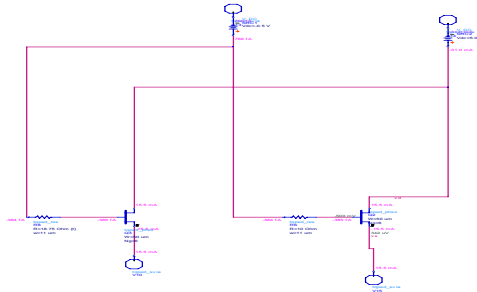
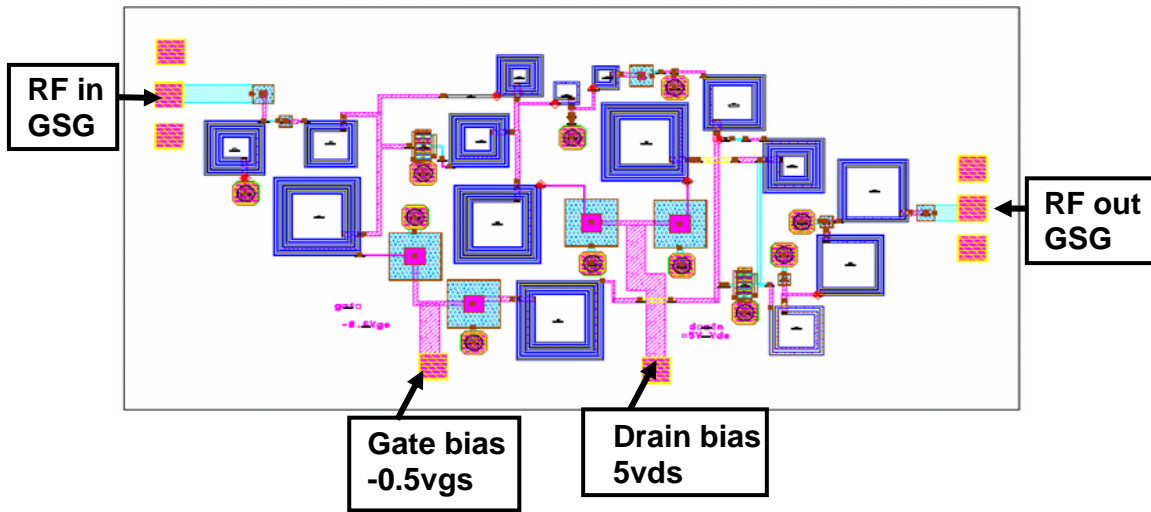


Fig 10



DC schematic



Layout

Test Plan

RF testing 100 MHz to 10GHz 100MHz steps
 S11, S12, S21, S22

DC Bias
 Vds 5V
 Vgs -0.5V

In summary, we designed an SSA with a small signal gain of 20dB. Each stage is designed individually and integrated into one amplifier. The input and output return loss could be better. The trade-off is the bandwidth.

In conclusion, there were a few lessons learned in the design of the SSA of which only the most important one will be discussed here. One important consideration is that it is easier to use two devices instead of one device when maximum gain as well as bandwidth is important. This design we were successful in meeting the design requirements for a two stage SSA.