

# THREE BIT PHASE SHIFTER

MMIC Project Final Report

EE525.787 Fall 2007

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## Abstract

A three bit phase shifter was designed for frequencies 2.305 GHz to 2.497 GHz, with delay bits of 45, 90, and 180 degrees. Each delay bit is switched between reference and delay using two control lines, either -2V and 0V, to shut off and turn on a path, respectively. Depletion, or D mode, FETs were used for switching. The circuit was fit into a 60 mil x 60 mil GaAs chip, to be fabricated by TriQuint Semiconductor Inc.

## Introduction

A three bit phase shifter has been designed for the John Hopkins University Fall 2007 MMIC design class, EE525.787. The phase shifter was designed as a part of an S-band duplex transceiver, and is used in the receive mode, as depicted in Figure A. The frequency band of interest falls between 2.305 GHz to 2.487 GHz, which covers the wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies.

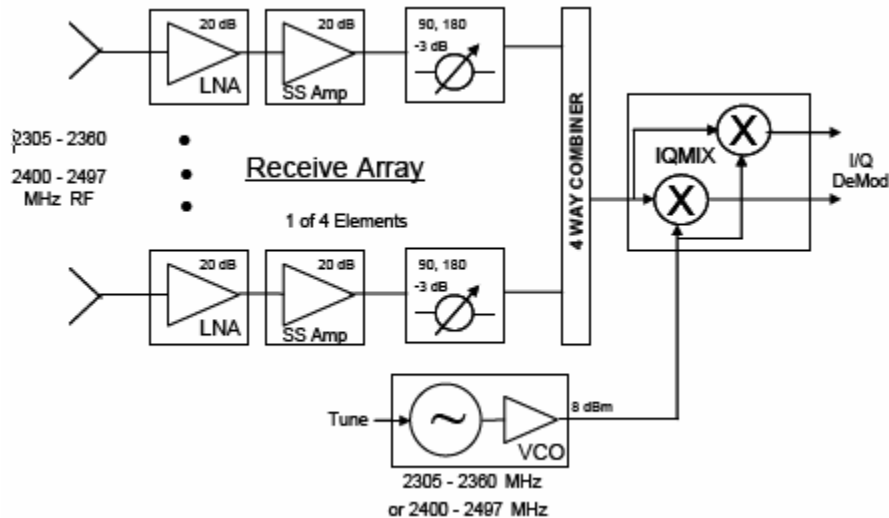


Figure A. S-band duplex transceiver for JHU EE525.787 MMIC design class, receive path

The phase shifter comprises three individual phase shift units, 45°, 90°, and 180° bits, which provides phase shift levels from 0° to 315° in 45° increments. Each bit would require two switches according to the configuration in Figure B.

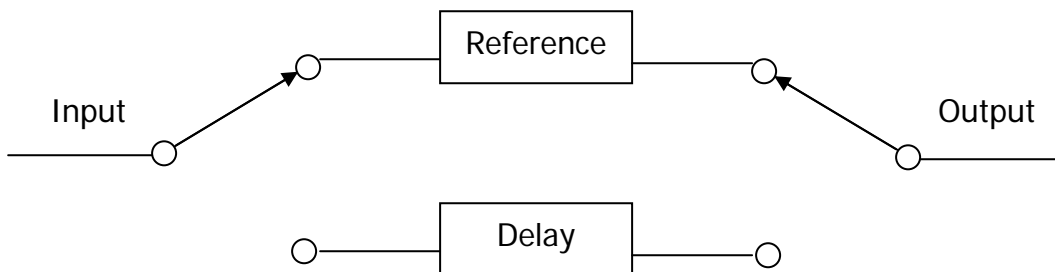


Figure B. General phase shift bit configuration

This report details the design, simulation, layout, and test plan for this phase shifter design.

## **Design Approach**

### *Phase delay circuits*

An important aspect to remember when designing a phase shifter, or any sort of delay circuit, such as a digital time delay unit, or a digital attenuator unit, is that it is the relative difference between the reference and delay circuits that is important. In other words, when designing, for example, a  $90^\circ$  phase shifter, it is not important that the reference circuit produces  $0^\circ$  of phase shift while the delay circuit produces precisely  $90^\circ$ . It only matters that the phase of the reference circuit subtracted from the phase of the delay circuit equals  $90^\circ$ . There may be applications that dictate the absolute values of the sub-circuits in addition to the relative difference, but in this instance, as well as in most applications, the absolute values are not crucial. More crucial is usually size constraints of circuit components.

In this design I found that it was much easier to design the reference and delay circuits around 0 degrees of phase, for example,  $-45^\circ$  and  $+45^\circ$ , than it is to design say  $0^\circ$  and  $90^\circ$  degrees. In the latter case, additional effort is required to achieve an identical phase sloping in frequency for a flat relative difference. In my experience, if the reference and delay circuits are designed to deviate more or less equally from 0 degrees in opposite directions (e.g.  $-45^\circ$  and  $+45^\circ$ ) the resulting frequency sloping of both circuits usually end up matching without any additional effort to make it so. This may or may not apply to wide-band applications of which this is not.

In this design I aimed for  $-90^\circ$  and  $+90^\circ$  to compose the  $180^\circ$  shift,  $-45^\circ$  and  $+45^\circ$  for the  $90^\circ$  shift, and  $-25^\circ$  and  $+20^\circ$  for the  $45^\circ$  shift. Those absolute numbers serve as an aim and as guidelines, but final values actually deviate slightly, so long as the relative values are maintained.

The general topology used for any phase shift is a T-network, with a parallel inductor between two series capacitors, where possible, to reduce the area required by the MRIND inductors. Some circuits needed series inductors and a parallel capacitor to meet performance requirements, and that was allowed so long as the sizing was reasonable. Figure 1 shows the circuit topology, with layout interconnects inserted, for the  $-25^\circ$  phase shift (reference) used in the  $45^\circ$  shift bit. Notice that the via for the parallel capacitor is connected through Port 3 at a higher hierarchical level.

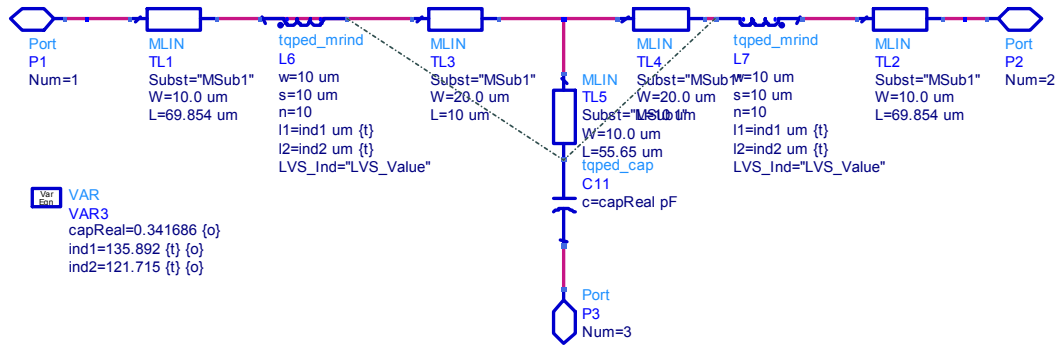


Figure 1. -25 degree phase shift topology

### Switches

Initially the topology pursued for the switch was a parallel FET and then a series FET on each switch path (four FET's total). The rationale for the parallel FET was to pull the signal to ground when the path is switched off. However, when that topology introduced too much loss, the parallel FET's were removed. It turned out that two FET's alone could still perform the job well as a switch.

Since the goal was TTL for the control bits, initially enhanced mode FET's were used for the switches for more straightforward voltage control. But when that resulted in unpredictable and deviant behavior whenever multiple phase bits were turned on, the E mode FET's were switched to depletion mode FET's instead. D mode FET's produced more stable behavior for all phase shift levels. Figure 2 below shows the switch topology used.

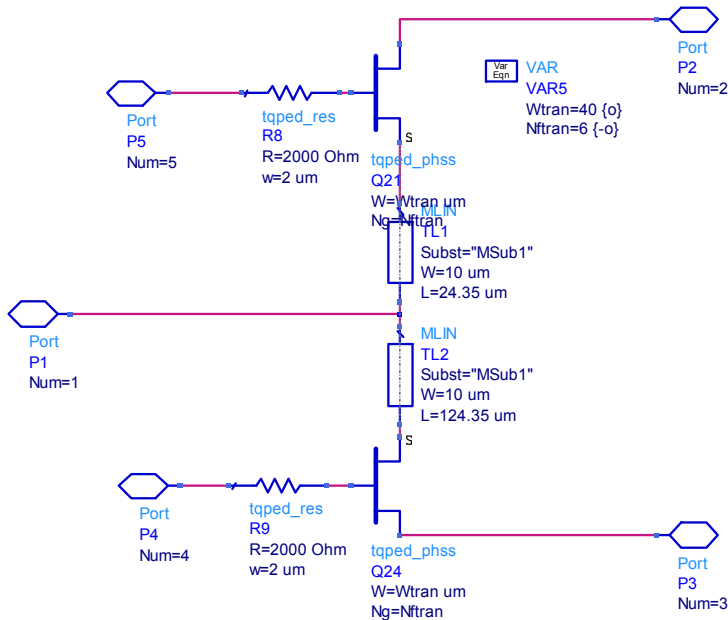


Figure 2. Switch

### Top Level Design

Due to time constraints an inverter or voltage converter were not designed which would otherwise simplify the control bits for the phase shifter. Figure 3 shows the top level circuit topology. In the end each shifter bit required two complementary control lines of 0V and -2V, to switch on and off the paths, respectively.

Once the switches are connected with the reference and delay circuits to make all three delay bits (i.e. 45°, 90, or 180° bits), the order in which they are arranged impact the VSWR (or return loss) or the total circuit. Figure 3 shows that the order that was found to be most beneficial to reducing total VSWR is from RF in to first the 90° bit, then the 180° bit, and finally the 45° bit which connects to RF out.

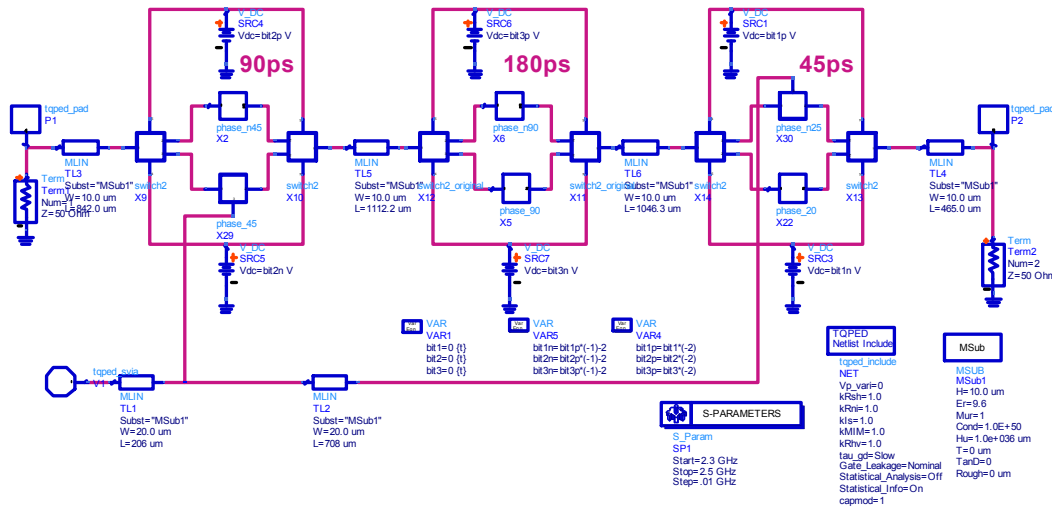


Figure 3. Top level phase shifter topology

Table 1 below shows the specifications for this design as well as the achieve simulation results with all layout interconnects included.

Table 1. Specifications and simulated results

	<i>Specification</i>	<i>Simulated Results</i>
<b>Frequency</b>	2305 to 2497 MHz	2305 to 2497 MHz
<b>Insertion Loss</b>	< 5 dB	5.6 < IL < 6.3 dB
<b>Insertion Balance</b>	+/- 1 dB	+/- 0.35
<b>Phase Shift</b>	Steps 45°, 90°, and 180°	Steps 45°, 90°, and 180°
<b>VSWR, 50 Ohm</b>	<1.5:1 input and output	<1.59:1 for 180° shift <1.5:1 for all other degree shifts
<b>Control</b>	TTL	0V, -2V
<b>Size</b>	60 x 60 mil “ANACHIP”	60 x 60 mil “ANACHIP”
<b>Phase accuracy</b>	½ LS bit, or 25°	< +/- 3°

## Simulations

Figure 4 shows the simulated results for the final phase shifter adjusted for all layout interconnects. Notice that the plot shows phase shifts starting from  $360^\circ$  ( $0^\circ$ ), so that  $315^\circ$  equals the  $45^\circ$  phase shift,  $270^\circ$  equals  $90^\circ$ , and so on. The results show a phase shift deviation of less than  $\pm 3$  degrees per phase level. The plots also show that except for one phase step (which is not labeled but is the  $180^\circ$  shift level), all VSWR results meet the 1.5:1 spec. The switches, however, introduced more loss than desired, so that the total circuit insertion loss is more than 5dB. That reduction in performance for the insertion loss was accepted as a part of a tradeoff with return loss.

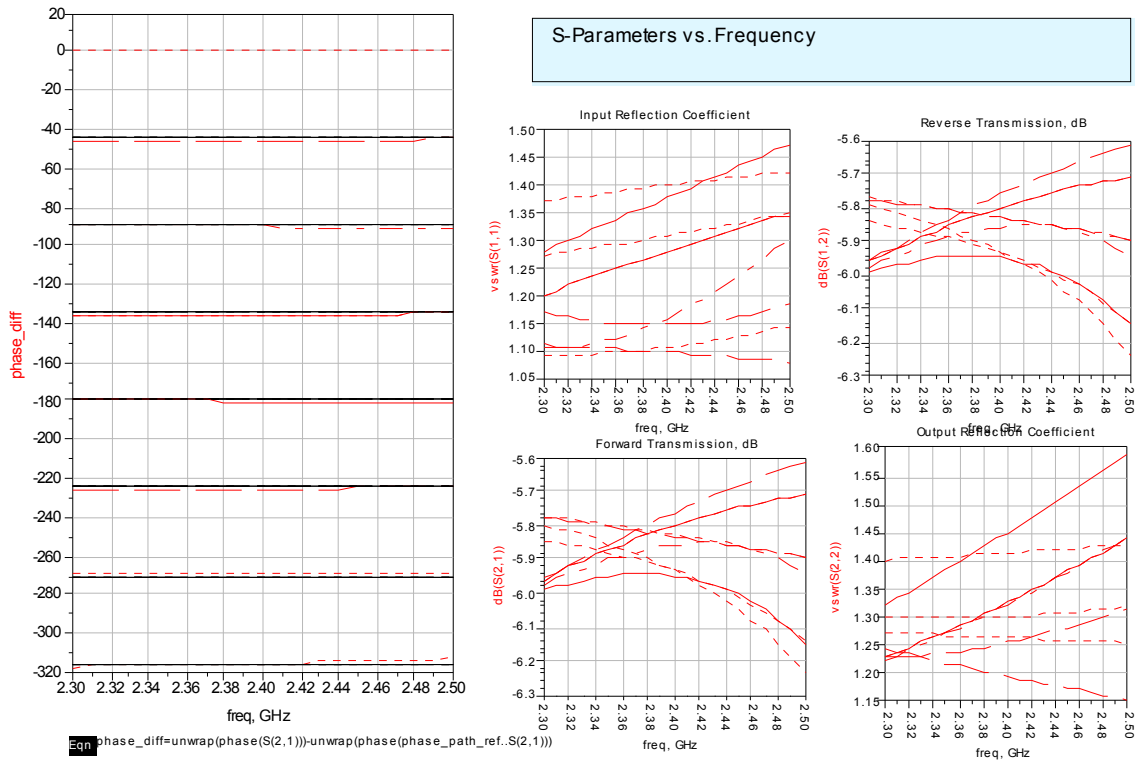
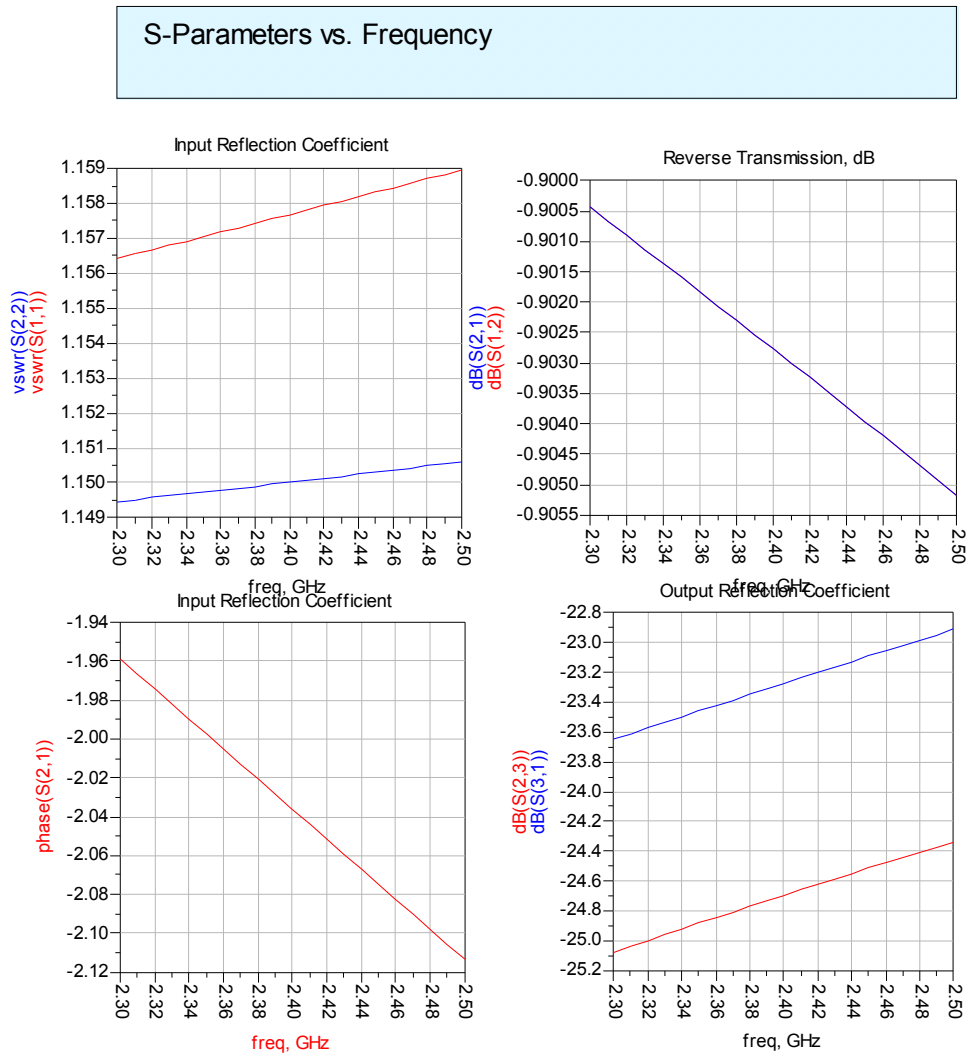


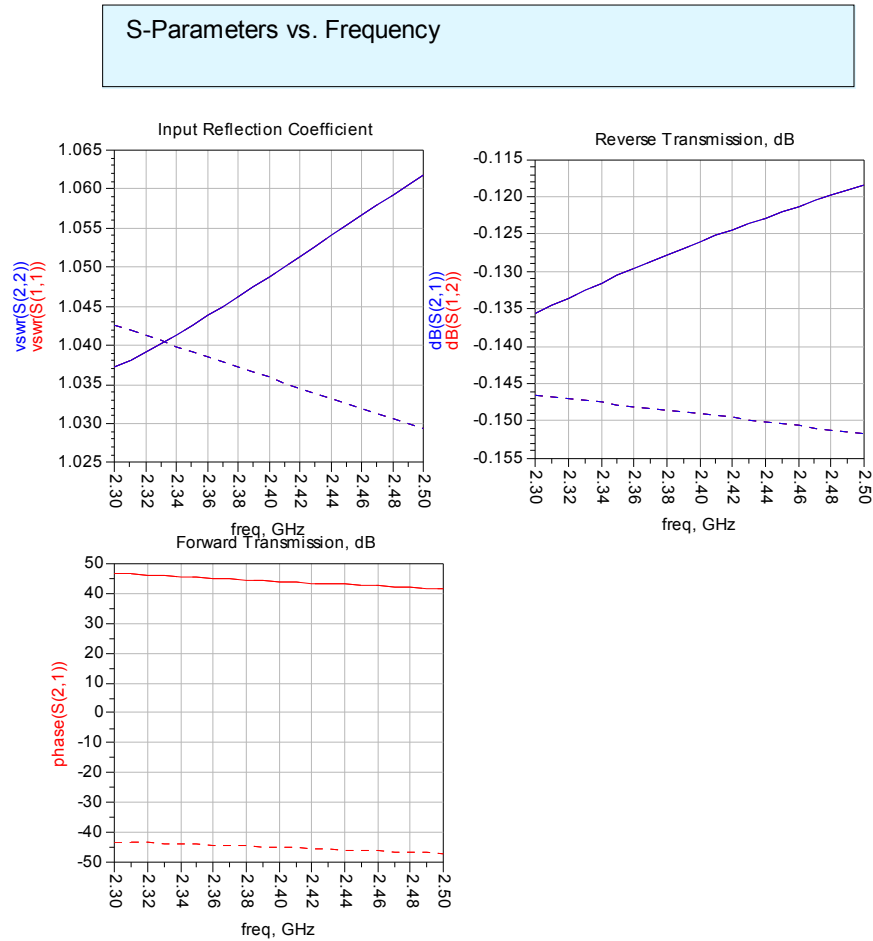
Figure 4. Phase shifter S-parameter and phase shift simulation results

Figure 5 shows simulated results for the switch used in the design project. It shows that for the active switch path, the switch gives both input and output VSWR's of better than 1.16:1. Switch loss is a little better than 1dB, and since there are 6 switches in the design, two for each of the three shift bits, there will be almost 6dB of loss just from the switches alone. As ensuing simulations will show, the switch loss is the major and primary contributor to the total circuit insertion loss. All phase shift circuits have but a fraction of a dB of insertion loss.



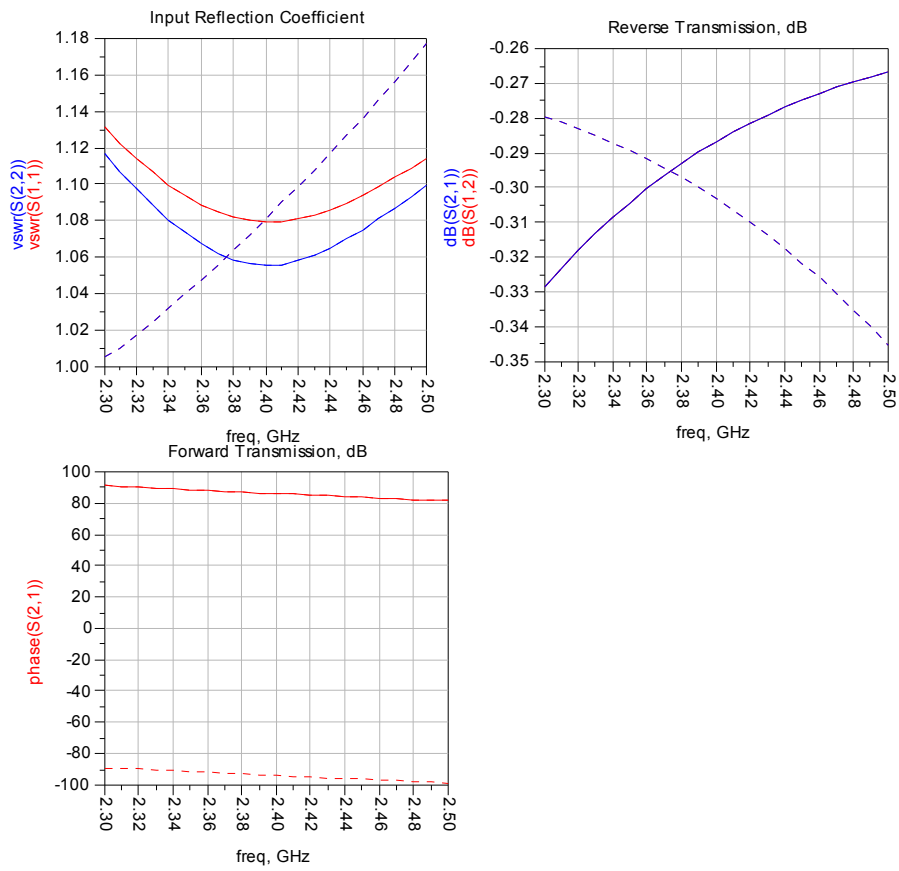
**Figure 5. Switch simulation results**

Figures 6 through 8 show simulated results for reference and delay circuits of the 90°, 180°, and 45° phase shift bits. The dotted lines represent the traces for the reference circuits. Notice that all VSWR plots are better than 1.2:1, and all insertion losses are but a fraction of a dB. The VSWR worsens once all shifter bits are combined.



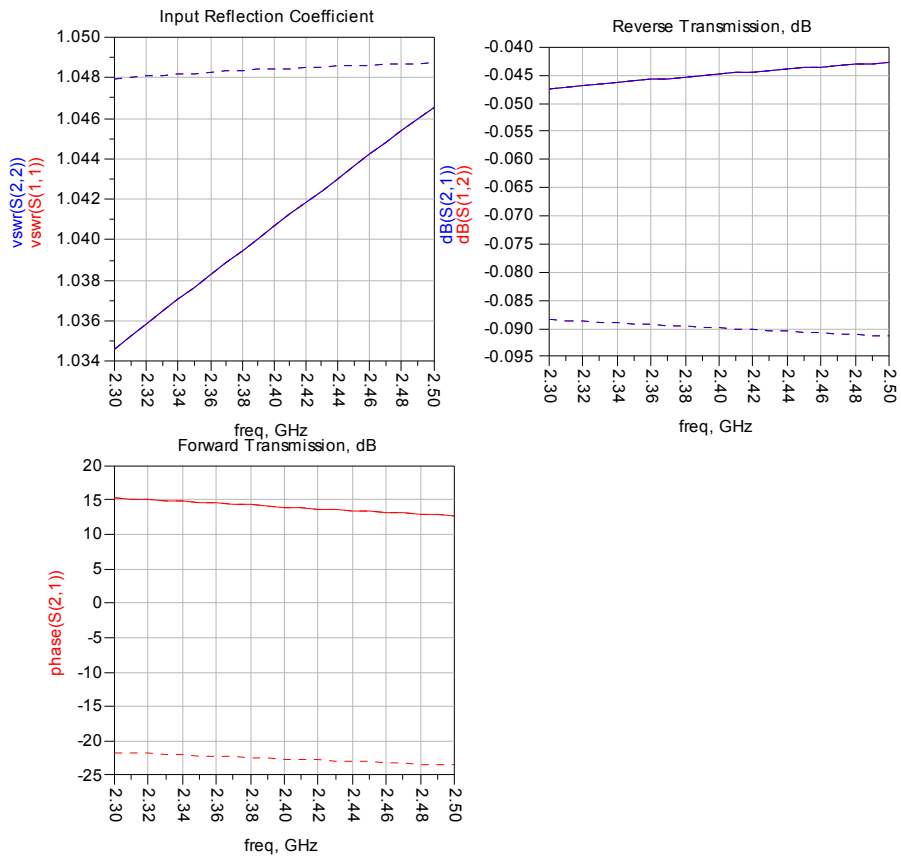
**Figure 6. Reference and delay simulation results for 90° phase shift**

# S-Parameters vs. Frequency



**Figure 7. Reference and delay simulation results for 180° phase shift**

## S-Parameters vs. Frequency



**Figure 8. Reference and delay simulation results for 45° phase shift**



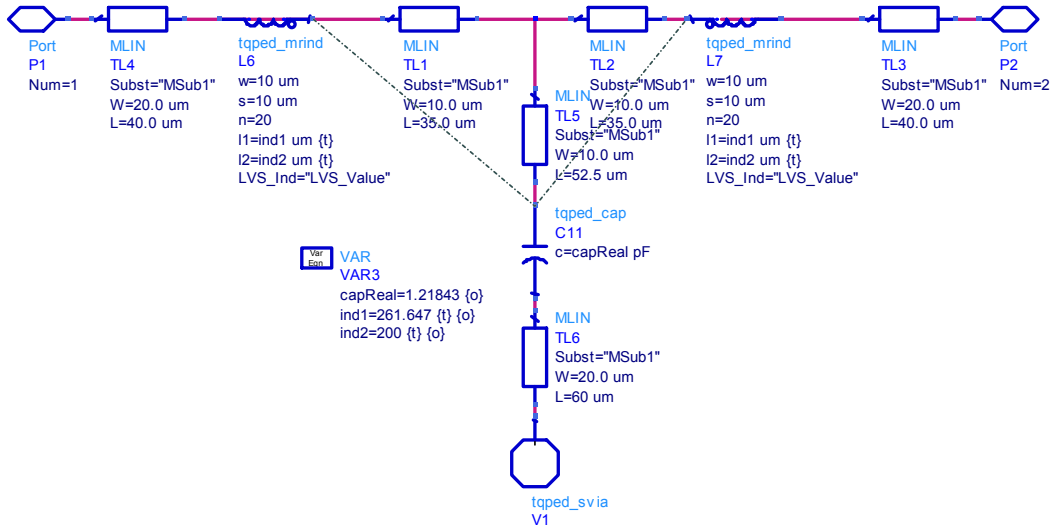


Figure 11.  $-90^\circ$  phase shift

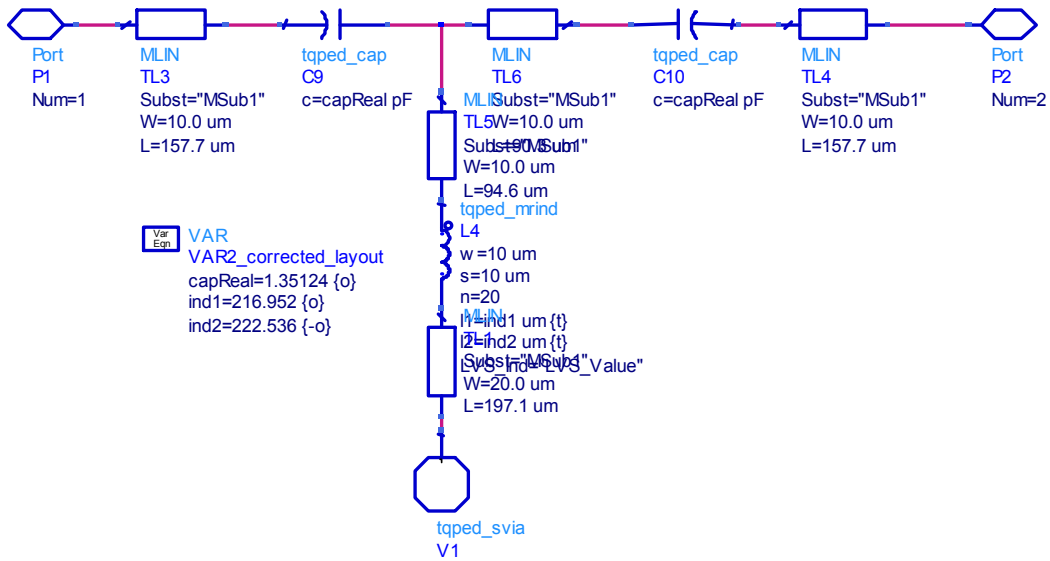
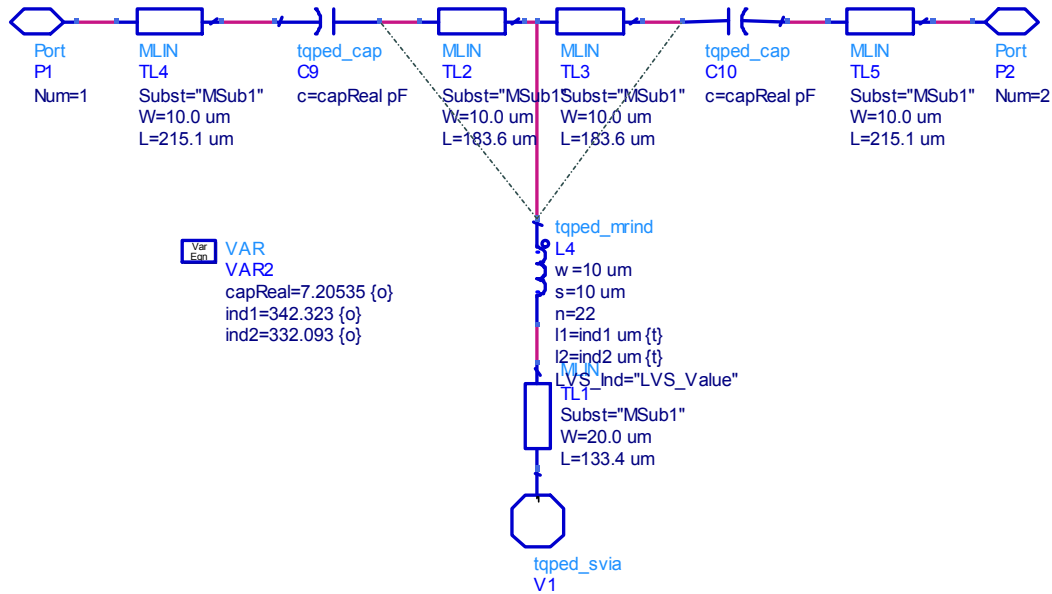


Figure 12.  $+90^\circ$  phase shift



**Figure 13. +20° phase shift**

### Layout Plot

Figure 14 shows the final layout for the phase shifter on a 60 mil by 60 mil GaAs substrate. Notice that there are three white boxes outlining the perimeter of the chip, the inner most box signifies the boundary for all vias. The second innermost box represents the boundary for all other circuit components. You'll notice that there is an empty margin on the left and bottom of the chip where components are allowed. The reason for that is that I had previously been under the impression that the circuit boundary was smaller than it actually was.

The RF input and output GSG (ground-signal-ground) pads are on the top left corner and right side of the chip, respectively. The GSG pads have a pitch of 150um. There are three more pairs of pads for the control lines. Each pair has a pad labeled "R" for reference, and "D" for delay, depending on which path is desired to be switched on or off. In-between each pad pair is also the label for the phase shift (i.e. 45, 90, or 180). Care was taken to compact the design, as well as to make everything symmetrical wherever possible. Additional vias were added whenever the addition could help avoid too many lines from crossing each other during routing, and at the same time they were kept to a minimum to conserve space.

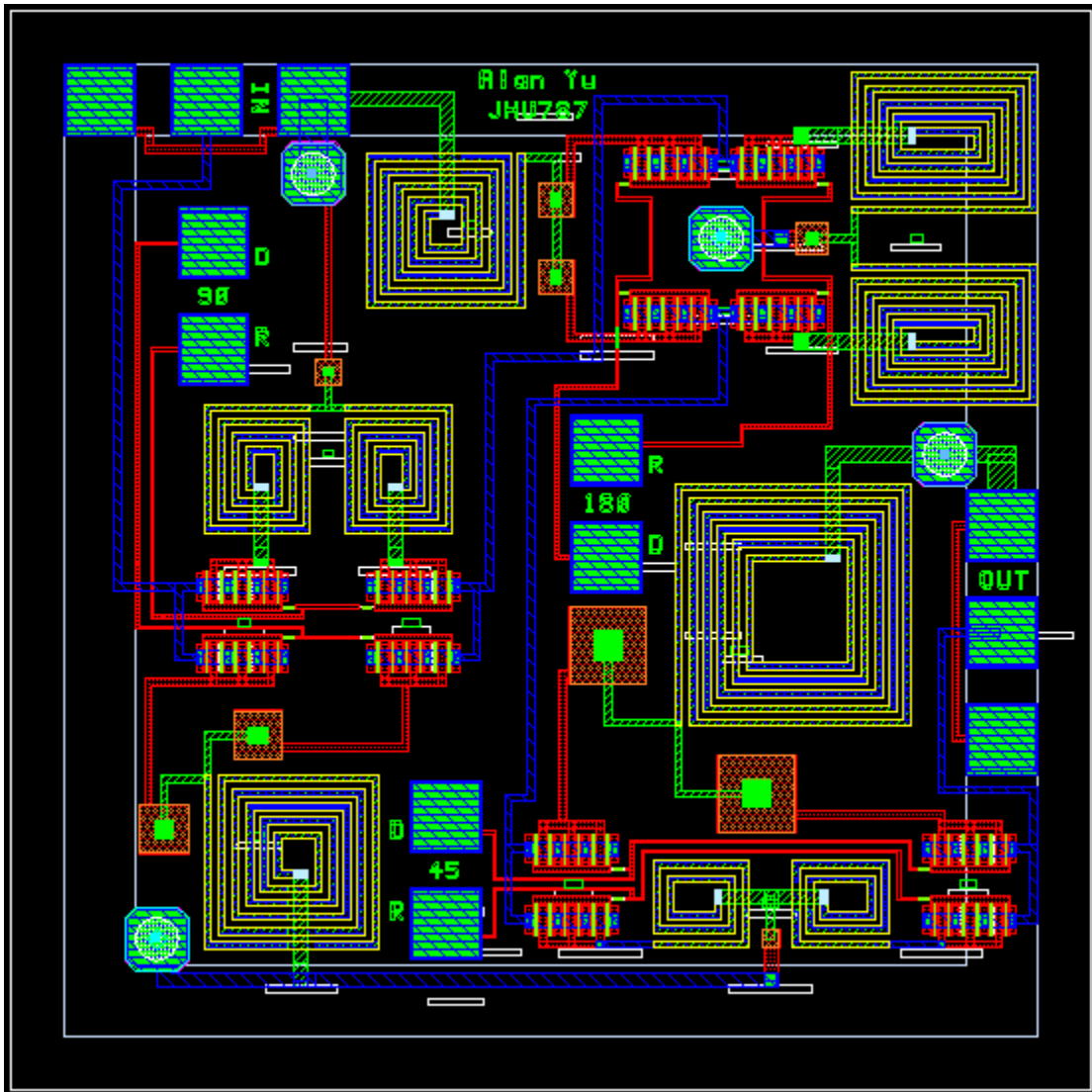


Figure 14. Phase shifter final layout

## Test Plan

A network analyzer, probing station with two 150um pitch GSG probes, three single probes, as well as a power supply capable of providing -2V control voltages are needed to test the phase shifter.

### Steps

- Connect a -2V supply to all three pads on chip labeled D (for delay). The other three reference pads should automatically float to 0V during measurement.
- Connect a 150um pitch GSG probe from the network analyzer to the RF input pads labeled “IN.”
- Connect a 150um pitch GSG probe from the network analyzer to the RF output pads labeled “OUT.”
- Measure the S-parameters of the RF ports using the network analyzer from 2.3 to 2.5 GHz in 10MHz steps.
- Save results to disk.
- Disconnect the -2V supply from the pad labeled D on the 45° bit, and place it instead on the pad labeled R on the 45° bit. The pad D should now automatically float to 0V during measurement.
- Measure and save as done previously
- Repeat this procedure for measuring and saving data until the -2V supply has been supplied to the control pads in all combinations as listed according to Table 2 below. Measure using the network analyzer and save all results to disk.
- When done measuring, disconnect, return, and turn off all equipment.
- Finally compare measure results verses simulation to assess accuracy of model.

Shift	45° bit		90° bit		180° bit	
	R	D	R	D	R	D
0°		-2V		-2V		-2V
45°	-2V			-2V		-2V
90°		-2V	-2V			-2V
135°	-2V		-2V			-2V
180°		-2V		-2V	-2V	
225°	-2V			-2V	-2V	
270°		-2V	-2V		-2V	
315°	-2V		-2V		-2V	

**Table 2. Combinations for -2V connections for testing all phase shift levels**

## Summary & Conclusions

In Summary, a three bit phase shifter was successfully designed for the S frequency band from 2.305 to 2.497 GHz. Phase shift accuracy exceeded specification requirements and had less than  $\pm 3^\circ$  of variation in-band. Input and output VSWR achieved spec of under 1.5:1 for all but one out of 8 phase shift levels, which was the  $180^\circ$  phase shift that had close to a VSWR of 1.6:1 up towards 2.497 GHz. All three bits of the design were compacted into a 60 x 60 mil GaAs chip. The higher loss in the switches used in the design, however, caused the insertion loss of the total design to exceed the spec of 5dB. The insertion loss ended up getting as high as close to 6.3dB at certain phase shift levels towards 2.497GHz. Also, the choice for using 3 pairs of control lines for the shift bits requiring 0V and -2V permits testing to be done on the fabricated design, but does not meet the goal of TTL compatibility.

With additional time, some enhancement opportunities include the following,

- Look into creating a DC converter circuit that converts 5V to -2V.
- Look into designing an inverter between 0V and -2V or 0V and 5V to be used in conjunction with the converter circuit so that only three control bits are necessary externally for controlling the phase shift levels.
- Since a transmission line is modeled as a sequence of series inductors and parallel capacitors, a version can be created with larger real estate and more components to achieve a wider bandwidth design
- Look into the possibility of using different transistors and switch topologies to reduce the switch loss while keeping the VSWR performance the same or better.
- Look at measured transistor performance to better predict circuit behavior.
- Do a measure versus model fit of the fabricated chip