



**EE 525.787 – Monolithic Microwave Integrated Circuit (MMIC) Design
Engineering and Applied Science Programs for Professionals**

Instructor: John Penn

**Design of a C-Band
Low Noise Amplifier (LNA) GaAs
Monolithic Microwave Integrated
Circuit (MMIC)**

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Abstract

LNA's are usually used as the front end of a receiver system. The purpose of an LNA is to amplify the weak signals that are received. It is usually located at the focal point on the antenna, so it can receive and amplify the weak signals so they can overcome the system losses of the receiver. The LNA must have the lowest noise, so it doesn't add noise to the microwave system. The purpose of this design is to design, simulate, layout, and test a two-stage GaAs MMIC LNA, which will operate in the C-band. We will use a GaAs substrate as part of the TriQuint Semiconductor's TQPED process for the MMIC fabrication.

Introduction

This LNA was designed to operate on low DC power. One of the primary objectives of this project was that the MMIC was intended to operate on battery power—typically 3.0 to 3.6 V, and to operate in the HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequency range (from 5150 to 5875 MHz). A DC battery power of +3.3 volts was chosen for VDS, and a frequency of 5500 MHz was chosen because it is in the middle of the C-band range. This LNA design consists of two similar stages with a matching network to separate the two stages. The LNA receives a 5.5 MHz input signal and passes it through the IMN to the gate of the 50 um E-mode FET. Each E-mode FET has a smaller 24 um D-mode FET on the Drain to supply current to the FET. The E-mode FETs are biased using a voltage divider network on the gate. The output of the first stage is sent to an intermediate matching network. This intermediate matching network acts as an OMN of the first stage and the IMN for the second stage. The signal is then amplified again with the second stage and passed through the OMN as RF OUT. The entire LNA was designed (schematic, simulation, and layout) using Agilent's Advanced Design Suite (ADS). The final schematic used all TriQuint components. The MMIC will be fabricated using the TriQuint TQPED Process (with vias) on a 4 mil (100 micron) thick wafer and will fit on a 60 x 60 mil ANACHIP die.

Design Approach

The initial decision that had to be made was to determine the battery power required and the size of the FETs to meet the DC power requirements of the project. Next, the Noise Figure circles and the Gain circles were plotted on the Smith chart. A tradeoff between minimum NF and maximum gain was determined. Since this design is a two-stage low noise amplifier, the NF of the first stage essentially determines the overall NF; therefore, the NF of the first stage needed to be as low as possible. The stability of the FET had to be checked. It was determined to add a stabilizing resistor to the output, to avoid amplifying additional noise. From here, the IMN could be designed. Finally, S_{22}^* of the first stage could be determined and matched to S_{11} of the second stage. Up to this point, all of the components have been ideal components. The next phase is to incorporate the TriQuint capacitors, resistors and inductors and compare the simulation results with the ideal components; retune the design if necessary. Create the layout, and then add the MLIN to compensate for the line lengths of the traces.

Specifications vs Goals

The goal of the C-band Low Noise Amplifier is to use small PMode PHEMTs (<50 microns) to achieve at least 20dB of gain, with a maximum NF of 3 dB and a goal of a 2dB NF. Ideally, it should consume no more than 5 mW per stage; however, it can have a specification of 10 mW per stage. Since the DC power criteria of this LNA is very low power, each FET should be biased at $I_{DSS}/4$ and 1.0 to 2V V_{DS} to achieve some gain.

The goals of this Low Noise Amplifier are as follows:

Parameter	Specification	Goal
FREQUENCY RANGE	5512.5 MHz	5150 to 5875 MHz
BANDWIDTH (S21)	1GHz	> 800 MHz
GAIN	24.25 dB	> 20 dB
DC POWER CONSUMPTION	35 mW	10 mW/stage; 5 mW/stage, goal
NOISE FIGURE	2.692 dB	< 3 dB; 2 dB, goal
INPUT IP3	-5dBm	> 0 dBm
VSWR, 50 Ohm		< 1.5:1
SUPPLY VOLTAGE	+3.3 Volts	+ 3.3 Volts only, goal (3 to 3.6V range)
SIZE	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP

Tradeoffs

Because this is a battery powered LNA, the size of the FET must be appropriate for the DC power requirement. Since this is a LNA, there is the fundamental tradeoff between minimum Noise Figure with the most gain. FET stability must also be considered while performing the tradeoff between minimum NF and maximum gain. The FET should be stable across the operating band, to avoid oscillations within the operating band.

Simulations

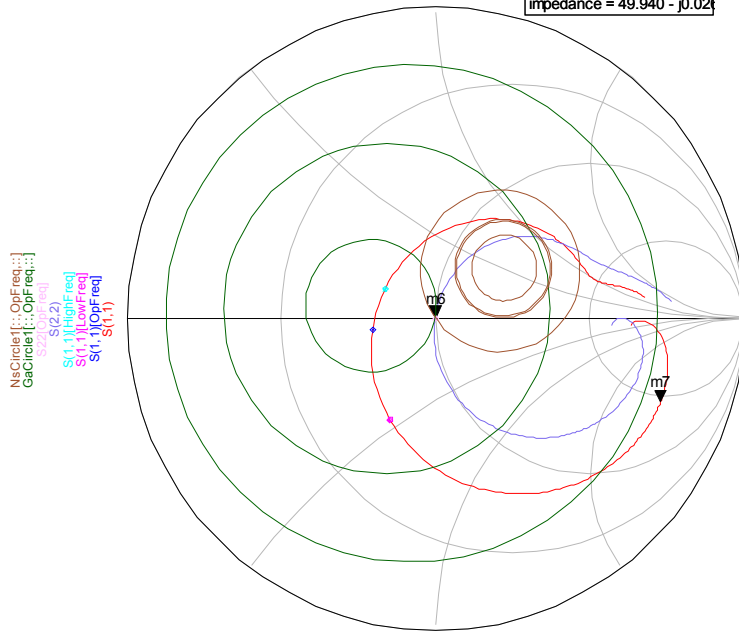
Linear Simulation

index	V/s	...ource.SP_DCOP.Power
1	3.300	-0.038

Entire LNA Power Consumption

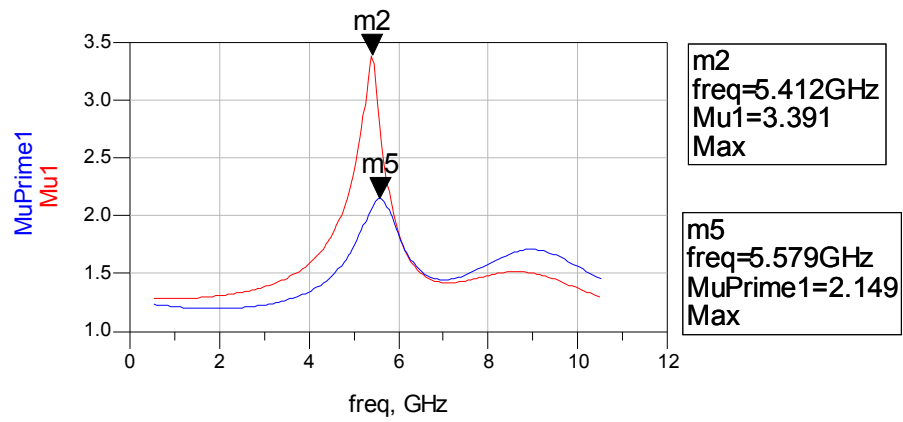
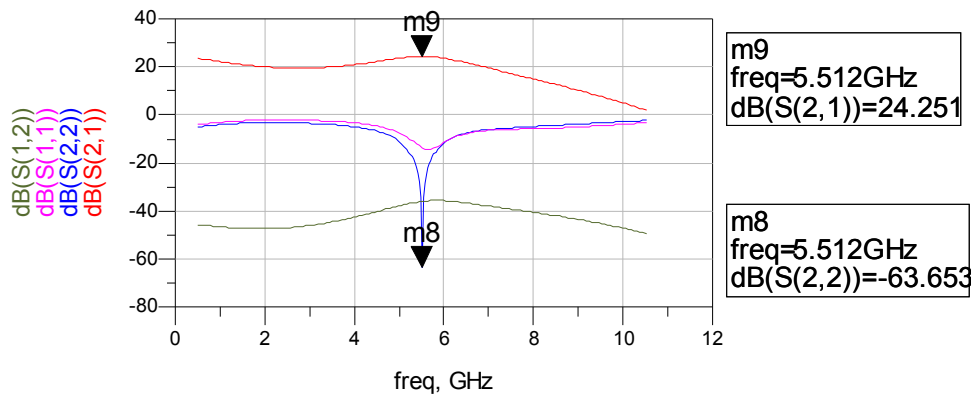
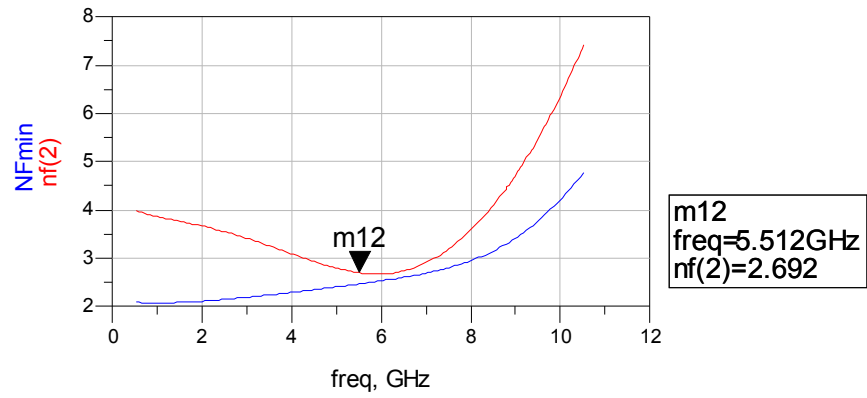
Zin1[OpFreq]	Zin1[LowFreq]	Zin1[HighFreq]	S(2,1)[OpFreq]	S(1,1)[OpFreq]	S(2,2)[OpFreq]
33.003 - j2.703	38.316 / -36.742	36.053 / 10.753	24.251 / 80.846	-13.671 / -169.099	-63.653 / -156.189
NFmin[OpFreq]	nf (2)[OpFreq]				
2.464	2.692				

m6
freq=5.512GHz
S(2,2)=6.567E-4 / -156.189
impedance = 49.940 - j0.02



freq (512.5MHz to 10.51GHz)
(0.000 to 0.000)
cir_pts (0.000 to 51.000)

m7
freq=2.41250GHz
S(1,1)=0.77874 / -20.20443
impedance = 135.905 - j185.75

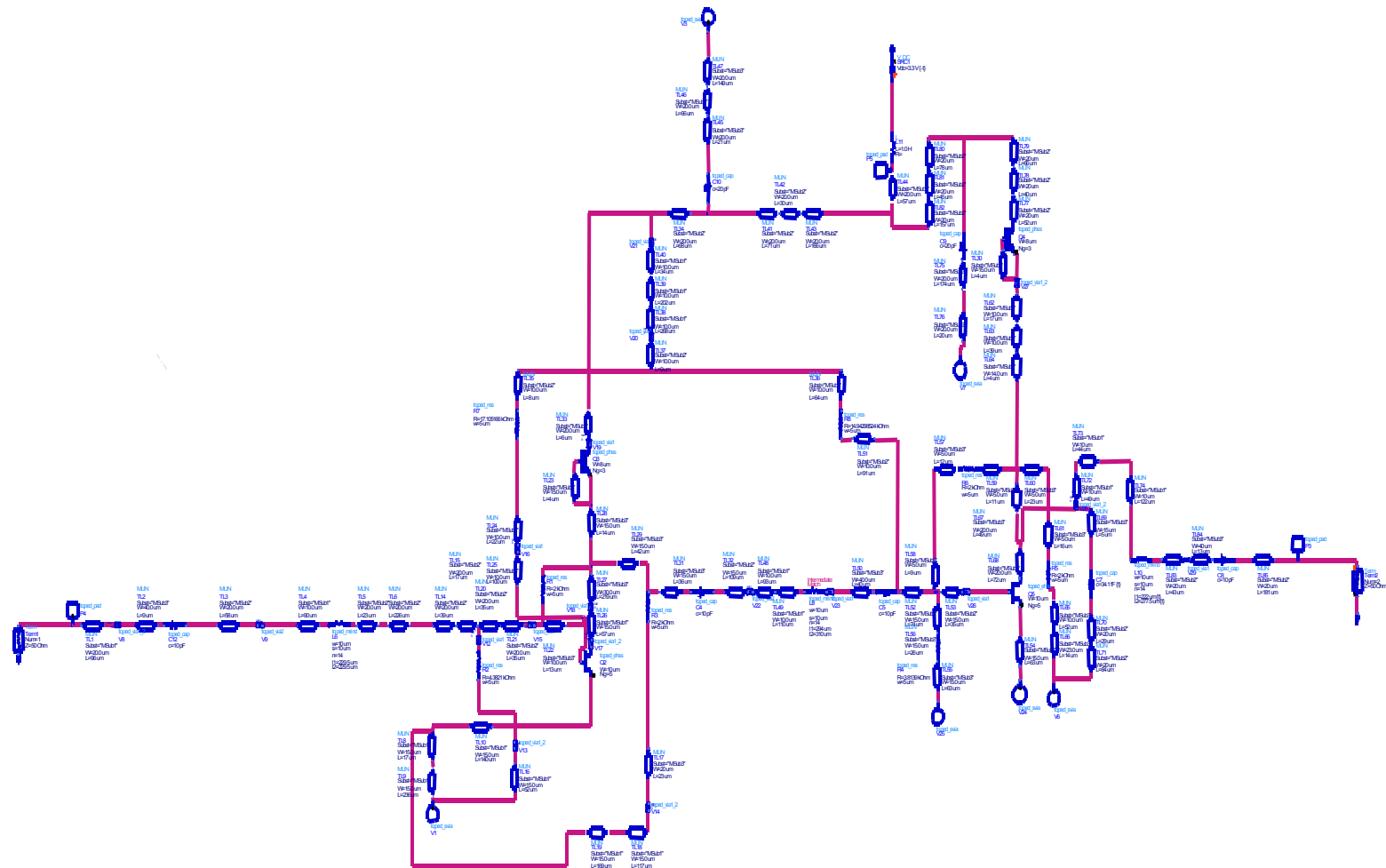


Non-Linear Simulation IP3



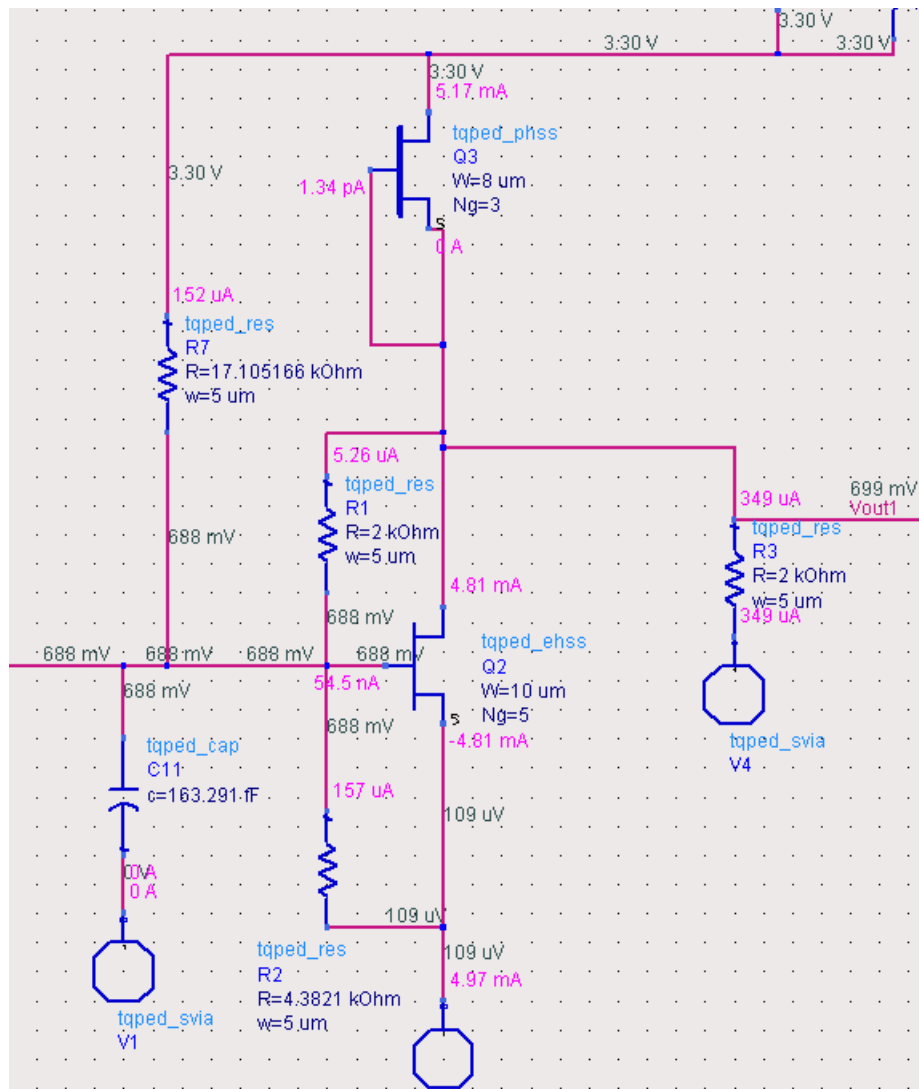
IP3 (TOI) I/O levels: Input power level = -5dBm & Output power level = ~25dBm.

RF (w/MLIN)



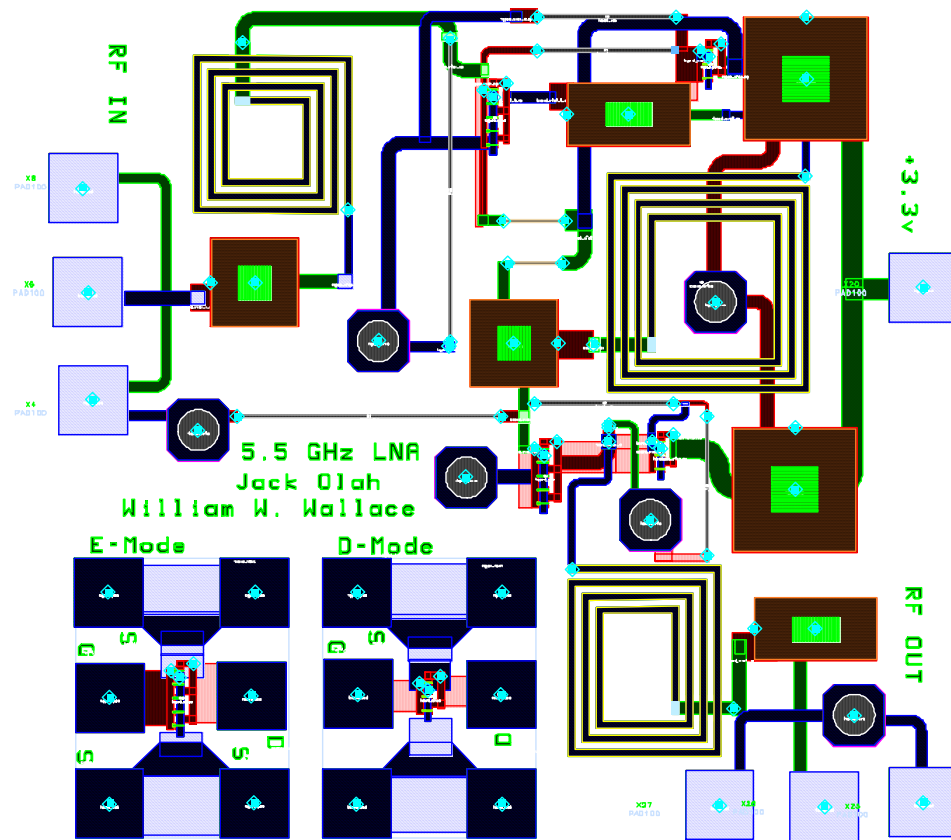
DC Annotation

Note: Only one stage is shown because the FETs are essentially identical for each stage.

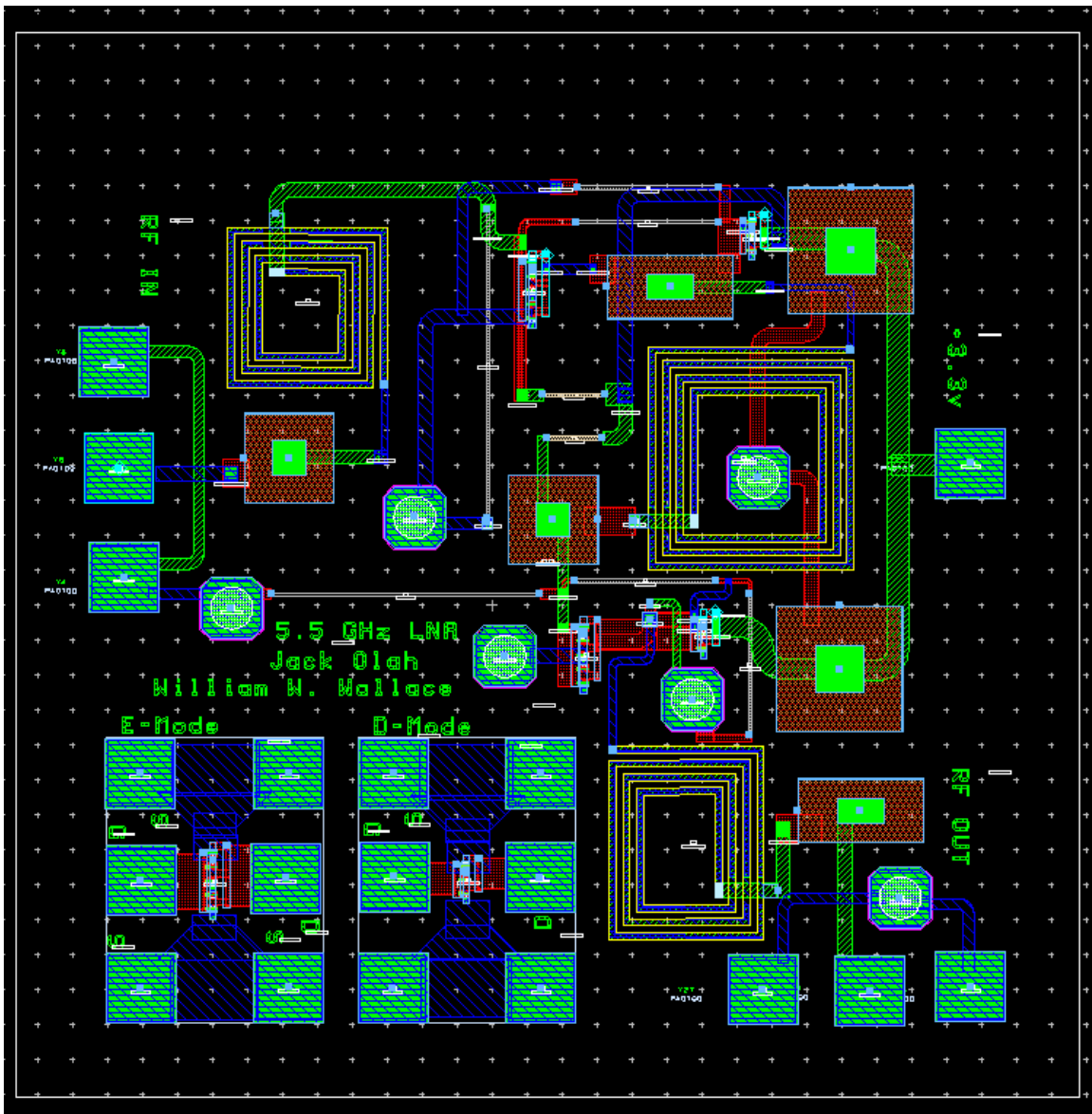


Layout

Plot of layout



Screen shot of layout



Test Plan

Since the MMICs will not be available for a few months after the class has ended, the testing phase of the project cannot begin until that time. The C-band LNA will be tested using an Agilent 8510 (45 MHz to 26 GHz) Vector Network Analyzer (VNA), a Cascade Model 43 wafer probe station with up to 4 RF probes (GSG), 4 DC needle probes, synthesized signal generators (26 GHz), a Noise Figure meter, and an 18 GHz Spectrum

analyzer. This test plan should be used as a guide for testing, not as an official test procedure.

Turn On Procedure

To protect the design from excessive current draw due to possible layout errors or defects, set the current limit of the supply to twice the nominal current pull. Increase the drain voltage of the DC supply slowly up to the required +3.3V (VDS) operating voltage. Record the current draw off the power supply

RF Measurements

S-Parameter Measurements

The VNA must be calibrated prior to making any measurements; however, the VNA in the lab as probably been calibrated at the beginning of the lab. After calibrating the VNA, connect the RF and DC probes up to the LNA. Make the measurements of S11, S21, S12, and S22.

Noise Figure Measurements

Once again, calibrate the noise figure test set. Connect the input probe to the RF IN pad. Connect the output probe to the RF OUT pad. Measure the noise figure of the LNA and store the measurement data.

IP3 Measurements

Set the test bench for two tones. Start with the power levels set to a low level, i.e. -30 to -20dBm. Using a spectrum analyzer, increase the power levels of the two tones and look for the third order products. Record the delta between the third order products and the fundament tones – these are the third order intercept (TOI) values.

Summary & Conclusions

Overall, the design meets the key requirements proposed in the project objectives. The gain and NF are relatively constant across the specified operating band. The LNA simulation yielded a gain (S21) of 24dB, an S22 of -63dB, an S11 > -10dB and a NF of 2.7dB at the center frequency. It uses about 35mW of power from the 3.3V source for the entire design. Unfortunately, this LNA consumes 15mW more power than the specification of 20mW (10mW/stage, two stages).

This report described the design, simulation and layout of a two-stage GaAs MMIC low noise amplifier, operating at C-band from 5.150 to 5.875 GHz as the initial amplification section of a wireless communications (WCS) transceiver system. The low noise amplifier design was a class project for Johns Hopkins University's MMIC Design Course (525.787), Fall 2007. The GaAs process used was TriQuint Semiconductor's TQPED process on a 4 mil (100 micron) GaAs substrate.