1.0) ABSTRACT

A vector modulator was developed for use within the Wireless Local Area Network (WLAN) frequency band. The amplitude and phase of the I (in-phase) and Q (quadrature) components are set via reflective attenuators, thus creating a flexible architecture that can generate quadrature phase shift keying (QPSK) while still supporting binary phase shift keying (BPSK). Optimal performance occurs at 5500 GHz, but with a -15 dB input impedance bandwidth from 5150 to 5875 MHz the modulator can operate over all frequencies in the WLAN band. Utilization of TriQuint's 0.5 um PHEMT GaAs process enabled the design to fit onto a 120 X 60 mil GaAs chip.

2.0) INTRODUCTION

A vector modulator allows the transmission of data across a wireless medium. The advantage of utilizing QPSK over BPSK is that for a given symbol rate within a system, the effective bit rate doubles since two bits can be sent simultaneously on the I and Q channels. This results in the bandwidth of the modulated signal being reduced by a factor of two.

A QPSK modulated waveform takes on one of four phase states; +45º, +135º, -135º, and 45º. The modulated signal that creates these phase states can be represented by the following equation:

$$S(t) = A_I \cos(wt) + A_Q \sin(wt)$$

The relative amplitudes of the I component (A_I) and Q component (A_Q) determine the phase state of the modulated signal based off the use of the trigonometric identity: $a\cos(wt) + b\sin(wt) = C\cos(wt + \theta)$. The values of A_I and A_Q required to create a QPSK waveform are as follows:

θ	A_I	A_Q
45	1	1
135	-1	1
-135	-1	-1
-45	1	-1

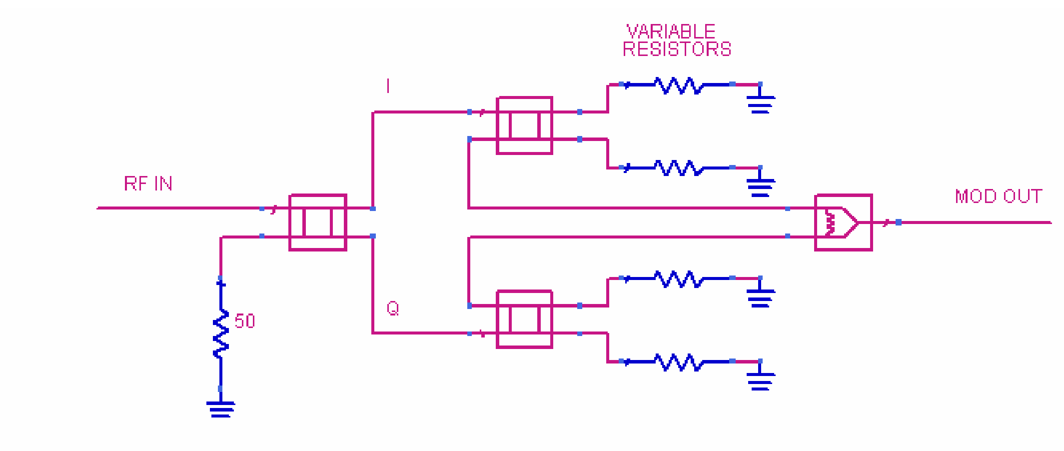
The vector modulator I designed inputs an RF tone with the generic form Acos(wt), and outputs a QPSK modulated waveform. This requires three sections within the modulator; a branch-line hybrid coupler to create the I and Q components, two reflective attenuators to vary A_I and A_Q, and a Wilkinson power divider to then combine the I and Q components. The adjustment of A_I and A_Q are controlled via the application of a unique DC voltage to each I and Q channel.

My vector modulator design also enables the transmission of BPSK data. A BPSK modulated waveform can also be represented by the same equation above, but the signal only takes on two phase states: 0º and 180º. Therefore A_Q is always set to 0 and the relative amplitude A_I of is toggled between +1 and 1.

The design, simulation, and layout of my design were all performed in Advanced Design System (ADS) using TriQuint components. Due to the operating frequency of my design (5150 – 5875 MHz), all sections of the modulator were built with lumped elements.

3.0) DESIGN APPROACH

A block diagram of my I-Q vector modulator is shown below:



The following sections will provide a detailed description of each segment of the modulator.

3.1) Branch-line Hybrid Design

The individual 50 and 35 Ω sections of the branch-line hybrid coupler were created with lumped elements using low-pass π networks designed for operation at 5500 MHz. For the 50 Ω sections, the ideal values for the inductor and capacitors were 1.45 nH and 0.58 pF respectively. For the 35 Ω sections, they were 1.02 nH and 0.82 pF.

Ideally, a branch-line hybrid will output two signals that are equal in power (-3 dB in relation to the input) and 90º out of phase. I therefore utilized a branch-line hybrid on the input of my design to establish the I and Q components.

The key characteristics of a branch-line hybrid are output signals having equal amplitude and 90º phase difference, and an input impedance of 50 Ω on all four ports. It is possible to design a 90º branch-line hybrid that has an input impedance of approximately 50 Ω across the WLAN frequency band, but it is possible only to have a 90º phase difference at one frequency. As a result, I chose to design my 90º branch-line hybrid such that the two outputs had a 90º phase difference at 5500 MHz.

When substituting TriQuint components for the ideal inductor and capacitor values calculated for the low-pass π networks, I was able to obtain results that closely mirrored an ideal 90º branch-line hybrid. In particular, the phase difference of the two output ports was 89.64º. Also, the loss of the I component was -3.59 dB as opposed to -3.62 dB for the Q component. The additional loss in relation to the -3 dB ideal case is due to the inherent loss in the TriQuint inductors. The input match to all four ports on my 90º branch-line hybrid design was better than -15 dB across the WLAN band.

3.2) Reflective Attenuator Design

A reflective attenuator is designed by taking a 90º branch-line hybrid and intentionally mismatching the through and coupled ports, thereby creating reflected power that can be captured on the isolated port. When an ideal 90º branch-line hybrid is loaded with 50 Ω terminations on its through and coupled ports, no power is delivered to the isolated port. The greater the mismatch on the through and coupled ports, the more power that will be delivered to the isolated port.

The goal of the reflective attenuators used in my design is to produce outputs that have relative amplitudes of either 0, +1, or -1. In other words the reflective attenuator will output signals that have a power level of either 0 Watts, or some other non-zero power level with 180º phase separation for the ± 1 case. As mentioned above, the 0 case occurs when the through and coupled ports are loaded with 50 Ω. The ± 1 cases can be obtained from many different resistance values, but the resistances must be paired up such that they create a reflection coefficient with equal magnitude and opposite phase based off the following equation:

$$\Gamma = \frac{R_{OUT} - 50}{R_{OUT} + 50}$$

The greater the magnitude of Γ, the more power that will be delivered to the isolated port. It is desirable that the reflective attenuator design supply as much power as possible to the isolated port as this translates into less insertion loss in the in the I-Q vector modulator as a whole. The maximum magnitude of Γ is 1, and this occurs when Rout is either a short or open circuit. A short would create a relative amplitude of -1, and the open +1.

For my reflective attenuator design, I am using the drain of a TriQuint 0.5 um PHEMT as the variable attenuator on the through and coupled ports. The drain of this PHEMT consists of a parallel RC circuit, where the resistance is adjustable via the voltage supplied to the gate. When the PHEMT is biased near its I_{DSS} level a very low resistance is provided. When the PHEMT is biased near pinch-off, a large resistance is presented. Even when the PHEMT is fully turned 'ON' however, a resistance of 0 Ω can not be obtained. The larger the physical size of the PHEMT, the lower the resistance value that can be achieved. On the contrary, a larger PHEMT also results in a greater parallel capacitance. This is undesirable because an ideal reflective attenuator requires a purely resistive load. In the 'ON' state, the effects of the parallel capacitance are negligible because the low resistance value dominates. In the 'OFF' state however the effects of this capacitance is much more pronounced. Therefore a compromise must be made in choosing a PHEMT size that provides adequate 'ON' resistance while keeping parallel capacitance at a minimum.

For my design a I chose a 200 um PHEMT, which provided an 'ON' resistance of 10 Ω. I was able to resonate out the parallel capacitance of this PHEMT by placing an ideal

8.45 nH inductor across its drain-to-source leads, but since this inductor would be physically large to implement via a TriQuint spiral inductor I chose not to include it in my final design as the effects of the parallel capacitance using a 200 um PHEMT was not too severe.

A reflective attenuator is required for both the I and Q channels to set the relative amplitudes of A_I and A_Q. To set the value of either A_I or A_Q to +1, the PHEMT devices on both the through and coupled ports of the branch-line hybrid are biased in the 'ON' state thus setting the load on these ports to 10 Ω. Conversely, to set the value of A_I or A_Q to -1 the PHEMT devices are biased in the 'OFF' state thus setting the load on these ports to 250 Ω. To set the value of A_Q to 0 for BPSK modulation, the PHEMT devices are biased to present 50 Ω to the ports. The following gate voltages are used to bias the 200 um PHEMT devices in the reflective attenuator:

Vgs (V)	R (Ω)
-0.66	250
-0.52	50
0.05	10

3.3) Wilkinson Power Divider Design

The 70 Ω sections of the Wilkinson power divider were created with lumped elements using low-pass π networks designed for operation at 5500 MHz. The ideal values for the inductor and capacitors were therefore 2.05 nH and 0.41 pF respectively.

Ideally, when used as a splitter a Wilkinson power divider will output two signals that are equal in power (-3 dB in relation to the input) and phase. When used as a combiner, it will equally sum two inputs that are 90º out of phase. I therefore utilized a Wilkinson power divider on the output of my design to sum the I and Q components.

For simplicity I chose to analyze my Wilkinson power divider as a splitter, recognizing that if I designed it correctly in this regard its use as a combiner would be transparent. The key characteristics of a Wilkinson power divider used as a splitter then are output signals the have equal amplitude and phase, and an input impedance of 50 Ω on all three ports. I designed my Wilkinson power divider to meet all of these specifications across the WLAN band. Additionally, my design was based off the two outputs having an absolute phase lag of 90º at 5500 MHz.

When substituting TriQuint components for the ideal inductor and capacitor values calculated for the low-pass π networks, I was able to obtain results that closely mirrored an ideal Wilkinson power divider. In particular, the phase and amplitude differences between the two output ports was indistinguishable, with the loss on both output ports measuring at -3.27 dB. The additional loss in relation to the -3 dB ideal case is again due to the inherent loss in the TriQuint inductors. The input match to all three ports on my Wilkinson power divider was also better than -15 dB.

3.4) Design Specifications

The following chart shows the specifications for my vector modulator design. As the attached plots in the Simulated Data section will show, all specifications were met except for input compression point when the phase state is set to -135º.

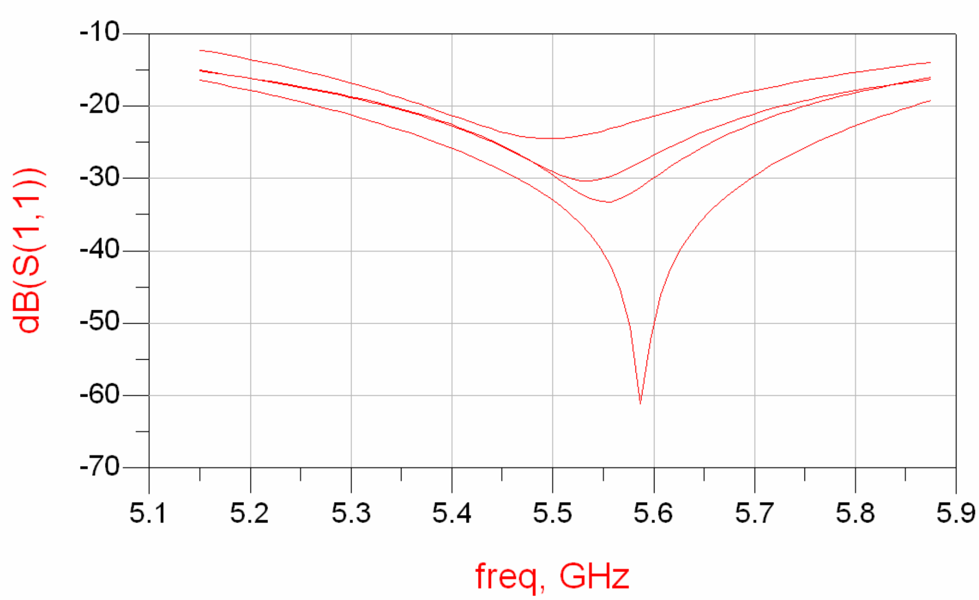
Specifications	MIN	TYP	MAX
RF Frequency Range (MHz)		5150 - 5875	
I/Q Frequency Range (MHz)		DC – 50	
I/Q to RF Isolation (dB)	10	16	
Conversion Loss (dB)		7	10
Input Compression Point (dBm)	0	7	
VSWR		1.5:1	2.5:1

4.0) Simulated Data

The following data is taken from simulations in ADS.

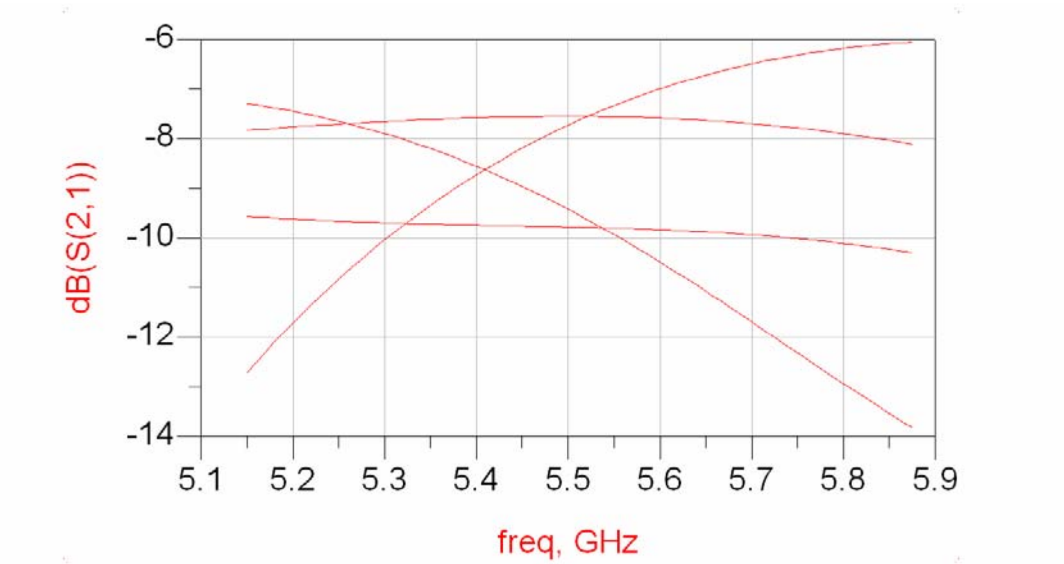
4.1) Input Match

The input matching plot is swept across the 5150 – 5850 frequency band, with one plot being taken for each of the four nominal phase states of a QPSK modulated waveform. The nominal phase states constitute the PHEMT's in the reflective attenuator being biased to either 10 or 250 Ω.



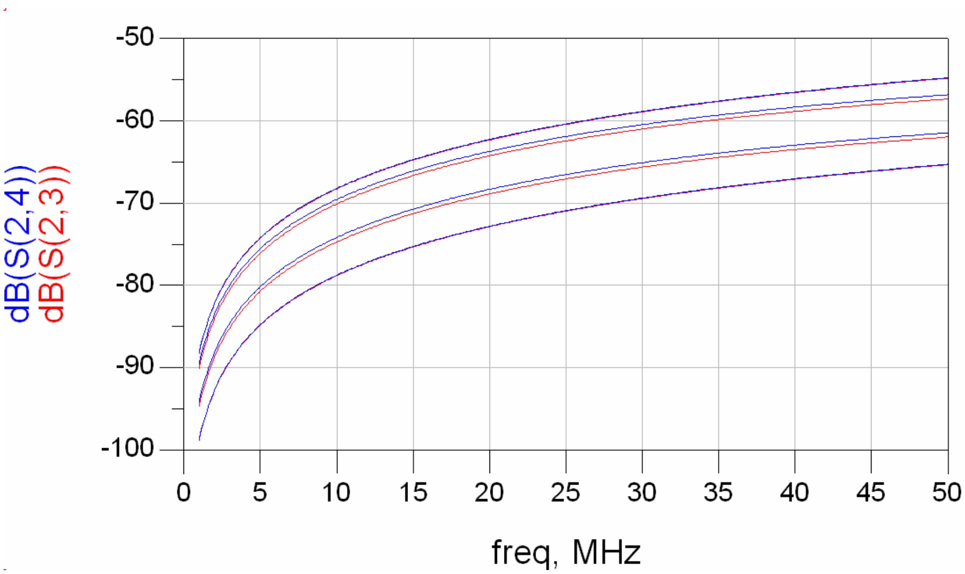
4.2) Gain

The gain plot is swept across the 5150 – 5850 frequency band, with one plot being taken for each of the four nominal phase states of a QPSK modulated waveform. As can be observed, the gain varies with each phase state as a result of the reflective attenuators not being ideal. In any case though, at the design center frequency of 5500 MHz insertion loss is less that 10 dB.



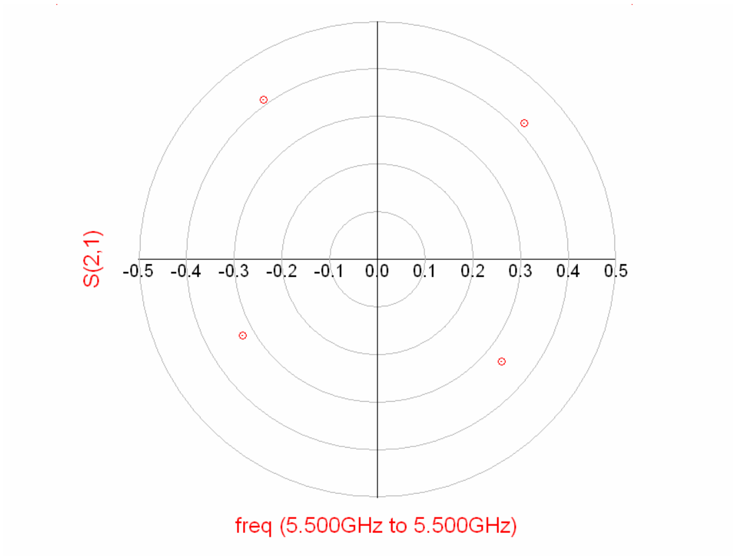
4.3) I/Q to RF Isolation

The isolation plot is swept across DC – 50 MHz with one plot being taken for each of the four nominal phase states of a QPSK modulated waveform.



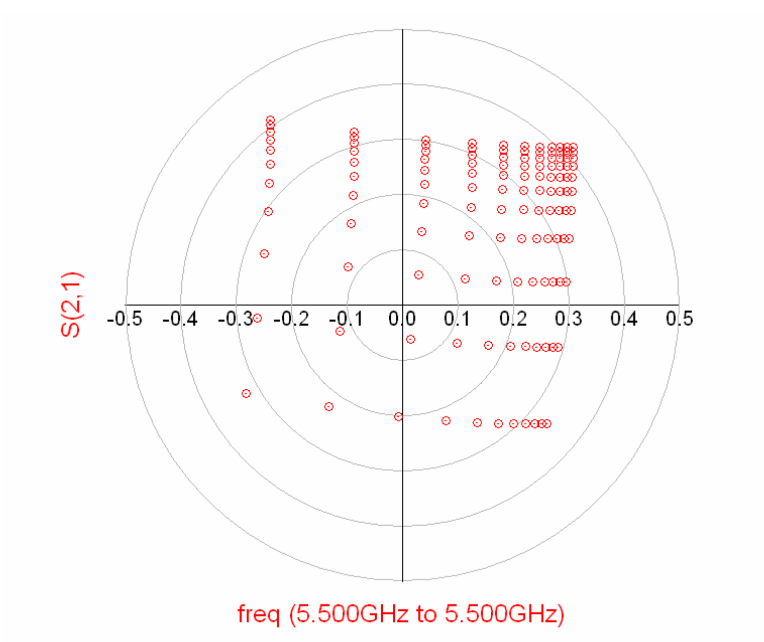
4.4) Constellation Diagram @ 5500 MHz

The following constellation diagram was taken with the load resistances set to 10 and 250 Ω on the reflective attenuators.



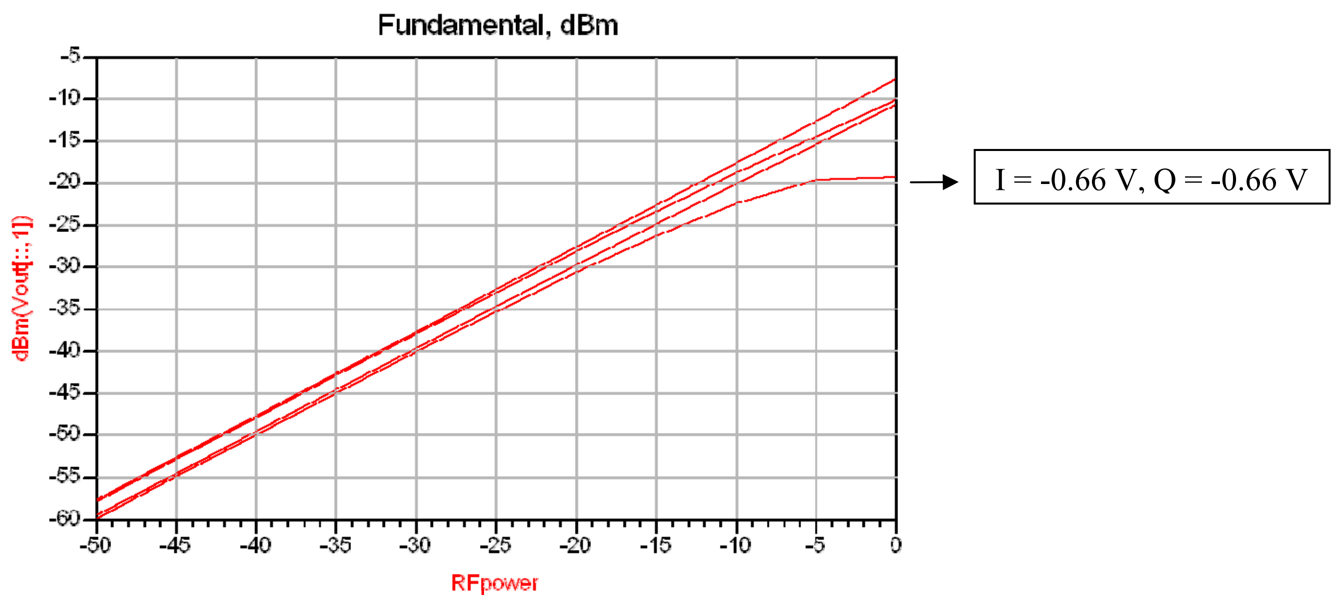
4.5) Constellation Diagram @ 5500 MHz Across Multiple Attenuator Settings

The following constellation diagram was taken with the load resistances set to multiple values in-between 10 and 250 Ω on the reflective attenuators. As can be observed, a square is formed by varying these resistance with any point inside the square being realizable.



4.6) Input Compression Point

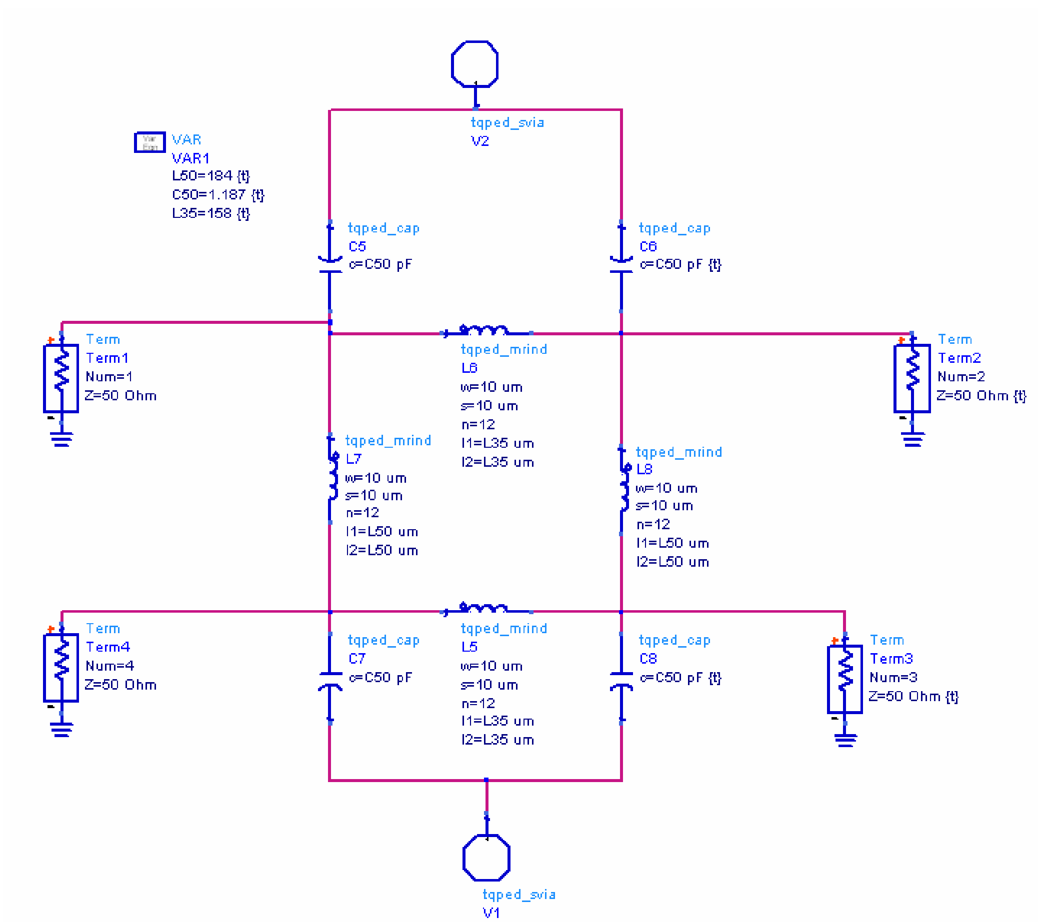
The following plot shows input vs. output power at 5500 MHz across all four nominal phase states of a QPSK modulated waveform. As can be observed, the input compresses rapidly when the phase state is set to -135º. At this phase state both the I and Q reflective attenuators are biased to 250 Ω meaning the PHEMT's are biased are near pinch-off.



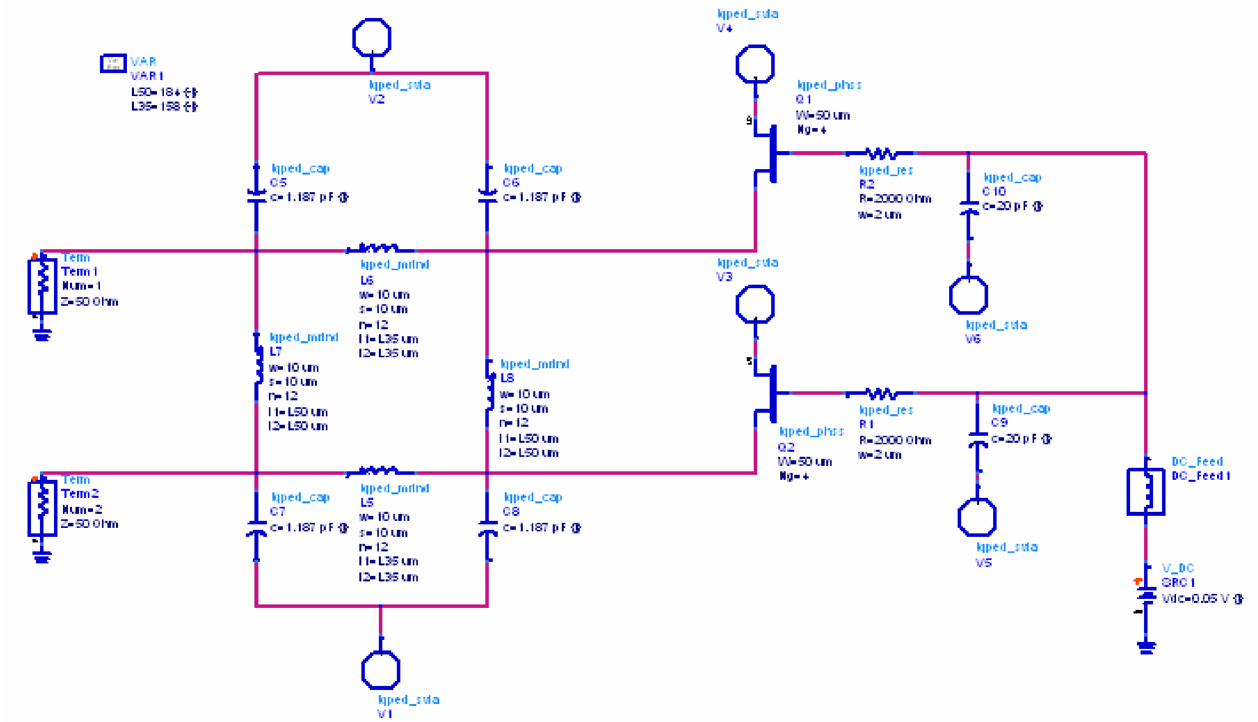
5.0) Schematic

The following sections show the three individual segments of my I-Q vector modulator design along with overall schematic.

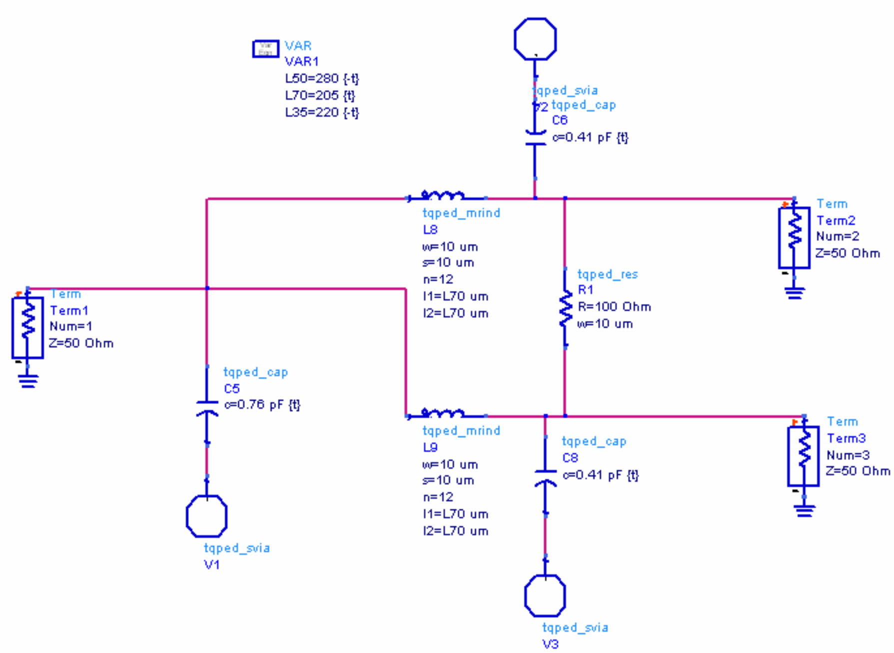
5.1) Branch-line Hybrid



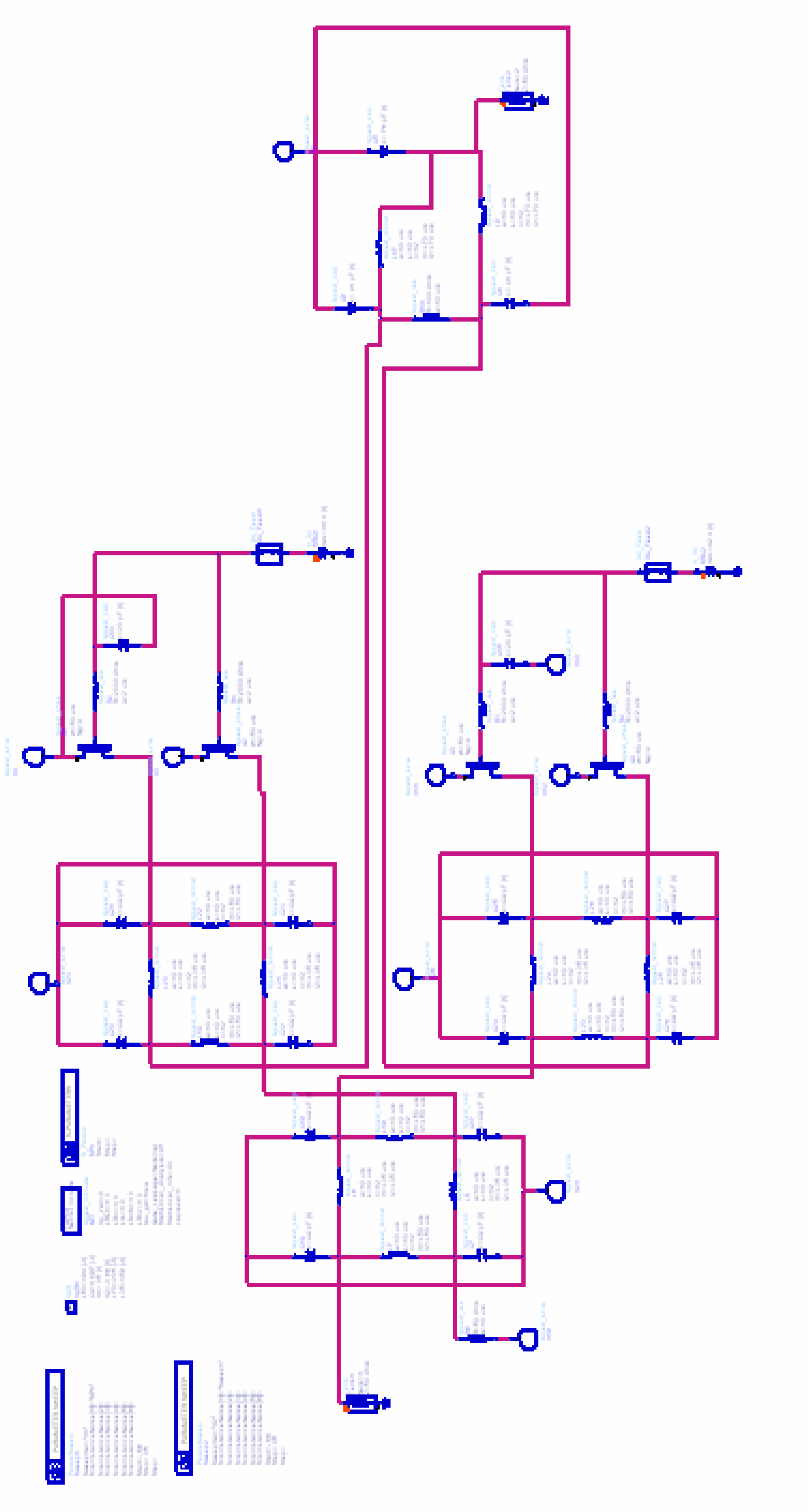
5.2) Reflective Attenuator



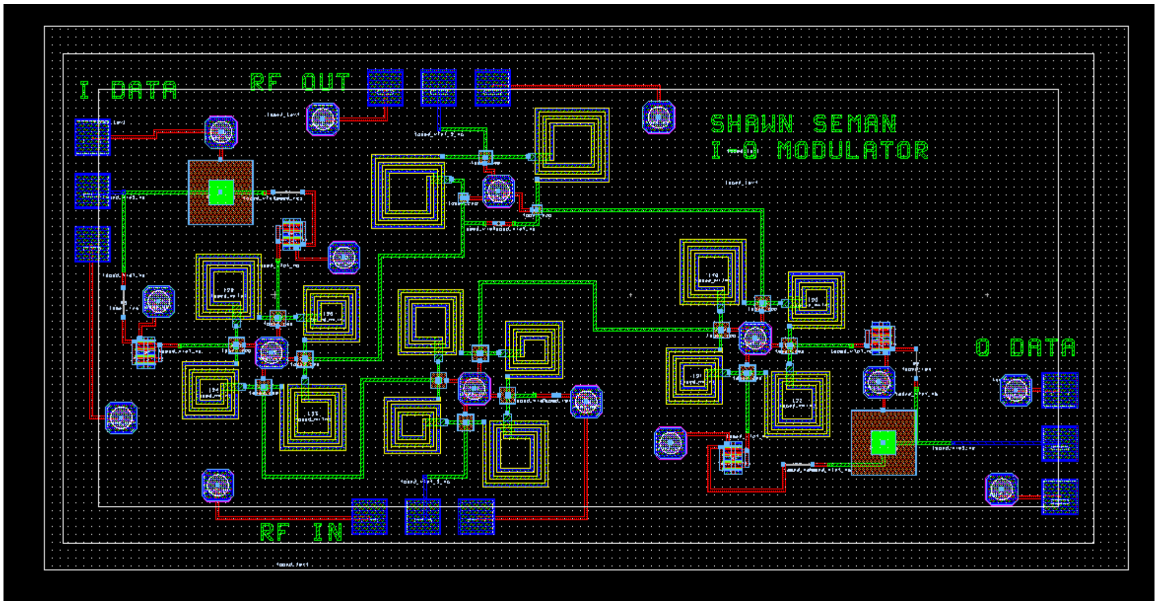
5.3) Wilkinson Power Divider



5.4) I-Q Vector Modulator



6.0) Layout



7.0) Test Plan

To test my I-Q vector modulator I will need a vector network analyzer (VNA) and two DC power supplies to bias the I and Q channels.

My plan is to test my design in three phases:

1) I will measure input match and gain across frequency for all four nominal QPSK phase states. The following table shows the DC voltages needed for these phase states:

θ	I	Q
45	0.05	0.05
135	-0.66	0.05
-135	-0.66	-0.66
-45	0.05	-0.66

2) I will measure input compression point and generate a constellation diagram at 5500 MHz for all four nominal phases states listed in Step 1.

3) I will tune the I and Q bias voltages to create a constellation diagram that places the phase states at exactly +45°, +135°, -135°, and -45° with equal magnitudes. This will involve setting the I and Q voltages somewhere between 0.05 and -0.66 V.

8.0) Summary and Conclusion

The use of TriQuint's 0.5 um PHEMT GaAs process in conjunction with ADS enabled the development of a MMIC I-Q vector modulator in the WLAN frequency band. Expectations from simulated data are that this modulator will operate over a wide bandwidth with low insertion loss. The flexible architecture of the design will enable the design to be tuned to an optimal performance level via the biasing of the I and Q channels. The design also has the additional appeal of being compatible with both QPSK and BPSK systems.

The one area of concern with this design is that simulated data shows the input compresses at a much lower power level when the phase state is set to -135º. In this phase state the PHEMT's in the reflective attenuators are biased near pinch-off, so it will be interesting to see if the simulations are accurate.

The hardest challenge posed during the design process was developing the reflective attenuators. As discussed in the Design Approach section, usually the difficult aspect of this particular design is the parallel capacitance present in the drain of the PHEMT. However even using pure resistances to load the through and coupled ports of the branch-line hybrid, I could not create an ideal reflective attenuator with TriQuint inductors and capacitors. Therefore for this design to perform more optimally without requiring tweaks on the I and Q channel bias voltages, I would recommend doing the design with distributed elements if at all possible.

9.0) References

Penn, John E. "A Balanced Ka-Band Vector Modulator MMIC." Microwave Journal, June 2005

Egan, Jonathan. "Vector Modulator." MMIC Design Final Report, Fall 2006

Pozar, David M. "Microwave and RF Design of Wireless Systems." Jon Wiley & Sons, Inc. 2001

http://en.wikipedia.org/wiki/Phase-shift_keying