

A 3.3V, 2.4GHz 0.5 μ m GaAs Common-Source, Two-Stage Low-Noise Amplifier

by

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ABSTRACT

Abstract — This paper presents a 3.3V battery operated, 0.5 μ m Gallium Arsenide (GaAs) low-noise amplifier (LNA) operating at 2.4GHz. Using a common-source configuration with two stages and EMODE pHEMT transistors, the designed amplifier provides a noise figure of less than 2.2dB in conjunction with a power gain of greater than 26dB. Focusing on a low power consumption design, this LNA operates using a 3.3V battery and draws less than 20mW. A shunt resistor on the drain along with a feedback resistor between the drain and gate were utilized to eliminate potential stability problems. The ideal elements are replaced with the foundry library elements and a layout is generated in preparation for fabrication. A test plan is discussed for evaluating the fabricated device and allowing for a comparison of the measured results to the simulated performance.

Keywords — MMIC, 0.5 μ m Gallium Arsenide (GaAs), Low-Noise Amplifier, Common-Source

1. INTRODUCTION

The overall theme of the design project for the Johns Hopkins University EE787 Microwave Monolithic Integrated Circuit (MMIC) Design course is a configurable S-band or C-band duplex transceiver. This paper will focus on the S-band frequency regime of the project, particularly the design and development of a low-noise amplifier (LNA). The S-band frequency range of interest is from 2.305 to 2.497 GHz, covering the wireless communications services (IEEE 802.11, Bluetooth, Wireless LANs) and the Industrial, Scientific, and Medical (ISM) radio bands. One key aspect of this project is that it will concentrate on small, lightweight, and low power designs that will be intended for battery powered operation, from 3.0 V to 3.6 V.

In a RF transceiver, the LNA is the first component in the receiver subsystem. Designed for low noise figure, the LNA is used to bound the receiving systems' overall noise figure. A low noise figure allows weak received signals to be amplified with minimal additive noise and distortion, thus increasing the dynamic range of the receiver. Large gain in the first stage of the receiving chain also factors into setting the overall noise figure of the receiver; however, a high gain and low noise figure amplifier is difficult to obtain using a single-stage design. Therefore, multi-stage designs are utilized to incorporate both of these desired traits.

This paper details the design of a 2.4GHz, 0.5 μ m GaAs common-source, two-stage LNA powered by a single 3.3V battery. Two 4 X 15 μ m (60 μ m) EMODE pHEMTs are used in the design due to their high gain and low noise characteristics with low bias power. Several aspects of the design affect the amplifiers performance. First, the output and intermediate matching networks are used to obtain maximum gain as well as to maintain a good impedance match. Second, the input matching network sets the noise figure for the design. Lastly, a feedback circuit in addition to a shunt impedance is used on each of the amplifier stages to stabilize the amplifier and reduce power consumption.

2. LNA TOPOLOGY

Various topologies exist for LNA circuits, but the common-source topology was chosen for this design. A common-source design has the RF input signal applied to the gate of the transistor while the amplifier RF output signal is extracted from the drain. Any stabilizing resistors must be implemented on the output of the transistor so the thermal noise introduced is post-amplification. The input and output matching networks perform impedance transformations to provide noise and power matching, respectively. Ideally, an LNA would have low noise and high gain characteristics. However achieving power matching and noise matching require two different approaches that often result in two different solutions. Maximum output power occurs when the input impedance equals the conjugate match of the source impedance, resulting in $\Gamma_{in} = \Gamma_s^*$. The condition for minimal noise is met when $\Gamma_s = \Gamma_{opt}$. An input matching network (IMN) is designed to impedance match Γ_{opt} of the transistor to 50Ω , where Γ_{opt} is the optimum reflection coefficient for the lowest noise figure at a particular frequency. Figure 1 illustrates a common-source low noise amplifier circuit with stabilizing resistor, IMN, and OMN.

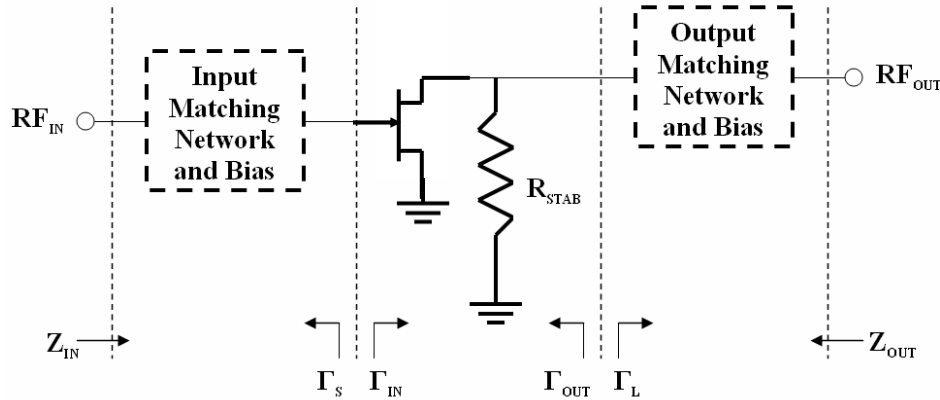


Figure 1. Common-Source LNA Topology

To achieve a high gain LNA, a two-stage design is employed. This architecture allows for the first stage to be designed with an extremely low noise figure, hence setting the overall noise figure of the LNA. Then the second stage provides the necessary amplification to achieve an overall high gain.

3. SIMULATION SOFTWARE PACKAGE AND FOUNDRY

3.1 SIMULATION SOFTWARE PACKAGE

Agilent Technologies Advanced Design System (ADS), version 2006A, was used as the simulation software package for this project. Linear and nonlinear circuit simulations were used to analyze the performance of the LNA, while the tuning and optimization capabilities were exploited to finalize the design. Elements in the TQPED process library from TriQuint Semiconductor were used to create a final design that accounts for parasitics in these non-ideal components.

3.2 FOUNDRY

TriQuint Semiconductor provides custom foundry services with capabilities including Gallium Arsenide (GaAs) wafer processing. Using proprietary libraries developed by TriQuint Semiconductor that are compatible with Agilent Technologies ADS simulation software package, more realistic simulations were performed and analyzed in the development of the LNA. The TQPED library, version 2.2, was used for the simulations provided in this paper.

4. DESIGN APPROACH

4.1 BIASING

The first step in the design process is to determine the DC operating point. This is accomplished by sweeping the drain voltage (VDS) and the gain voltage (VGS) of the transistor. The EMODE pHEMT is used in calculating the DC IV curves, shown in Figure 2. It is determined that an appropriate bias for the LNA is:

VDS = 2.4 V
 IDS = 3 mA
 VGS = 0.58 V

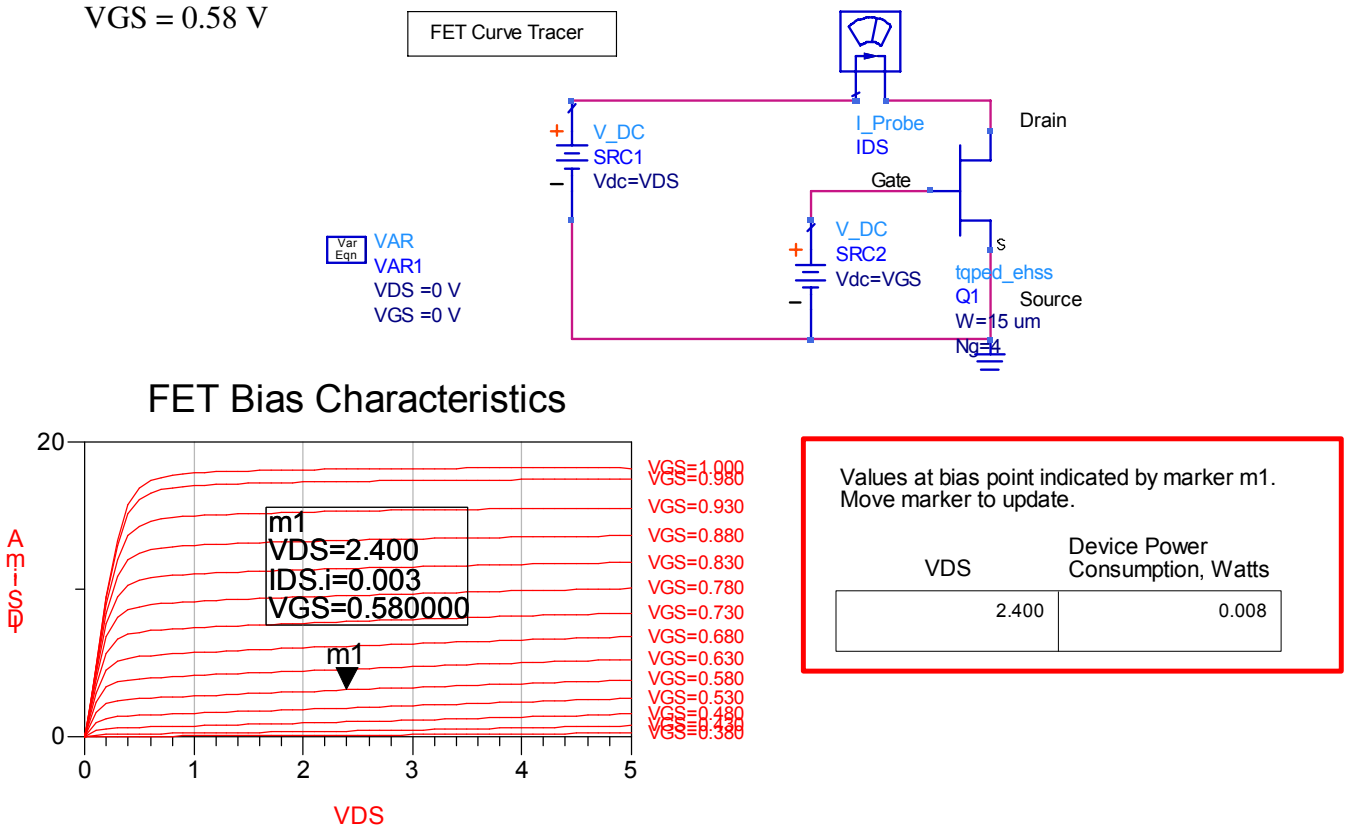


Figure 2. Determining an Appropriate DC Bias

Note that the biasing gate voltage is positive because the pHEMT is an EMODE. With this bias point the DC power for a single stage is 8 mW. The above bias voltages are less than the battery operating limits of 3.0V – 3.6V. Therefore, a resistor divider network will be used to drop voltage when the biasing network is designed. Initially ideal bias components are used when designing the LNA, and these will be replaced with nonideal components once the amplifier is completely designed.

4.2 STABILITY

The next step in the design process is to stabilize the transistor. Because the LNA is being designed for a minimum NF, the stabilizing network should be placed on the output side of the LNA. Two methods of stabilizing the transistor were studied, (1) a feed back resistor between the drain and gate, and (2) a shunt resistor on the drain. Both of these options were attempted separately, but neither provided unconditional stability. However, when used in conjunction with one another, the LNA became unconditionally stable from 100 MHz to 10 GHz.

Since the LNA is being designed to operate via a battery, it is essential to minimize wasted power loss in any portion of the stabilizing network. Therefore, DC blocking capacitors were used in series with the stabilizing resistors to minimize the amount of power dissipated by the resistors. DC blocking capacitors are also utilized to isolate the inter-stages of the amplifier in addition to the external RF ports on the amplifier from the various bias voltages.

4.3 INPUT AND OUTPUT MATCHING NETWORK

Subsequently the input matching network was designed for the best possible noise figure and the output matching network was designed for maximum gain as well as the best input and output match. Both networks are comprised of series capacitors and shunt inductors. It should be noted that all components are ideal in this initial design phase, including the components used in the previously discussed stabilizing network.

4.4 IDEAL SINGLE-STAGE DESIGN

After designing the input and output matching networks, a single-stage design is complete. Favorable results were obtained after simulating the design:

Gain = 13.6 dB
NF = 1.5 dB
Match (input) = -10 dB.
Match (output) = -46 dB

4.5 IDEAL TWO-STAGE DESIGN

After the ideal single stage design yielded promising results, two identical single stages were cascaded together. The ideal cascaded system provided the following performance:

Gain = 27.9 dB
 NF = 1.5 dB
 Match (input) = -7.5 dB
 Match (output) = -32dB

4.6 NON-IDEAL TWO-STAGE DESIGN

Next, the ideal components were replaced with TriQuint components and the design was tuned and optimized. As expected, the performance of the system was degraded due to the parasitic losses modeled in the TriQuint components. The non-ideal cascaded system provided the following performance:

Gain = 26.2 dB
 NF = 2.1 dB
 Match (input) = -5.0 dB
 Match (output) = -40.9 dB.

The last step in the design was to design the DC bias network. To reduce complexity in the layout of the design it is of interest to bring in only one battery to supply the drain and gate voltages for both pHEMTs. Because this LNA is designed for a VDS value less than 3.0 V to 3.6 V a resistor divider network is implemented. One leg of the divider drops the voltage down to approximately 2.4 V to supply the drain voltage and another leg of the divider drops the voltage down to 0.58 V to supply the gate voltages. One single resistor divider network is used to provide power to both pHEMTs.

5. SPECIFICATIONS VS GOALS

Table 1 compares the initial design goals to anticipated performance based on the non-ideal design simulations.

Table 1. Design Goals vs. Simulated Performance

| Parameter | Design Goal | Simulated Performance |
|----------------------------|---------------------|-----------------------|
| Center Frequency [f_c] | 2.305-2.497 GHz | 2.4 GHz |
| Bandwidth | > 200 MHz | 200 MHz |
| Gain [S_{21}] | > 24 dB | 26.9 dB (nom) |
| Gain Ripple | ± 0.5 dB | ± 1.0 dB |
| Noise Figure [NF] | < 3 dB | 2.06 dB (nom) |
| Input IP3 | > 0 dBm | -12 dBm |
| Input VSWR | < 1.5:1 | 4.1:1 (nom) |
| Output VSWR | < 1.5:1 | 1.07:1 (nom) |
| Supply Voltage | 3.0 – 3.6 V | 3.3 V |
| Size | 60 x 60 mil ANACHIP | 60 x 60 mil ANACHIP |

6. TRADEOFFS

The first tradeoff in this design was encountered near the beginning of the design process. It involved stabilizing the circuit. There was no easy way to stabilize the system without using a feedback network. Initially it was a concern that this topology would feed noise back into the system. However, after running simulations, the noise fed back into the system was not enough to compromise the system. It was still well below the 3dB NF goal.

Another tradeoff encountered was trying to optimize gain and output match as well as noise figure and input match. A nominal gain of 26.1 dB was achieved across the band, while at the same time a 1.4:1 output VSWR was maintained. The gain ripple was not bad, at a value of ± 1 dB, but did not meet the ± 0.5 dB goal. Also, a nominal NF of 2.2 dB was achieved. However, the input VSWR was not desirable, at a nominal value of 4.7:1. No way was found to meet the goals for all these parameters simultaneously; such is the nature of a tradeoff.

7. FINAL DESIGN

The final design of the two-stage, common-source LNA design using TriQuint library components is presented. Figure 3 illustrates the overall schematic of the final design with the complete bias circuit included.

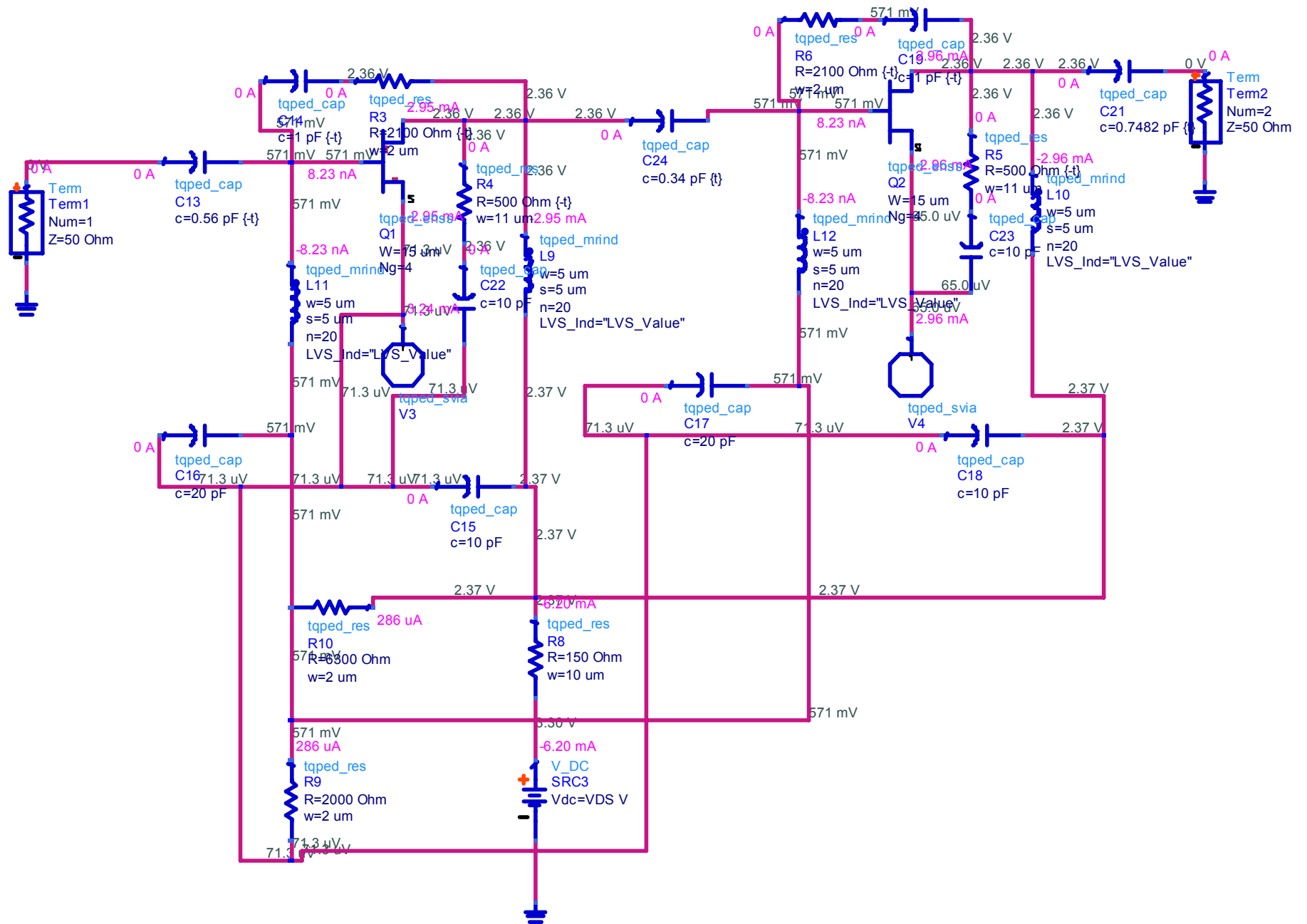


Figure 3. Final Design Schematic with DC Bias

Figures 4a-4d illustrate the simulated S-parameters of the final design. Both a broadband and narrowband view of the response is shown. The markers indicate the performance at the designed center frequency.

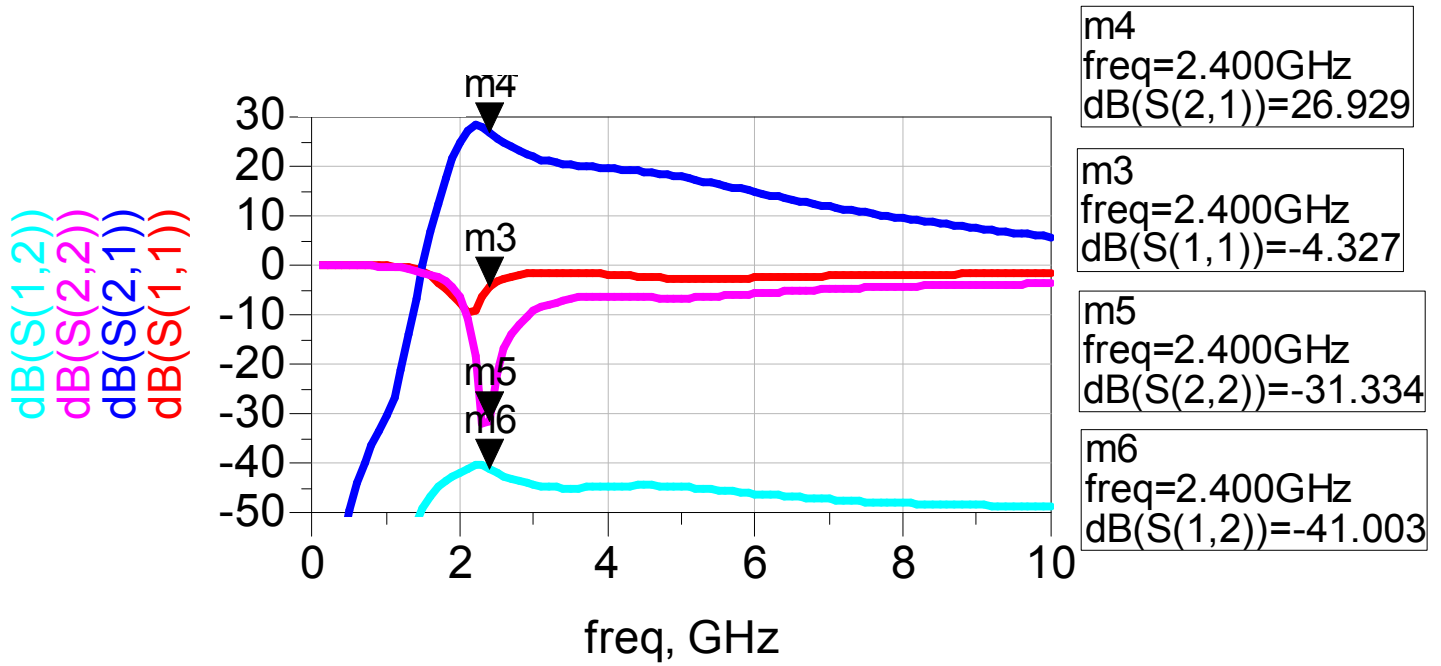


Figure 4a. S-Parameters (Broadband) of Final Design

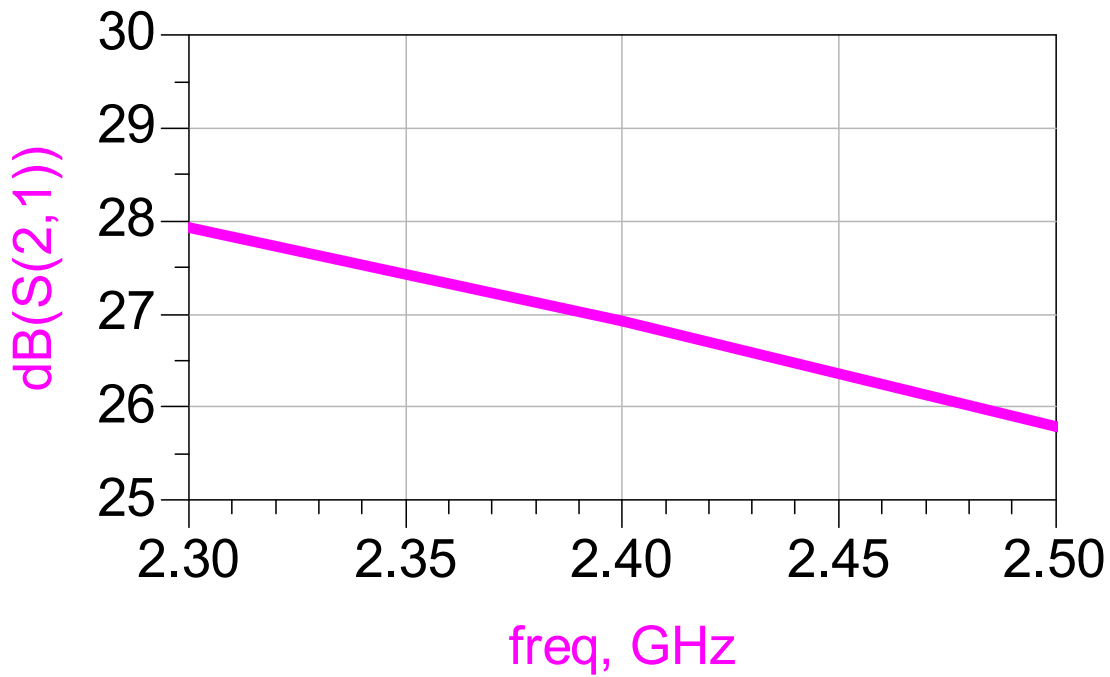


Figure 4b. Gain (S₂₁) of Final Design

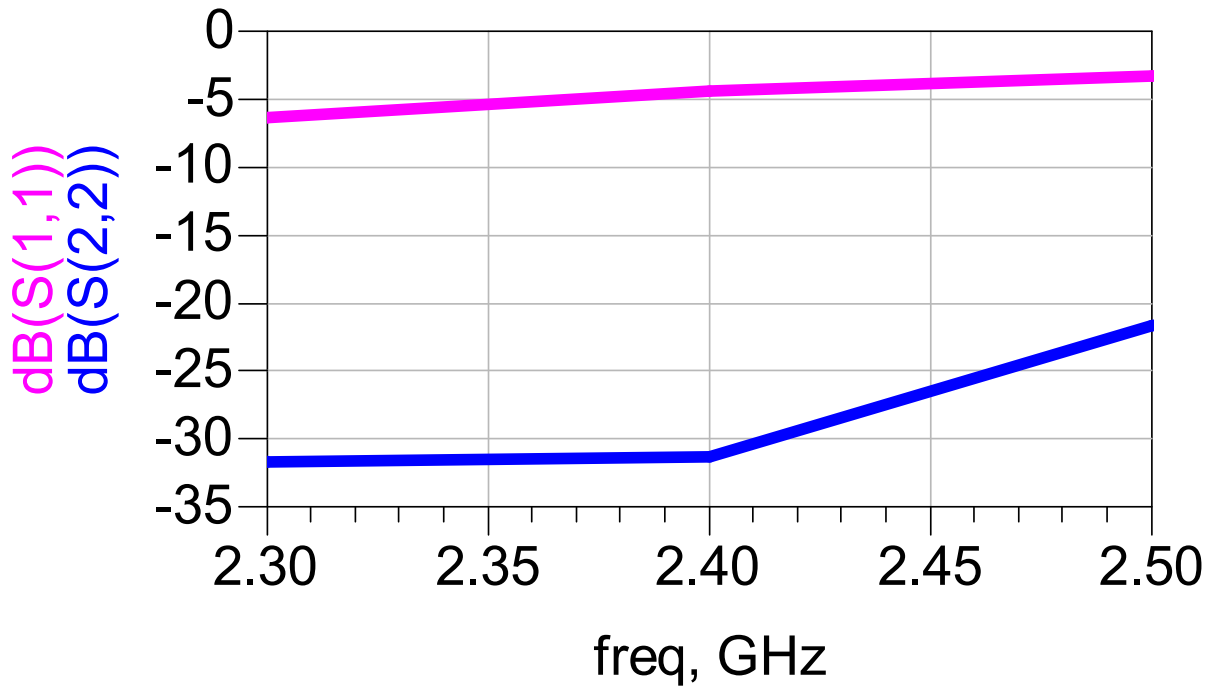


Figure 4c. Input/Output Matching (S_{11}/S_{22}) of Final Design

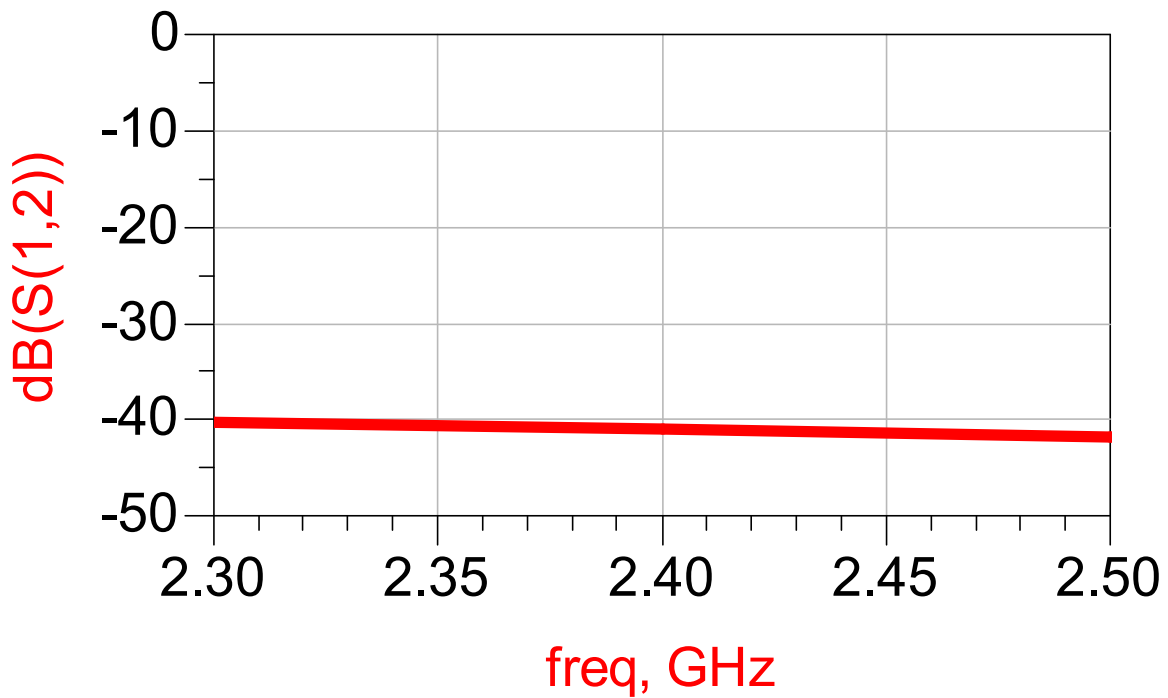


Figure 4d. Reverse Isolation (S_{21}) of Final Design

Figure 5a displays the simulated broadband noise figure of the final design and the theoretical achievable minimum noise figure. The markers indicate the performance at the designed center frequency. A narrowband view of the response is shown in Figure 5b.

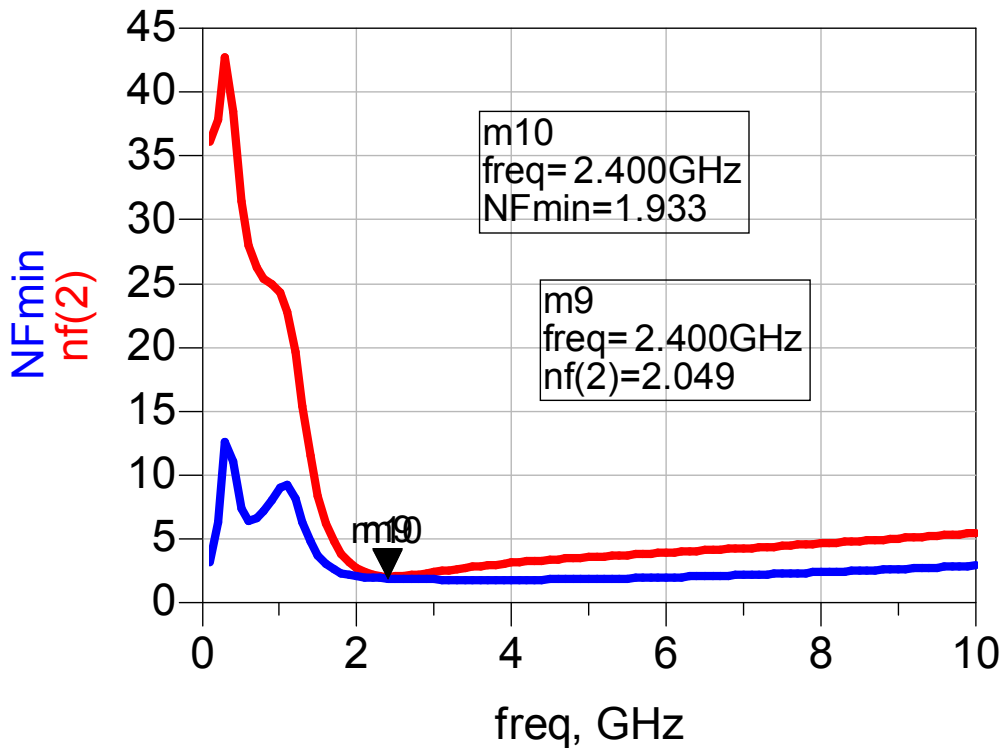


Figure 5a. Noise Figure (Broadband) of Final Design

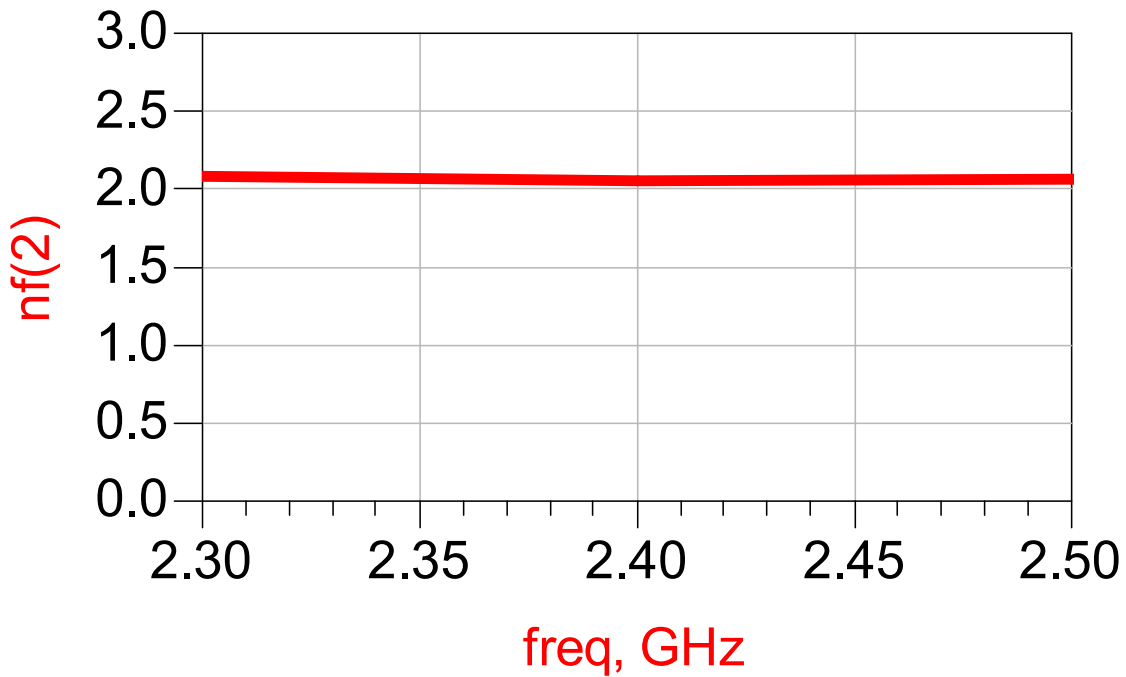


Figure 5b. Noise Figure (Narrowband) of Final Design

Figure 6 displays the simulated stability of the final design. Note that all μ (Mu) values are greater than 1 across the broad frequency range.

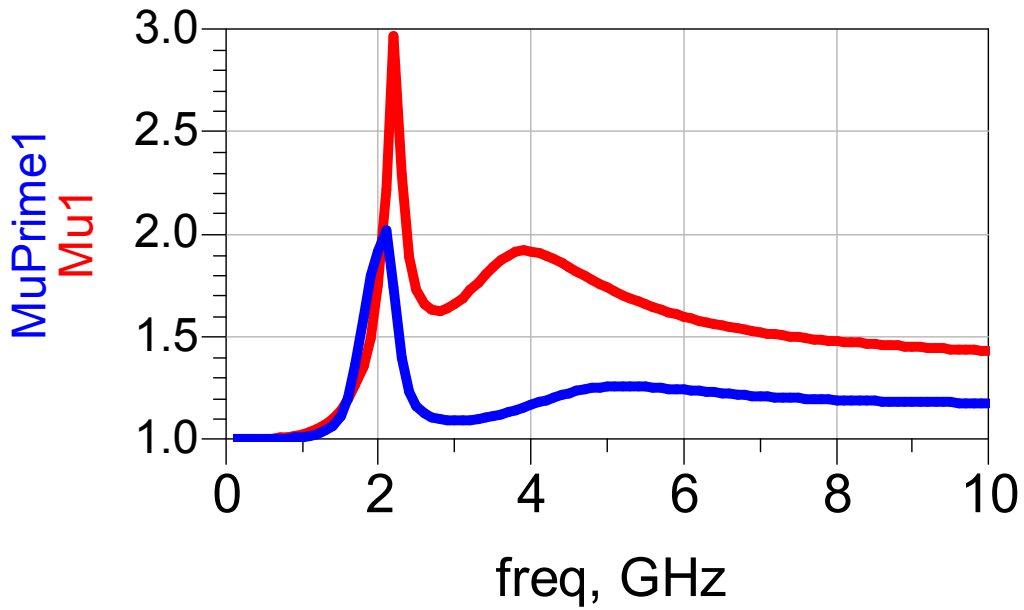


Figure 6. Stability of Final Design

Figure 7 illustrates the simulated third order intercepts (IP3) of the final design. The red curve is the first-order response while the blue curve is the third-order response. The theoretical intersection point of these two curves (displayed by the dashed lines stemming from the linear region of the amplifier) designates the IP3 point, which is approximately -12dBm relative to the input RF power.

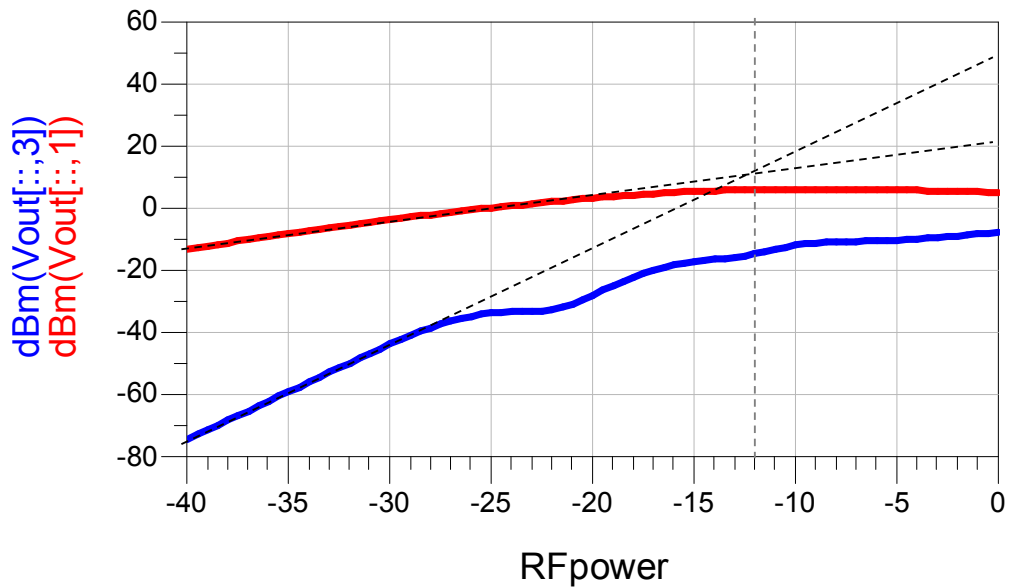


Figure 7. Third-Order Intercept of the Final Design

Several attempts were made before successfully placing all of the components in the layout. Precaution was taken to ensure there was enough space between inductors and other components so as not to introduce coupling into the system. Also, care was taken to place the ground vias as close as possible to the ground-signal-ground (GSG) pads. Lastly, it was important to ensure that the traces, as well as resistors, were large enough to handle the amount of current that the simulation predicted would run through them. Figure 8 illustrates the final design layout.

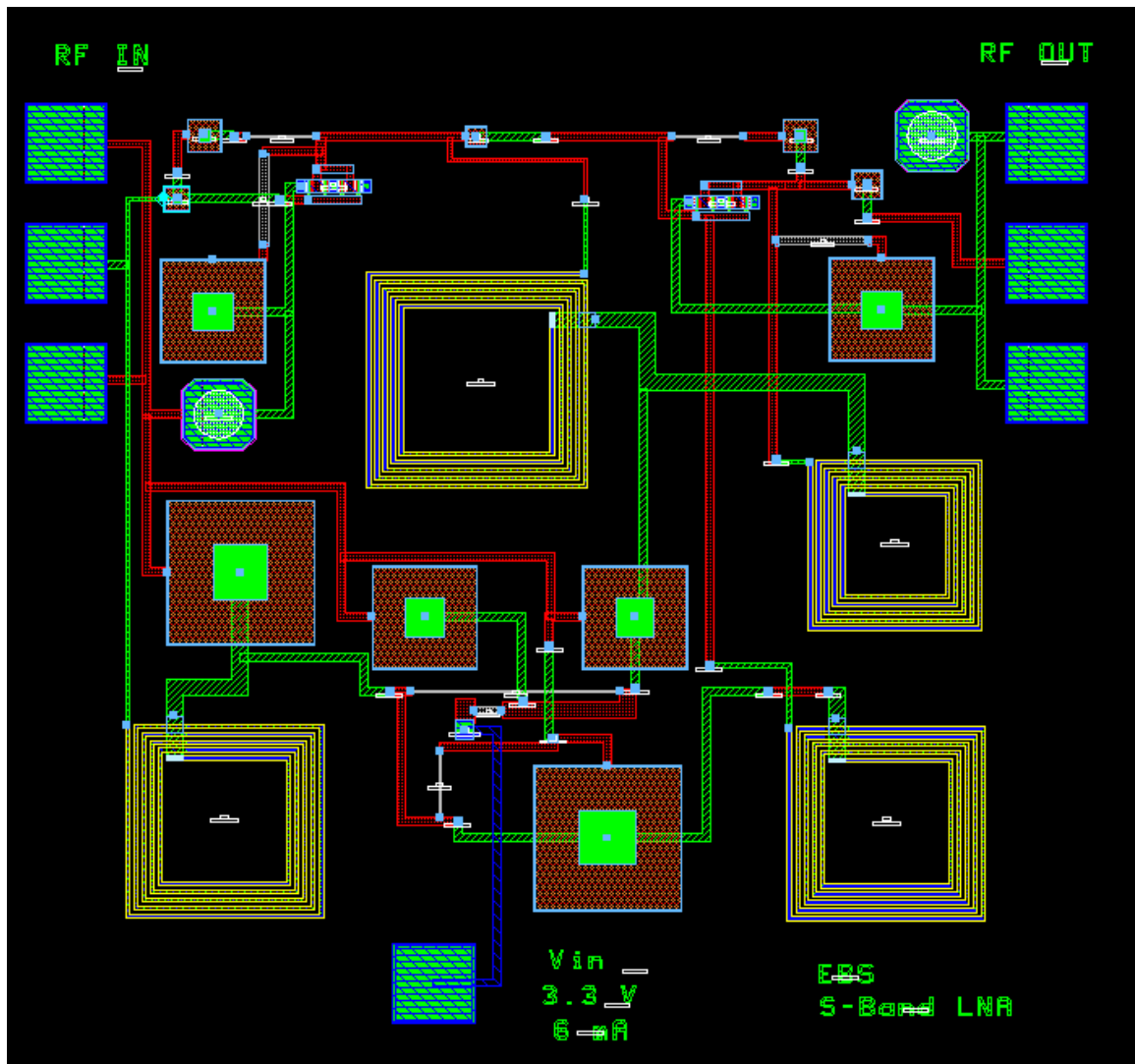


Figure 8. Final Design Layout

8. TEST PLAN

There are three measurements of interest for the LNA: (1) S-parameter measurements, (2) noise figure measurements, and (3) compression measurements.

First, power must be applied to the chip. To do this, apply a needle probe to the Vin pad on the chip. Slowly, increase the voltage to 3.3 V and verify that the power supply is drawing approximately 6.2 mA of current.

For the s-parameter measurements, first calibrate the network analyzer. Then, connect the GSG probes to the RF IN pad and the RF OUT pad on the chip. Finally measure the s-parameters on the network analyzer and save the data to a disk.

A similar setup is employed when taking the noise figure measurements. First calibrate the noise figure meter. Apply a noise source at the RF IN side of the chip. Take a measurement at the RF OUT side of the chip and save the data.

A signal generator in conjunction with a spectrum analyzer is used to make the compression measurements. Connect the signal generator to the RF IN side of the chip. Connect the spectrum analyzer to the RF OUT side of the chip. Set the signal generator to 2.4 GHz. Start at -40 dBm, and sweep the input power in 1dBm increments until compression is reached. Save the data to a disk.

9. SUMMARY

Overall, the designed LNA exhibits low noise figure, high gain, high reverse isolation, and low DC power consumption all encompassed in a compact layout. The gain ripple is slightly larger than the design goal, but still is comparable with COTS LNAs. In addition, the design goal for input VSWR was not achieved, but a tradeoff could be made to sacrifice some noise figure and/or gain to attain a better input match. The main focus of designing a compact, low power consumption device operable via a single battery cell was successfully accomplished. A comparison of measured results to the simulated performance will allow for validation of the models used in the design.