

Minhaj Raza
EE 787
WIDE BAND LOW NOISE AMPLIFIER
1.2-3GHz
Dec 9th 2008

Abstract:

The design of a Monolithic Microwave Integrated Circuit (MMIC) low power low noise amplifier (LNA) circuit will be described in this paper. The use of LNA Design is applicable in the industrial fields of GPS, Medical, and Cellular technologies. The amplifier operates with 3 VDC supply voltage at VDD and a 0.75 VDC at VGG and total current draw of 76 mA. The amplifier has a 1 dB bandwidth of more than 1.8 GHz (1.2 GHz-3 GHz). The amplifier has the NF of less 1.7 db throughout its working frequency. The amplifier achieves a power gain of 29 dB with the input 1 dB compression point of -14.5 dBm. The amplifier has the input port match (S11) of -14dB or better, and in addition the output port match (S22) is also -13 dB or better. The unconditional stability of the LNA is also observed for the entire working frequency.

Introduction:

This report will focus on the design, simulation, layout, optimization and test plan for the low power low noise amplifier. The normal use of a LNA is at the front end of the RF receiver system providing the first stage of amplification after the receive antenna and adding as little noise as possible with providing the maximum gain. Large gain in the first stage of the receiving chain also factors into setting the overall noise figure of the receiver; however, a high gain and low noise figure amplifier is difficult to obtain using a single-stage design. Therefore, multi-stage designs are utilized to incorporate both of these desired traits.

Design Approach:

The design consists of a two-stage amplifier design powered by a positive 3VDC source for drain ports of the PHEMT and another 0.75 VDC source for the gate ports of the PHEMT. Two 6 X 50um EMODE FET's are used in the amplifier due to their higher gain and lower noise figure. A feedback resistor in series with a capacitor was used to flatten the output response of the LNA as shown in Figure 1.

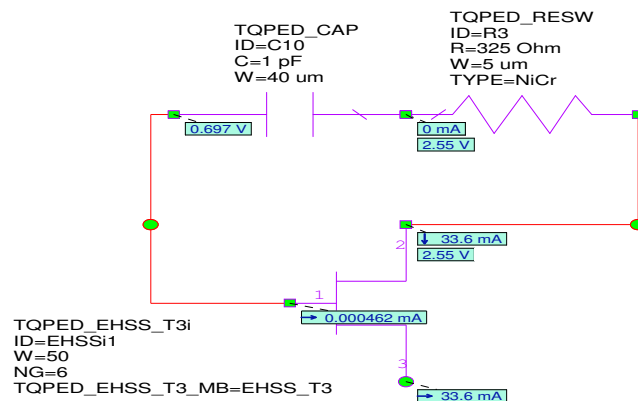


Figure 1. PHEMT with feedback Resistor

The simplest form of the design (common-source) was used to approach the design goals. In it, the RF input signal is applied to the gate of the PHEMT while amplifier RF output signal is extracted from the drain port. The input and output matching networks perform impedance transformations to provide noise and power matching, respectively. The goal is to have low noise and high gain characteristics at the same time. Maximum output power occurs when the input impedance equals the conjugate match of the source impedance, resulting in $\Gamma_{in} = \Gamma_s^*$. The condition for minimal noise is met when $\Gamma_s = \Gamma_{opt}$. An input matching network (IMN) is designed to impedance match Γ_{opt} of the transistor to 50Ω , Γ_{opt} is the the optimum reflection coefficient or the lowest noise figure at a designed frequency (2GHz). This information was obtained from the .s2p data file of the measured data provided in the class. Figure 2 shows a generalize input and output matching circuit of an amplifier except for a series resistor added prior to the output matching network.

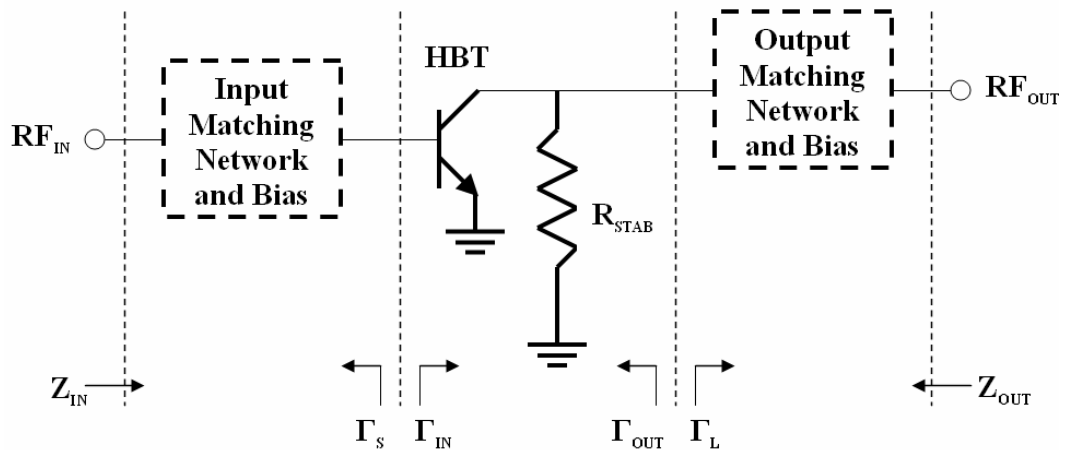


Figure 2. Input and Output Matching

The stability of the circuit was observed at this point, and it was noticed that a stabilizing circuit network was required to add stability resistors to stabilize the the LNA for the entire working frequency. Figure 3 shows a output stability circuit.

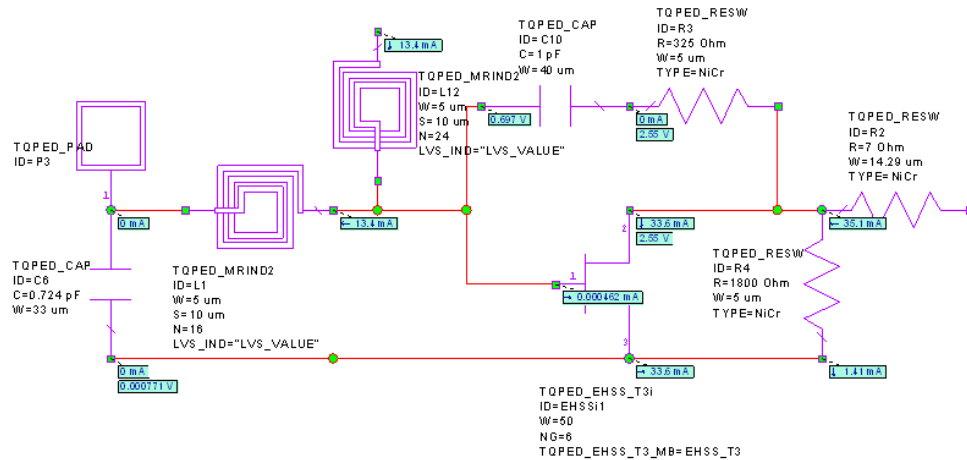


Figure 3. Output Stability Resistor Network

To achieve a high gain LNA, a two-stage design is employed. This architecture allows for the first stage to be designed with an extremely low noise figure, hence setting the overall noise figure of the LNA. Then the second stage provides the necessary amplification to achieve an overall high gain.

SIMULATION SOFTWARE

Applied Wave Research (AWR) Microwave Office provided by the Applied Wave Research version 9.01 Build 4229 rev1 (58736), was used as the simulation software package for this project. Linear and nonlinear circuit simulations were used to analyze the performance of the LNA. Elements in the TQPED process library TQOR_TQPED v1.1.21 from TriQuint Semiconductor were used to create a final design that accounts for parasitics in these non-ideal components. The initial design was generated using the lumped elements and gradually these lumped elements were replaced by TriQuint parts.

BIASING

The first step in the design process is to determine the DC operating point. This is accomplished by sweeping the drain voltage (VDS) and the gate voltage (VGS) of the transistor. The EMODE pHEMT is used in calculating the DC IV curves, shown in Figure 4. It is determined that an appropriate bias for the LNA is:

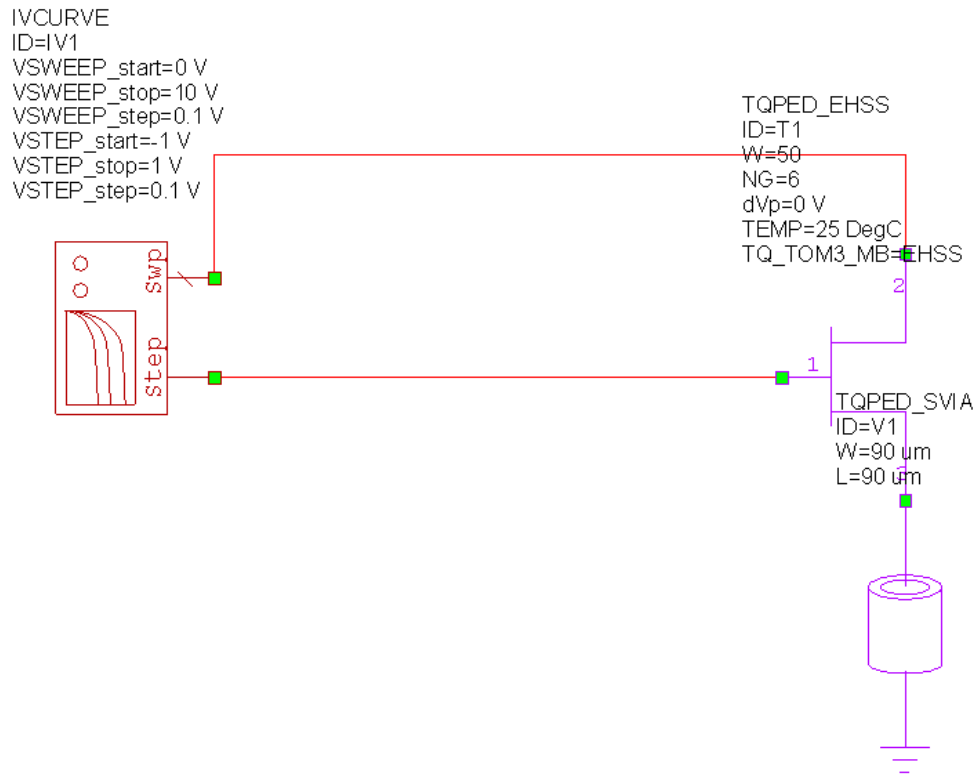


Figure 4. IV Curve Circuit

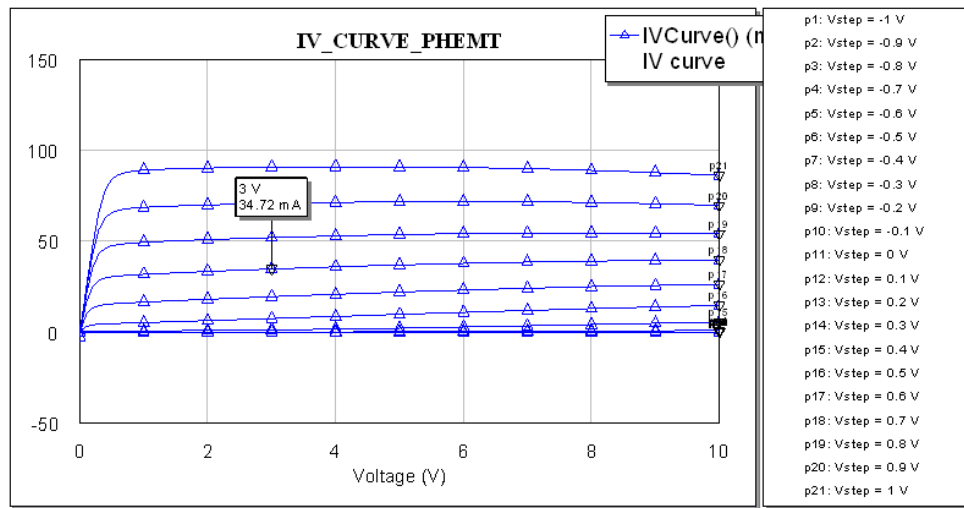


Figure 5. IV Curve for the PHEMT

Note that the biasing gate voltage is positive because the pHEMT is an EMODE.

STABILITY

The next step in the design process is to stabilize the transistor. Because the LNA is being designed for a minimum NF, the stabilizing network should be placed on the output side of the LNA. Two methods of stabilizing the transistor were studied, (1) a feed back resistor between the drain and gate, and (2) a shunt resistor and a series resistor on the drain. Both of these options were attempted separately, but neither provided unconditional stability. However, when used in conjunction with one another, the LNA became unconditionally stable from 1 GHz to 3.2 GHz.

Since the LNA is being designed to operate via a battery, it is essential to minimize wasted power loss in any portion of the stabilizing network. Therefore, DC blocking capacitors were used in series with the stabilizing resistors to minimize the amount of power dissipated by the resistors. DC blocking capacitors are also utilized to isolate the inter-stages of the amplifier in addition to the external RF ports on the amplifier from the various bias voltages.

INPUT AND OUTPUT MATCHING NETWORK

Subsequently the input matching network was designed for the best possible noise figure and the output matching network was designed for maximum gain as well as the best input and output match. Both networks are comprised of series capacitors and shunt inductors. It should be noted that all components are ideal in this initial design phase, including the components used in the previously discussed stabilizing network.

IDEAL SINGLE-STAGE DESIGN

After designing the input and output matching networks, a single-stage design is complete. Favorable results were obtained after simulating the design:

Gain = 15 dB

NF = 1.5 dB

Match (input) = -15 dB.

Match (output) = -20 dB

IDEAL TWO-STAGE DESIGN

After the ideal single stage design yielded promising results, two identical single stages were cascaded together. The ideal cascaded system provided the following performance:

Gain = 29.2 dB

NF = 1.65 dB

Match (input) = -13 dB

Match (output) = -22dB

Final Design:

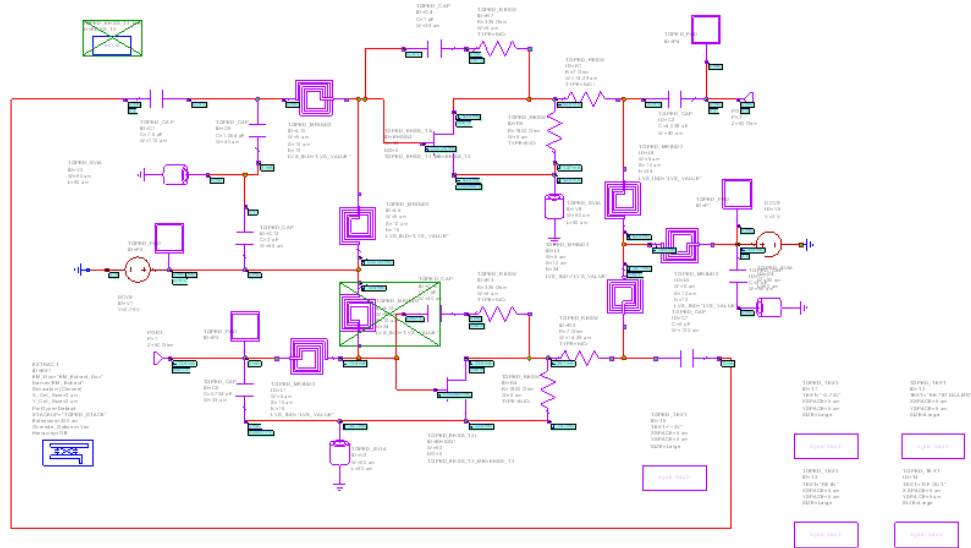


Figure 6. Complete Circuit Design of the LNA with TriQuint Parts

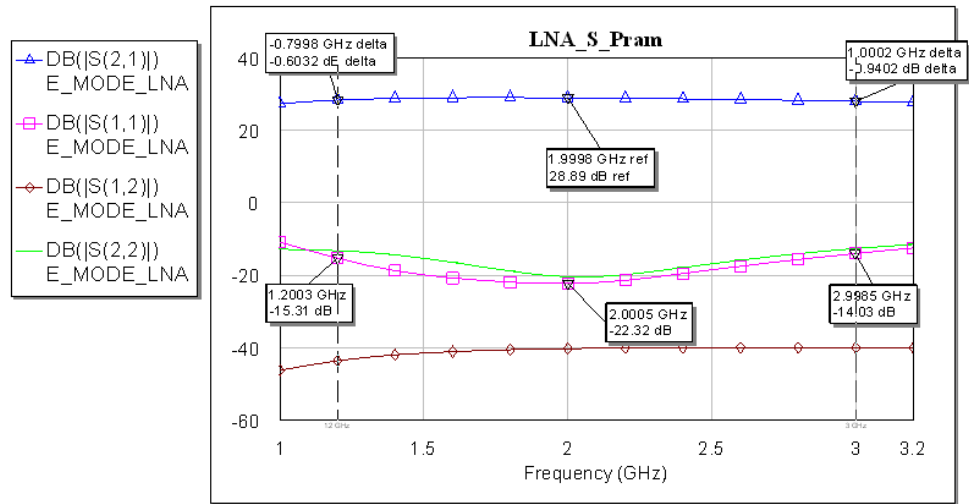


Figure 7. Linear / S-Parameters of LNA

It was observed that by comparison the E-mode PHEMT has better gain response with a low Noise Figure than the D-mode.

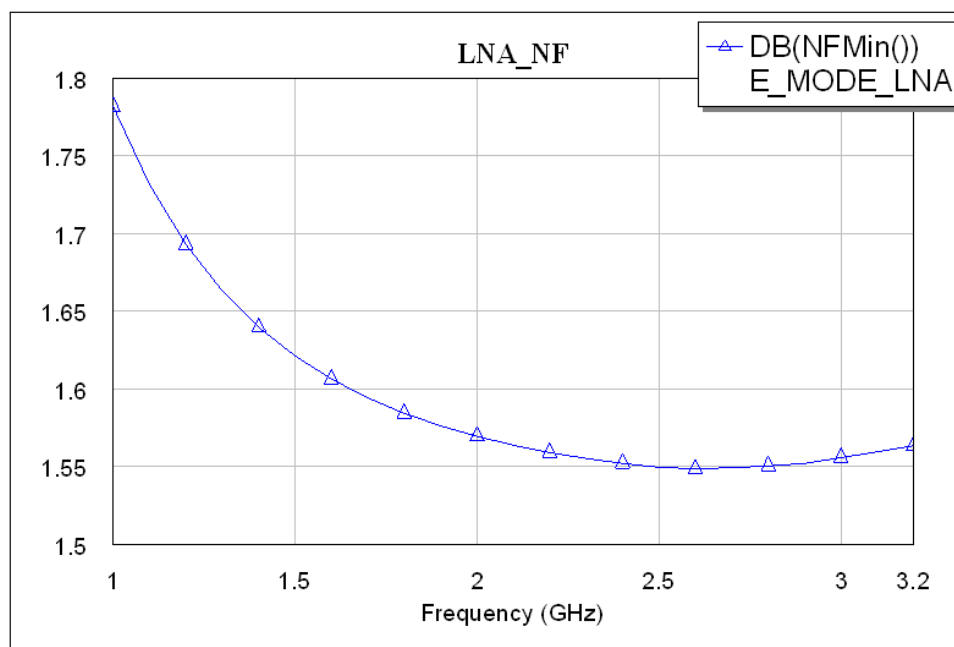


Figure 8. Noise Figure Response of the PHEMT

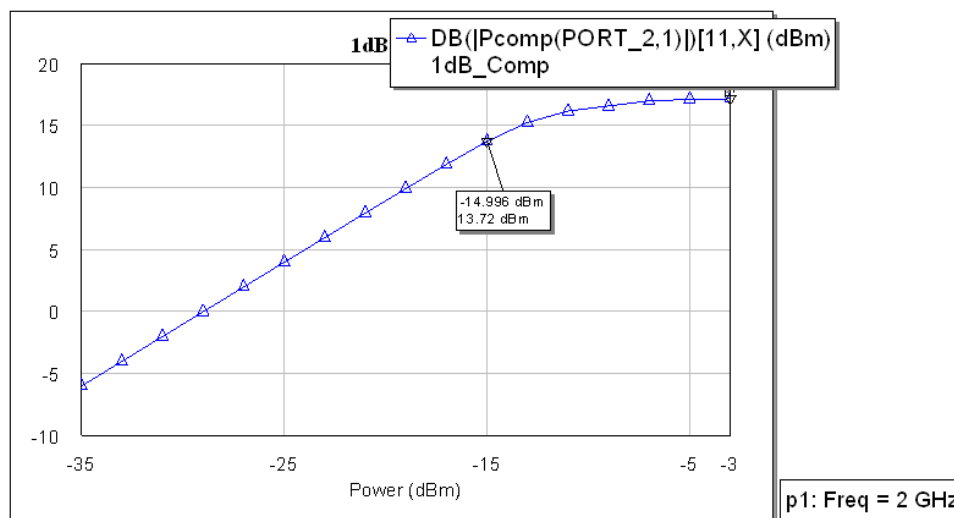


Figure 9. 1 dB compression point for the LNA

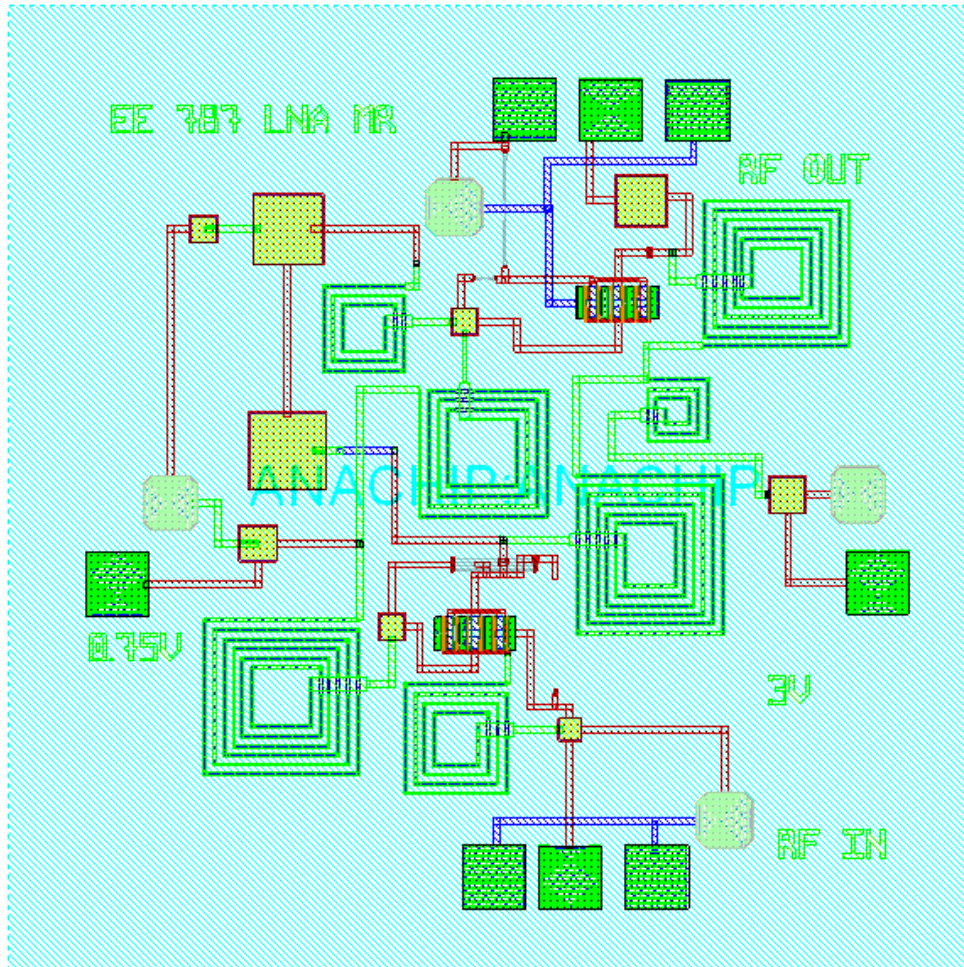


Figure 10. Final Layout of the LNA

TEST PLAN

There are three measurements of interest for the LNA: (1) S-parameter measurements, (2) noise figure measurements, and (3) compression measurements.

First, power must be applied to the chip. To do this, apply a needle probe to the voltage supply to 0.75 and 3 volts pads on the chip. Slowly, increase the voltage to 3 VDC with also providing 0.75 VGS and verify that the power supply is drawing approximately 36 and 45 mA of current for both stages.

For the s-parameter measurements, first calibrate the network analyzer. Then, connect the GSG probes to the RF IN pad and the RF OUT pad on the chip.

Finally measure the parameters on the network analyzer and save the data to a disk. A similar setup is employed when taking the noise figure measurements. First calibrate the noise figure meter. Apply a noise source at the RF IN side of the chip. Take a measurement at the RF OUT side of the chip and save the data.

A signal generator in conjunction with a spectrum analyzer is used to make the compression measurements. Connect the signal generator to the RF IN side of the chip. Connect the spectrum analyzer to the RF OUT side of the chip. Set the signal generator to 2.4 GHz. Start at -40 dBm, and sweep the input power in 1dBm increments until compression is reached. Save the data to a disk.

SUMMARY

Overall, the designed LNA exhibits low noise figure, high gain, high reverse isolation, and nominal DC power consumption all encompassed in a compact layout. A comparison of measured results to the simulated performance will allow for validation of the models used in the design.