

Matthew Crowne
525.787 MMIC Design
Fall 2008
Instructor: John Penn
C-Band Low Power PA

Abstract

A C-Band power amplifier for lower power applications was designed using the Triquint GaAs MMIC library and Applied Wave Research's Microwave Office design environment. The amplifier consists of two cascaded stages and is intended to maximize efficiency over other design parameters. The amplifier is centered at 5.5 GHz and achieves 38% power added efficiency and 20 dB of Gain across a +/- 200 MHz bandwidth with 9 dBm output power.

Introduction

A single ended C-Band power amplifier was designed for maximum efficiency on a Triquint MMIC process. The amplifier consists of two stages utilizing enhancement mode GaAs PHEMTs with on-chip matching networks. The driver stage has a gate periphery of 16um and is biased class AB. The final stage has 72um of gate periphery and is biased deep class B. The design is intended to run off a single 3.3V supply and has internal bias circuitry to produce the gate voltage. In Addition, separate gate pads are provided that can both check the bias points of the PHEMTs or, if necessary supply gate bias. This design allows maximum flexibility for prototype development.

A simplified schematic is shown in Figure 1. The output matching network was designed to maximize efficiency. The interstate match also had to be designed for gain and efficiency, while the input match could focus on increasing gain.

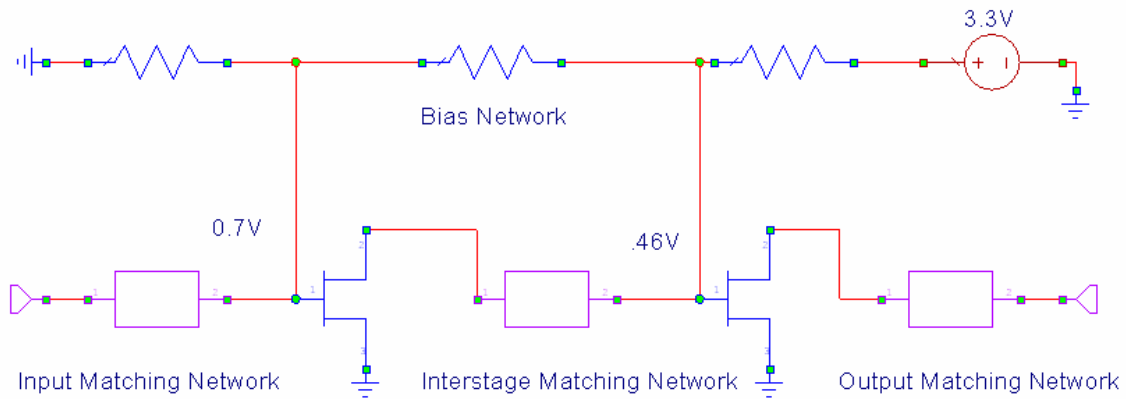


Figure 1. – Simplified Schematic

Table 1 summarizes key performance parameters across the operating bandwidth.

Frequency	Pout	Gain	PAE
GHz	dBm	dB	%
5.3	9.58	20.39	38
5.5	9.89	20.74	43.25
5.7	9.26	20.15	40.27

Table 1. - Key Performance Parameters

Design Approach

The amplifier was designed to maximize efficiency for a low power application. The metrics used to design this amplifier are summarized in Table 2

	Spec	Goal
BW:	5.3 Ghz-5.7GHz	
Pout:	9 dBm	10 dBm
PAE:	>40%at fc	40% across the bandwidth
Gain Ripple:	+/- 0.5	+/- 0.5

Table 2. – Specifications and Goals

Several approaches were investigated for meeting these specifications. Approaches that seemed promising early in the design phase utilized class-F or some other high efficiency technique. However, such an approach requires more components than a traditional matching network. Ideal simulations that appeared promising quickly lost their appeal when the low quality inductors inherent with Triquint and other GaAs MMIC processes. When the results reduced to efficiencies that are achievable with a deep class B approach the simpler matching networks they offered became more attractive. The DCIV plots are shown in Figure 2. For the driver stage $V_{gs} = 0.7V$ and for the final stage $V_{gs} = 0.5V$. These values were tuned in the final design

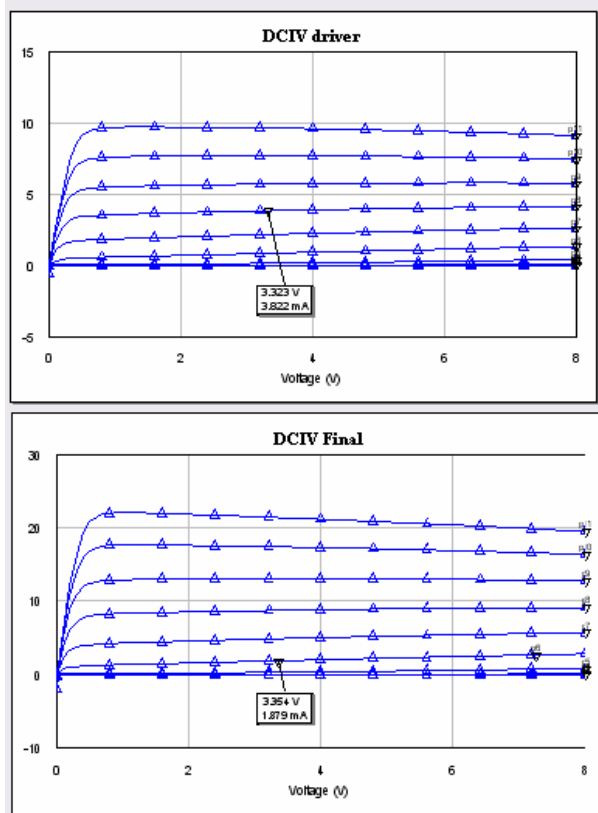
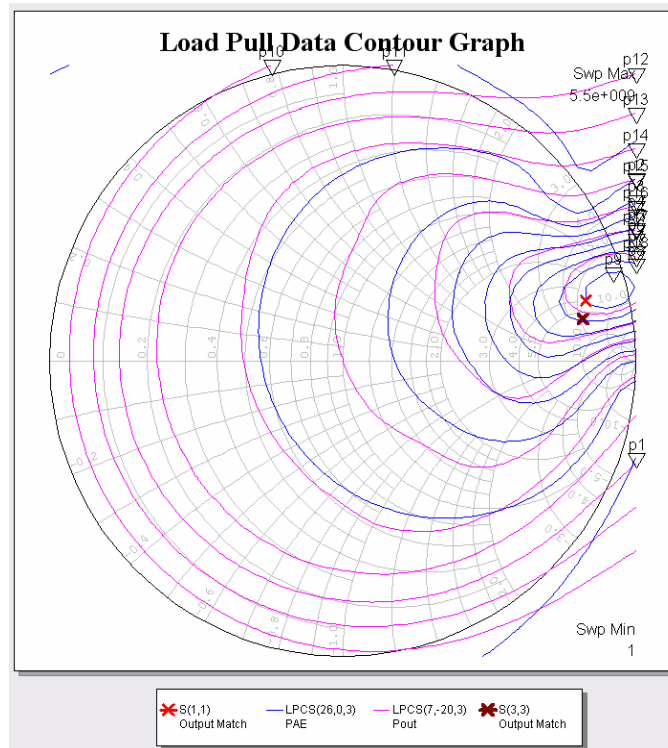


Figure 2 – DCIV curves

As a deep class B bias excluded a Cripps method approach to determining optimum output load, a load-pull simulation was performed on the output FET model. The load pull contours are shown in figure 3 for 5.5 GHz. The simulated ideal output matching network is indicated with the red “x” and the maroon “x” is the output match from the finalized layout.



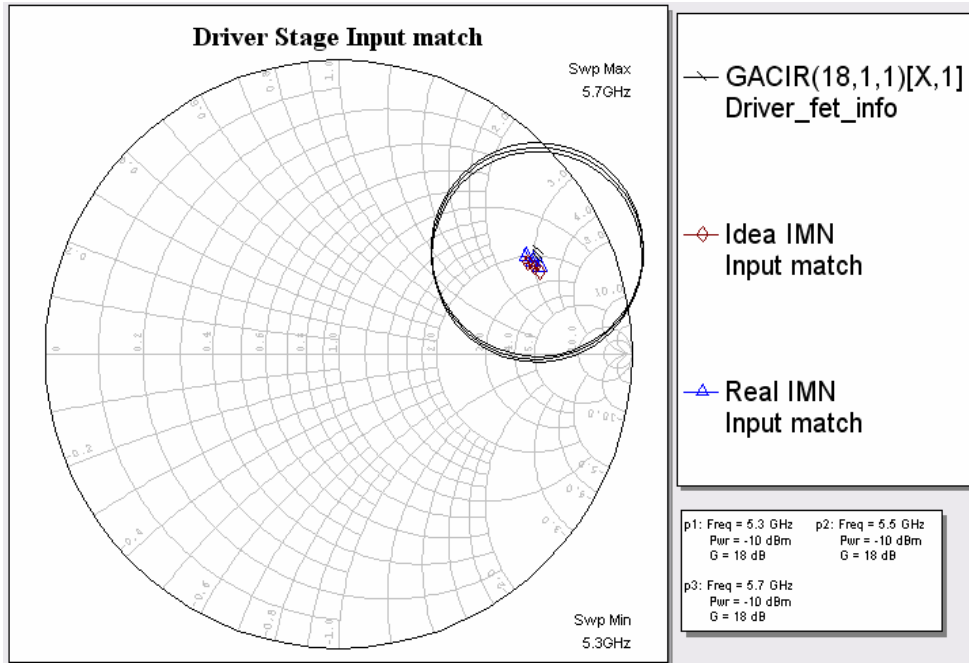


Figure 4. – Available gain circles and input match for the driver stage

The design is stabilized with a shunt resistor on the power device with a large cap to ground. In this location the resistor will not dissipate significant RF power and the DC blocking cap to ground ensures no DC power dissipates in the resistor. It was decided not to put a stabilizing resistor onto the driver stage as a significant amount of gain was lost with the addition of the 200 ohm resistor on the final. The combined amplifier has an input and output mu value greater than 1 and with 50 ohm terminations the amplifier should not oscillate. Figure 5 shows the stability factor over frequency.

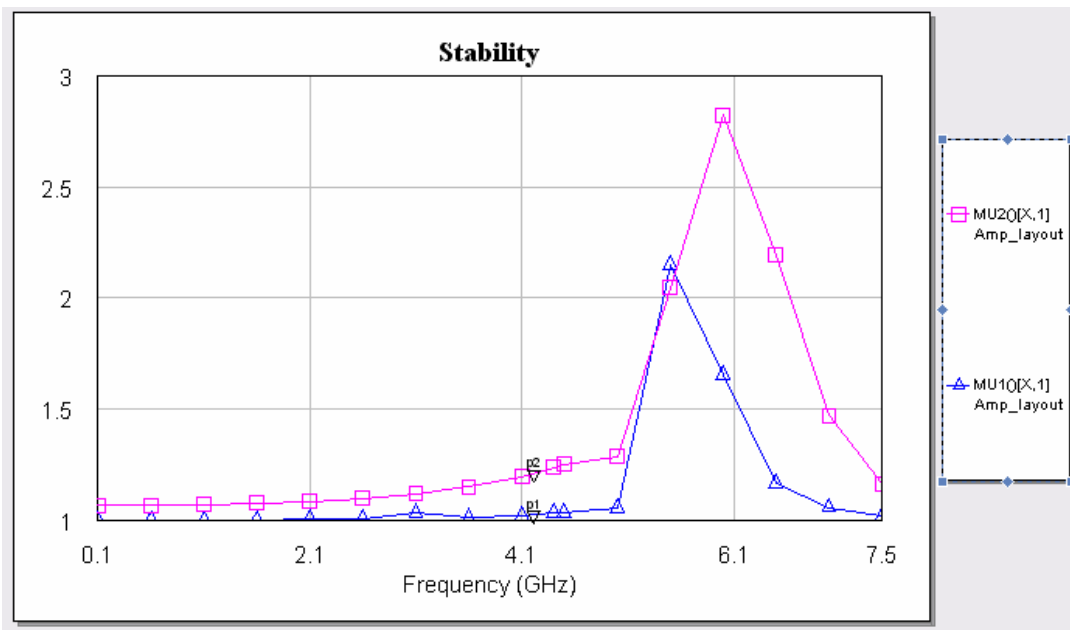


Figure 5.-Stability factor for the final design

Figures 6 and 7 shows the combined amplifiers performance after the layout was finalized. Figure 6 shows the amplifiers power output, PAE and power gain as the input power is increased at the center frequency of 5.5 GHz.

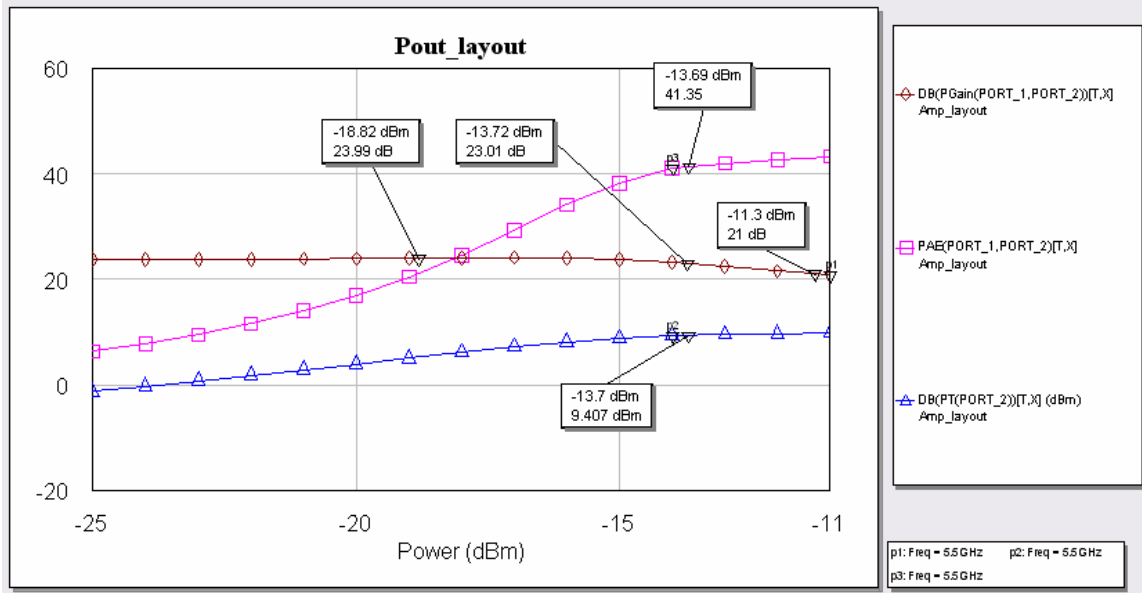


Figure 6 – Pout, PAE and Gain vs. Pin

Figure 7 shows a power sweep with a fixed Pin. When driven properly 38% PAE is achieved as is a Pout greater then 9 dBm with 20 dB of gain from 5.3 GHz to 5.7 GHz.

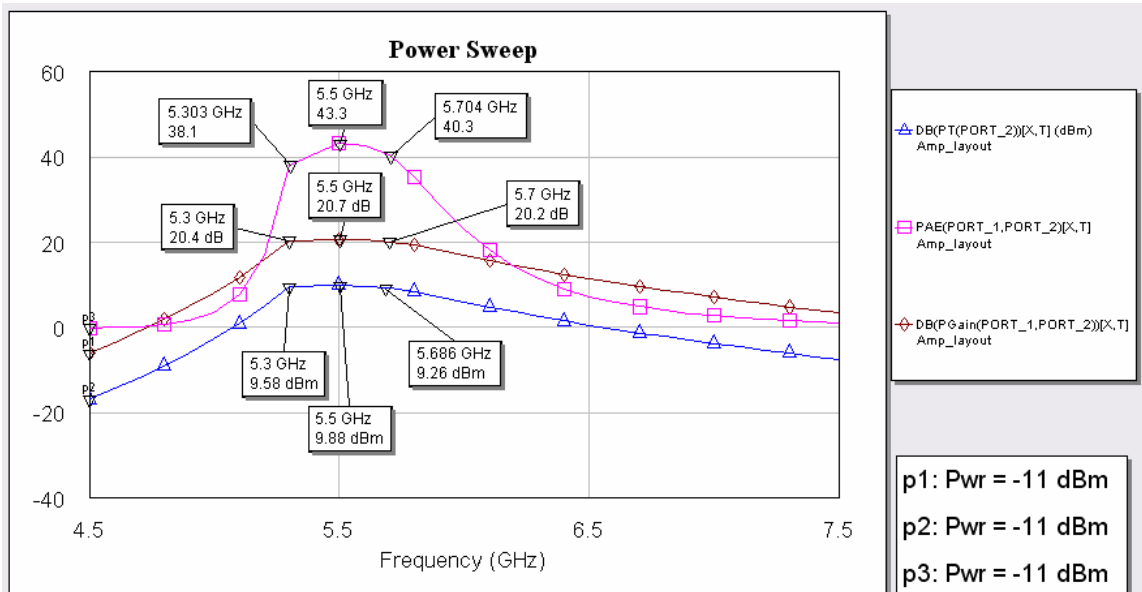


Figure 7 – Pout vs. Frequency

The simplified schematic is presented below in figure 8. The simulated data presented here used AWR’s transmission line models on the Triquint substrate that have been removed for clarity, see Appendix A for the full schematic. From left to right are the amplifier’s input matching network, driver stage, interstage matching network, final stage, and the output matching network. The bias network runs along the bottom of the amplifier.

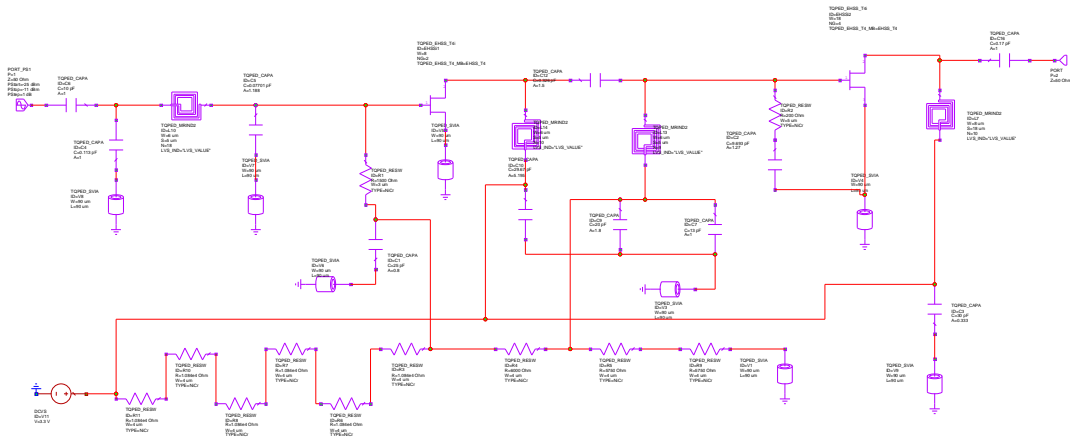


Figure 8 – Amplifier Schematic

The layout is shown in figure 9. The input is at the bottom of the chip and the output is at the top. The RF ports use ground-signal-ground ports for maximum RF performance. To the left are the supplementary gate bias ports. On the right hand side is the main power pin and a supplemental ground pin as well. Layout successfully passed ICED design rule check before submission to Triquint.

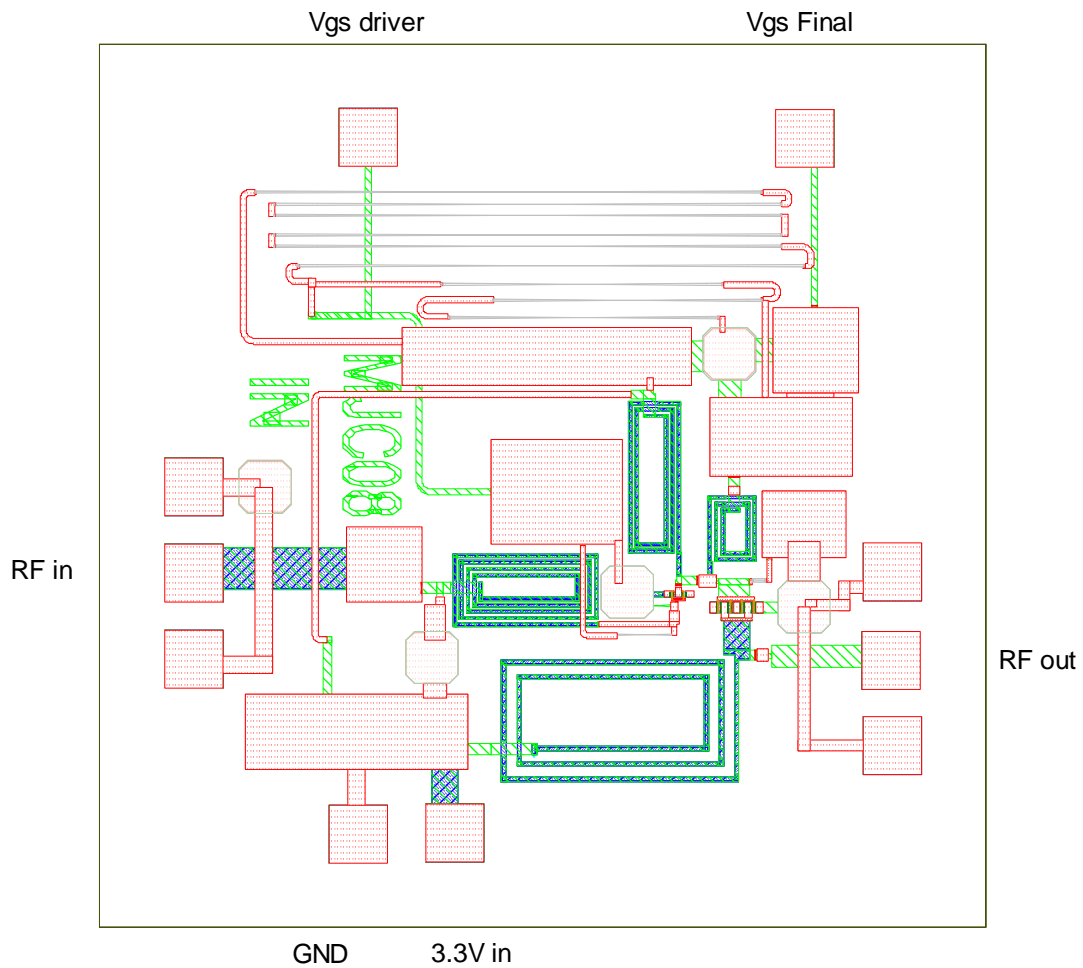


Figure 9 – Amplifier MMIC Layout

Test Plan

Test equipment needed:

1. Agilent 8510 Network Analyzer (or equivalent)
2. Agilent E3632A power supply (or equivalent)
3. Agilent 34410A DMM (or equivalent)
4. Agilent 8683B signal generator (or equivalent)
5. Agilent E4416A power meter (or equivalent)
6. Agilent 8480 Power sensor (or equivalent)

The Amplifier should be connected to a 3.3 V power supply which has been current limited to 20 mA. As the design consists of PHEMTs and contains internal bias circuitry there is not the concern of damaging the devices if there is not gate bias applied before the drain bias.

Test procedure:

1. With no RF source applied, power on DUT power pin with 3.3V and record quiescent current:
 _____ mA (approximately 3 mA)
2. Set logic analyzer so that Pout < -20 dBm and frequency from 2.5 GHz to 7.5 GHz. Record the small signal gain and the small signal S11 and S22.
 _____ S11
 _____ S22
 _____ S21

This will verify the general health of the amplifier as well as check that the design is centered at 5.5 GHz

3. Set the signal generator for -20 and 5.3 GHz and perform the following measurements (Grayed cells are calculated parameters.)

Pin = -20 dBm			
Frequency	Pout	Gain	Current
GHz	dBm	dB	mA
5.3			
5.5			
5.7			

1 dB compression Measurements						
Frequency	Pin at P1dB	P1dB	Gain @ P1	Current	Pconsumption	PAE
GHz	dBm	dBm	dB	mA	mW	%
5.3						
5.5						
5.7						

3 dB compression Measurements						
Frequency	Pin at P3dB	P3dB	Gain @ P3	Current	Pconsumption	PAE
GHz	dBm	dBm	dB	mA	mW	%
5.3						
5.5						
5.7						

Table 3. - Tabulated Data

Conclusions

A C-Band power amplifier was designed that achieves greater than 38% efficiency and 9 dBm out with 20 dB of gain across 400 MHz of bandwidth. All design specifications were achieved. Due to the design tradeoffs to maximize efficiency not all of the design goals were achieved, a summary of the simulated performance is given in table 4.

	Spec	Goal	Simulated	Measured
BW:	5.3 Ghz-5.7GHz			
Pout:	9 dBm	10 dBm		
PAE:	>40%at fc	40% across the bandwidth		
Gain Ripple:	+/- 0.5	+/- 0.5		

Table 4. - Specs, goals, and worst case measured parameters

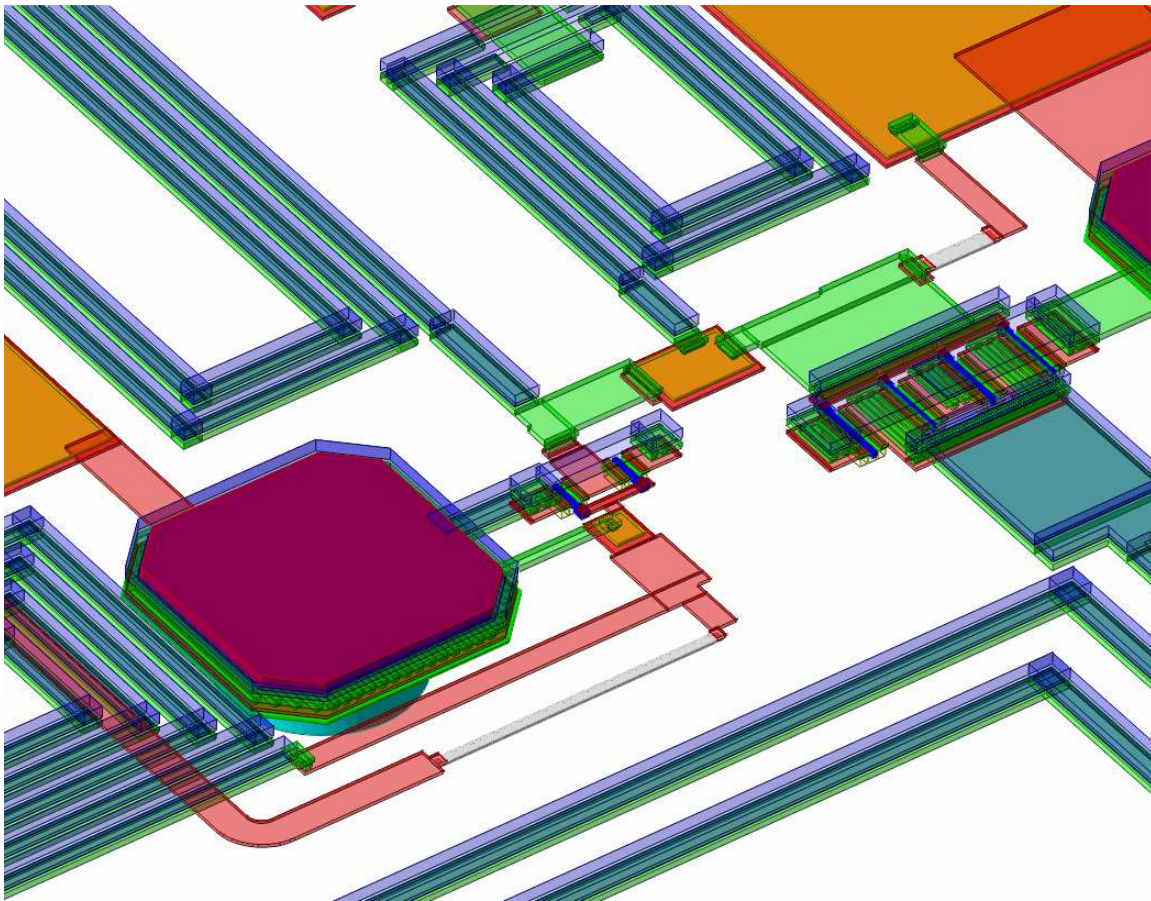
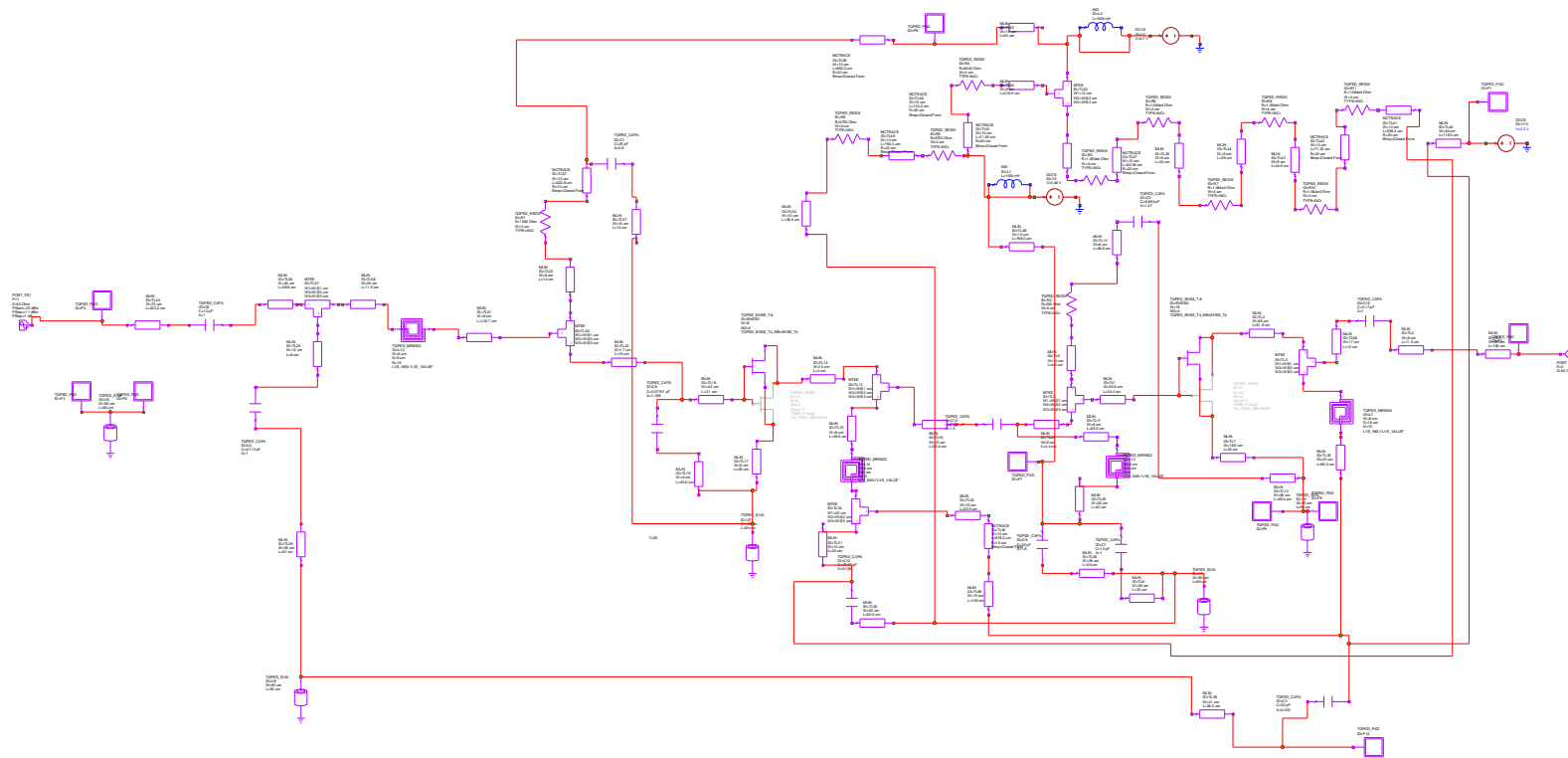


Figure 10. – close up of the transistors

APENDIX A – Schematic Views

Full Schematic



Simplified Schematic

