2.4 GHz LNA Project

525.787 MMIC Design

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Abstract

This paper describes the design and simulated results of a low noise amplifier (LNA). The LNA is to operate at 2.4 GHz and will be fabricated on Triquint's TQPED pHEMT (pseudomorphic high electron mobility transistor) process. The main design goal was to design the amplifier to have a noise figure as close as possible to the optimum noise figure, NF_{opt}, given from the scattering parameters (S-Parameters) for the process from Triquint. The design utilized inductive source degeneration in order to allow simultaneous optimization of noise figure and input return loss. The design has 10 dB of gain with a NF of < 0.9 dB with excellent match on input and output (S11 and S22 are approximately -20 dB). Input P-1 dB compression is approximately -4 dBm.

Introduction

The design was targeted to be the first stage of gain in a receive chain, biased with a single (positive) power supply that would enable battery operation. Bias was chosen as +3V with current draw of 15 mA. Triquint's TQPED process allows enhancement mode and depletion mode pHEMTs , the design requirement of a single power supply is more easily met with an enhancement mode pHEMT. It was also convenient that NF_{opt} for the enhancement mode at 2.4 GHz occurred at a source impedance nearer to 50 ohms than for the depletion mode. A common-source, enhancement-mode pHEMT was therefore the chosen topology.

A gain of approximately 10 dB was chosen for two reasons. In order to properly "set" the noise figure of the chain, at least 10 dB of gain from a first-stage LNA is desired. But if this is to be the first stage of a two-stage LNA (total gain likely ~ 20 dB), it is desirable for the gain of the first stage to be only moderately high in order to prevent the first stage from becoming the dynamic range limiting element – allowing the second stage to also be approximately 10 dB but with higher bias and compression point. The gain of the process is much higher than 10 dB at the design frequency of 2.4 GHz, so feedback was employed to reduce the gain. Resistive feedback would raise the noise figure, so reactive feedback, in the form of an inductor from source to ground, was employed.

The NF_{opt} of the process at a bias similar to the designed LNA was approximately 0.5 dB; the goal, therefore, was to degrade this as little as possible, with an expectation that a final NF of < 1.0 dB would be attainable. In order to minimize noise figure degradation, efforts were made to minimize the need for components on the input side of the amplifier. All stabilization was done on the output of the LNA, and the input matching topology was chosen to allow the matching inductor to be the path for the gate bias. Ultimately, the finite quality factor (Q) of the input matching inductor was the single largest contributor to noise figure, with the source-to-ground feedback inductor being the only other contributor of significance.

Design Approach

The design of the LNA began with the noise parameters included in the S-Parameter file for the TQPED process. The IDSS/4 file was biased at +3.0V/19mA, a similar bias to the design.

RAW	NOISE	DATA		
Freq	FMIN	GAMMA	OPT	Rn
GHz	dB	Mag	Ang	(NORMALIZED)
1	0.42	0.609	6.676	0.155
2	0.43	0.5298	28.683	0.129
*2.4	0.482	0.50572	35.3646	0.1278
3	0.56	0.4696	45.387	0.126
4	0.66	0.4258	60.019	0.125

* 2.4 GHz row is interpolated

The table above set the design goal of the NF – specifically, to degrade this 0.48 dB number as little as possible. A realistic spec is that the noise figure will be < 1.0 dB once non-idealities are introduced, with a goal of < 0.8 dB.

The output match on an LNA should be excellent, as there is no NF penalty for matching into any arbitrary load and optimizing the output match simultaneously gives the maximum gain for a given input match. Correspondingly, a specification of a return loss of at least 15 dB is set, with a goal of 20 dB.

The input match on an LNA, however, does come with a tradeoff. Highest gain occurs when the input impedance of the amplifier matches the characteristic impedance of the system (typically 50 ohms), so the ideal input impedance for highest gain would be 50+j0 and the input matching network would be designed accordingly and would be from the perspective "looking into" the amplifier (S11). However, this matching network transforms the driving source impedance (assumed to be 50 + j0) into a load presented to the input of the transistor, and it is this input loading which determines the noise figure of the amplifier. It is only when the input matching network presents 50 ohms as the Z_{opt} for the transistor that NF_{opt} is attained.

It would be simply fortuitous if the matching network which optimizes S11 simultaneously presented a source impedance of 50 ohms to be the ideal source impedance for optimal noise figure. To an extent, there can be significant forgiveness for an imperfect S11; gain can always be increased with additional stages later, and passband ripple due to input reflections may not be an issue, especially in narrowband systems. A spec of S11 < -10 dB is viewed as acceptable, and there is little effect on the overall gain at this point. However, with the use of source degeneration feedback, a goal of S11 < -15 dB is pursued, again bounded by the governing goal of minimization of noise figure degradation.

Similarly, the stability of the transistor is a parameter which does come with a tradeoff, although the significance of the tradeoff ultimately depends on the design. If, for example, resistive stabilization was required on the input that could not be bypassed at the operational frequency, the noise figure will be strongly impacted by the need to stabilize the device. If, however, the stabilization can occur at the output, only the gain and output intercept points are affected and, assuming there is still decent overall gain even with the stabilization resistor, the effect on the noise figure is small. This was the design goal for this LNA – that all stabilization occurs on the output.

The power supply requirement is single supply, +3V operation. It is likely that the design, if battery powered, might be exposed to +2.7V to +3.6V, so the design would ideally work well across this battery range. With a simple passive biasing scheme, the device current will vary with the power supply, but the overall specifications – especially gain and noise figure, should not vary significantly.

Input power compression is a specification driven by the gain of the device and the DC power budget. With approximately 45 mW of DC power consumption, even a 10% drain efficiency would produce an output power of 4.5 mW (+6.5 dBm). Referred to the input, with a gain of approximately 10 dB, an input P-1 dB of -3.5 dBm should be achievable, unless there is significant loss due to resistive stabilization (or unless the gain is actually higher than 10 dB).

The design should work from 2.3 to 2.5 GHz, and there is little tradeoff required to meet this specification. The matching networks are wideband enough to provide nearly identical performance across the entire band.

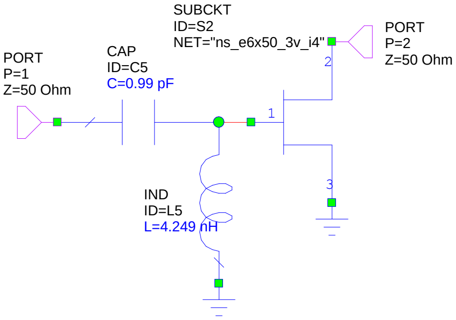
The sizing of the pHEMT would normally be a parameter available to the designer, but in this case, the 6x50 um device was chosen to match the device for which noise parameter data was given. This device size seemed to be well matched for the application and was not viewed as a significant tradeoff.

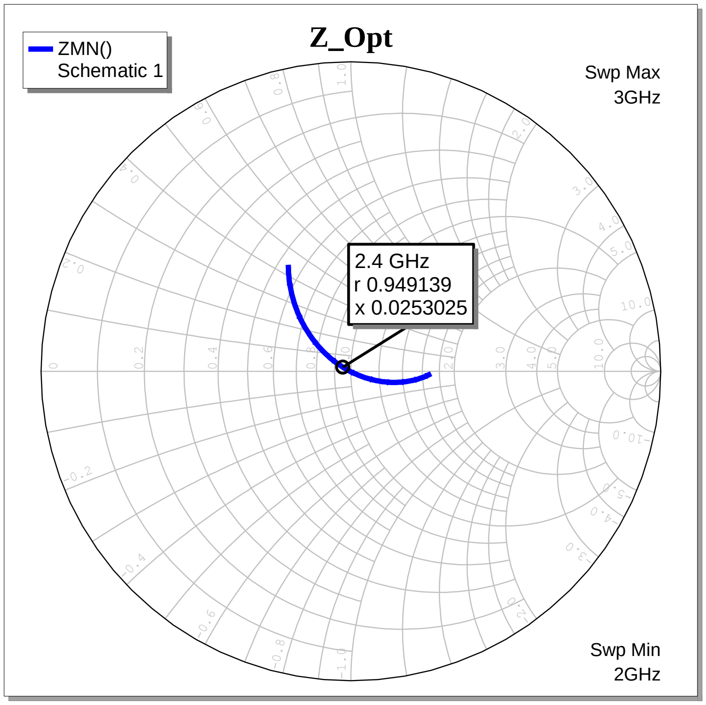
Given the analysis above, the following table reflects the specifications and goals of the design.

Parameter	**Specification**	**Goal**
Operating Frequency	2.3 to 2.5 GHz	2.3 to 2.5 GHz, same specs
Gain, S21	10 dB < Gain < 12 dB	Same
Gain Variation (Ripple)	< 1.0 dB	< 0.5 dB
NF	NF < 1.0 dB	NF < 0.8 dB
S11	< -10 dB	< -15 dB
S22	< -15 dB	< -20 dB
Power Supply Requirements	Single Supply, +3.0V	+3.0V to +3.6V operation
Power consumption	< 50 mW	Same
Input P-1 dB	-3.5 dBm	Same
Output P-1 dB	+6.5 dBm	Same
Stability	“Stable” – no obvious issues, especially near operating frequency	Unconditionally Stable, entire frequency range

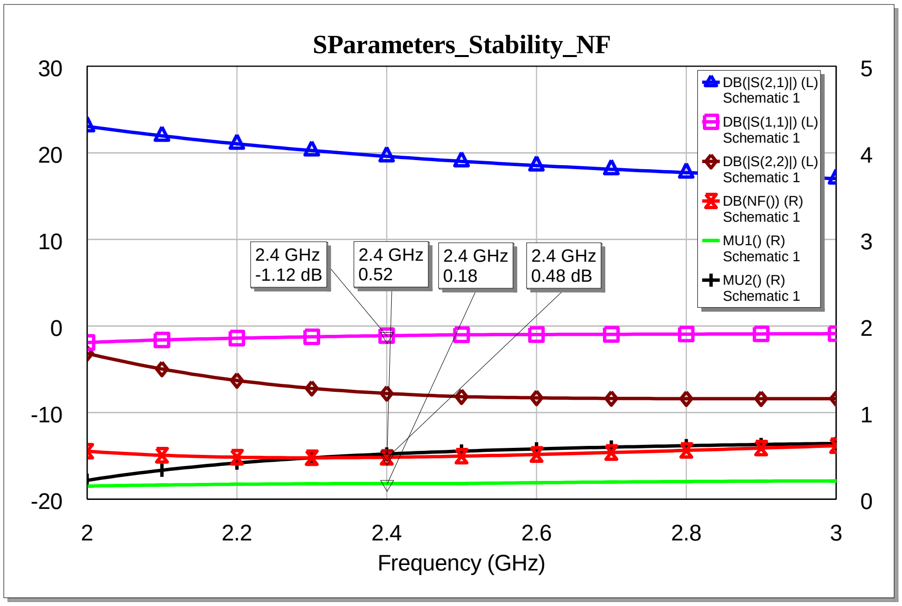
Because the stabilization of the device and the input match are the two specifications that do potentially come with a tradeoff, a quick analysis of these aspects of the design are included in more detail – specifically, how the source inductor helps the design.

Below is a simple two-element matching network which provides Z_{opt}, the source impedance which provides minimum noise figure. There are two such networks, but the one used is the highpass topology because it allows feeding in the bias through the shunt inductor. The simulated noise figure is 0.48 dB, which matches the NF_{opt} attained from the S-Parameter file, and is demonstrated with the plot of Z_{opt} showing that with the input matching network, optimal noise figure is achieved with a source impedance of 50 ohms.

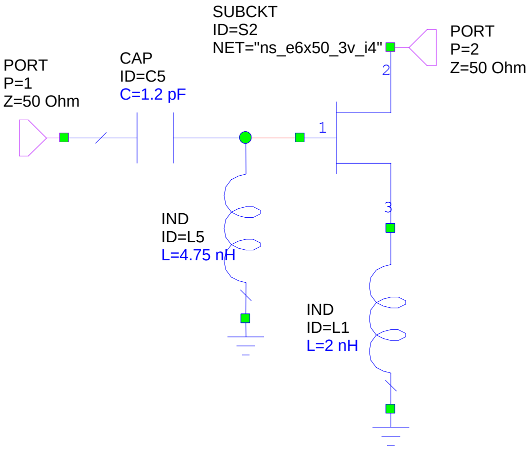


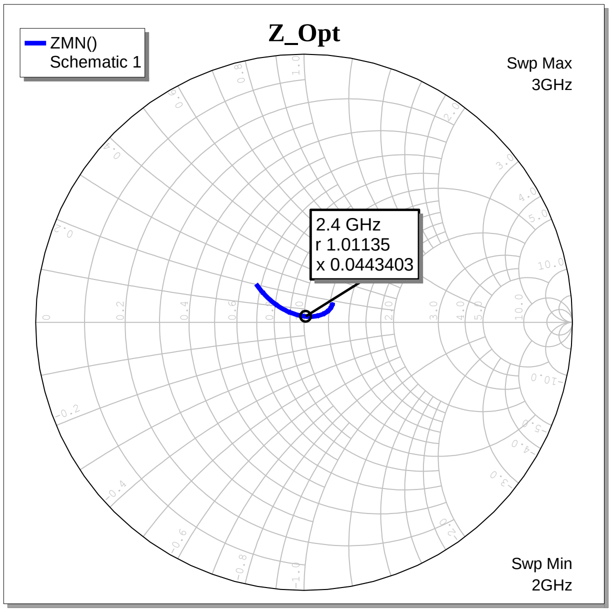


While noise figure is a priority, this input matching network is not a good starting point for the design. As shown in the following plot, the design is highly unstable, with MU1 and MU2 much less than 1.0, and S11 is an atrocious -1.1 dB. Even if the output could be stabilized with resistors, the input return loss will still be poor.



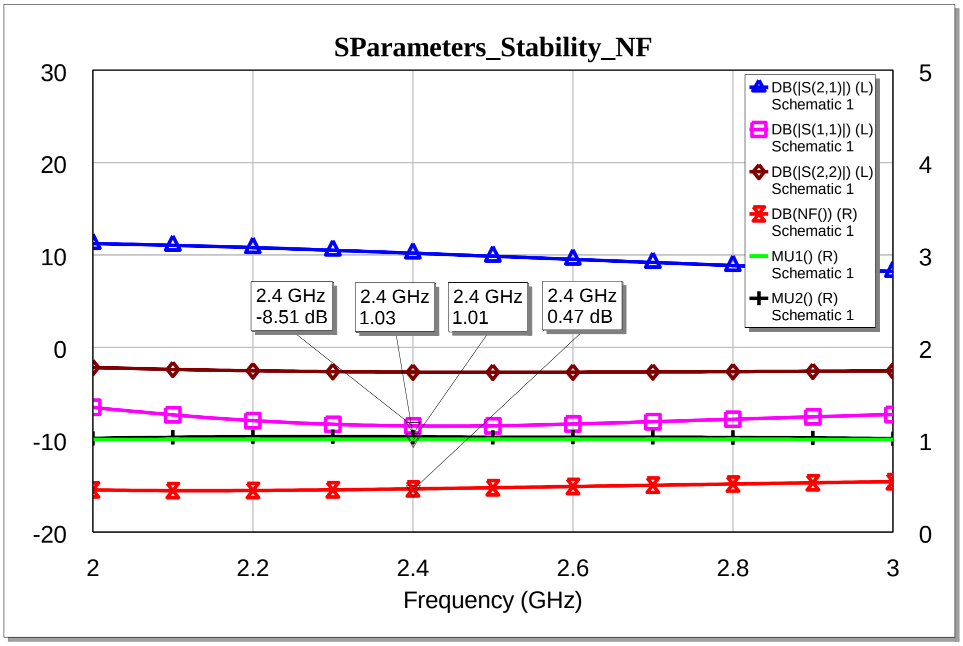
However, the addition of an (ideal) inductor from source to ground significantly improves the stability and input return loss of the amplifier without degradation to the noise figure. Below is the schematic with the addition of the source inductor. Note that the source inductor does slightly affect Z_{opt}, so the component values in the input matching network have been adjusted to re-center Z_{opt} at 50 ohms.





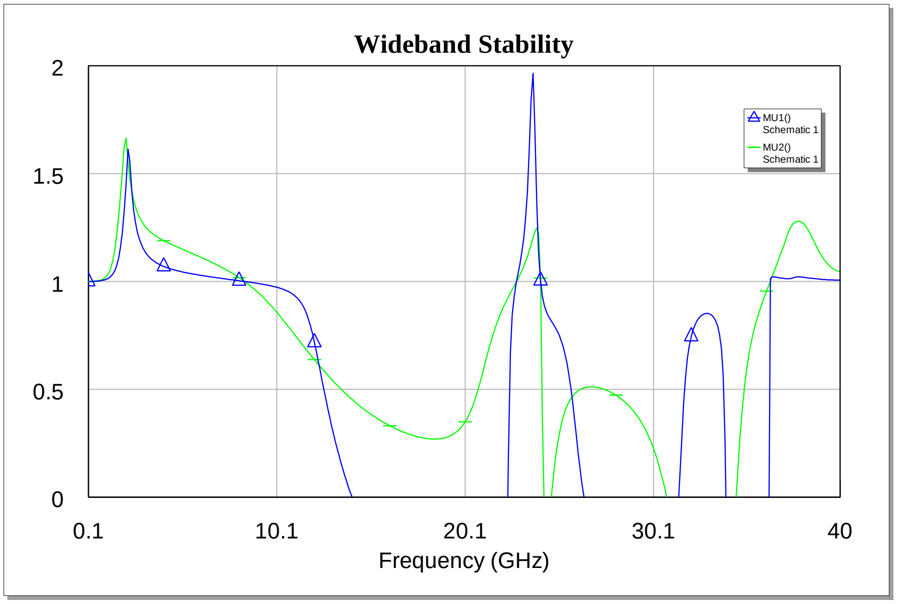
The 2 nH inductor has a significant effect on the overall design of the amplifier. MU1 and MU2 are now above 1.0 and the input return loss is greatly improved, with an S11 of -8.5 dB. As expected from the Zopt plot above, the noise figure remained at NF_{opt} of ~ 0.48 dB. Note that the gain is significantly reduced, which would be expected from feedback, but it is likely that a total LNA gain of 20+ dB would have required two stages of gain so lower gain is not only acceptable but desirable.

This demonstrates the value of the source inductor as a starting point for the design. Since the (ideal) inductive feedback has no resistance, there is no degradation in the noise figure and it relocates Z_{opt} to an S11-friendly portion of the Smith chart.

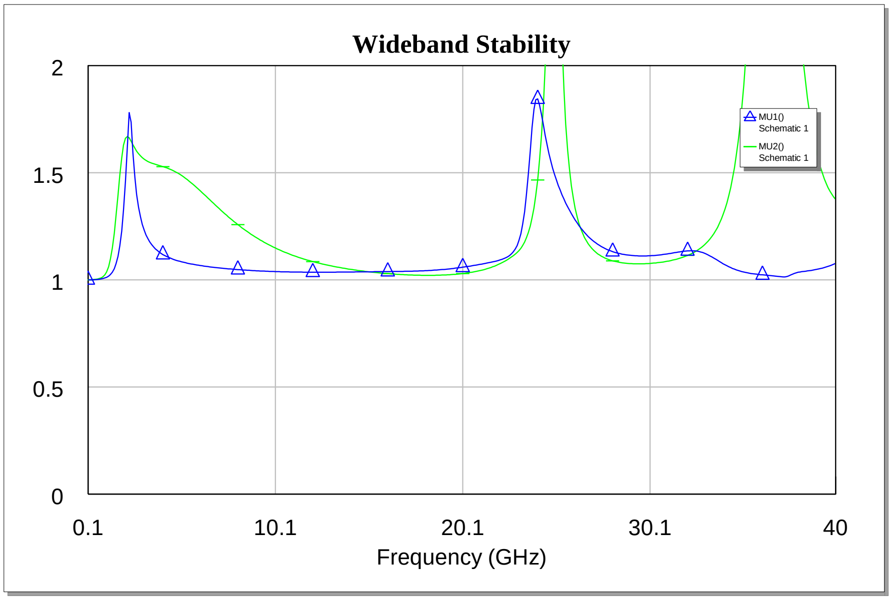


Simulations

The source inductor and ideal matching network served as the starting point for the design. While the source inductor stabilized the amplifier in the operating frequency range, the actual design with layout had a strong potential instability at high frequency (above 10 GHz).



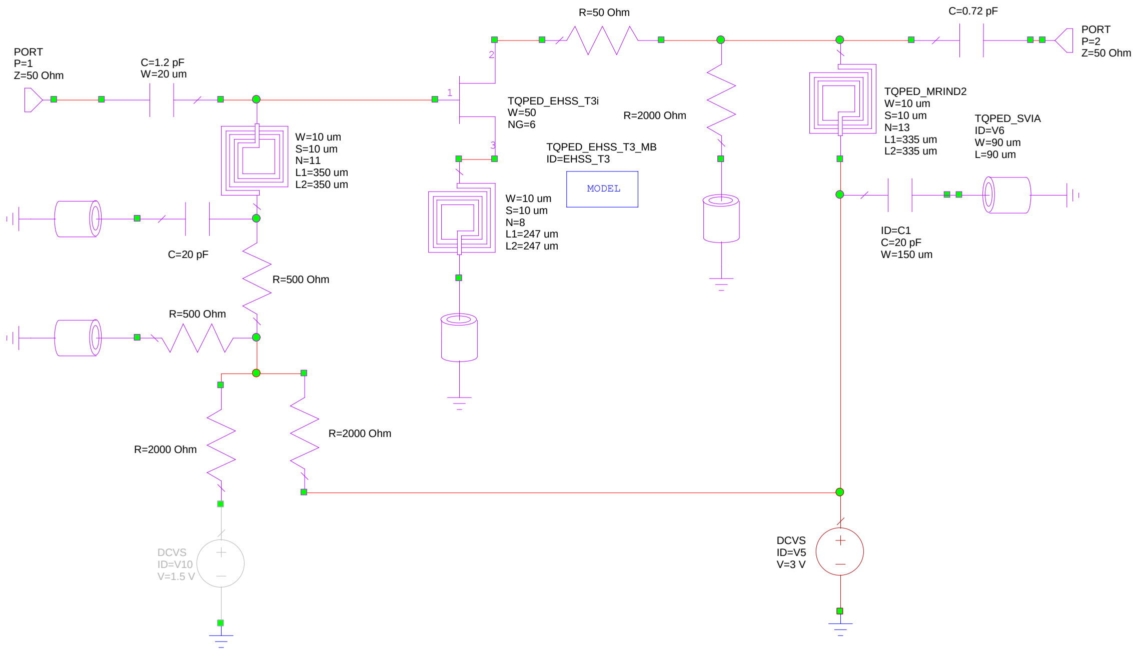
The addition of a series 50 ohm resistor followed by a shunt 2000 ohm resistor on the output solved this potential problem and achieved unconditional stability but did degrade the noise figure by approximately 0.07 dB (even though stabilization was all on the output).



Changing to actual Triquint TQPED spiral inductors degraded the noise figure, as expected. The source inductor was not a significant contributor (0.02 dB), and the input matching inductor was the dominant noise source, raising the noise figure by 0.2 dB. This brought the noise figure up to approximately 0.48 + 0.07 (stabilization) + 0.02 (actual source inductor) + 0.2 dB (actual input matching inductor) = 0.77 dB

This would have had an input return loss of approximately -10 dB, which would have likely been acceptable. However, subsequent tweaking found that at a relatively minor cost to noise figure, significantly better input return loss was achievable. Allowing another 0.05 dB of degradation allowed S11 to be < -17 dB; this tradeoff for better input return loss was made in the final design.

Below is the final schematic. Note that the input and output matching networks are highpass topologies, allowing the shunt inductor to feed in the bias (with a large 20pF capacitor to RF ground the shunt inductors). No attempt was made at bypassing (either at DC or at 2.4 GHz) the resistors was used for high-frequency stabilization on the output. This does come at a cost.

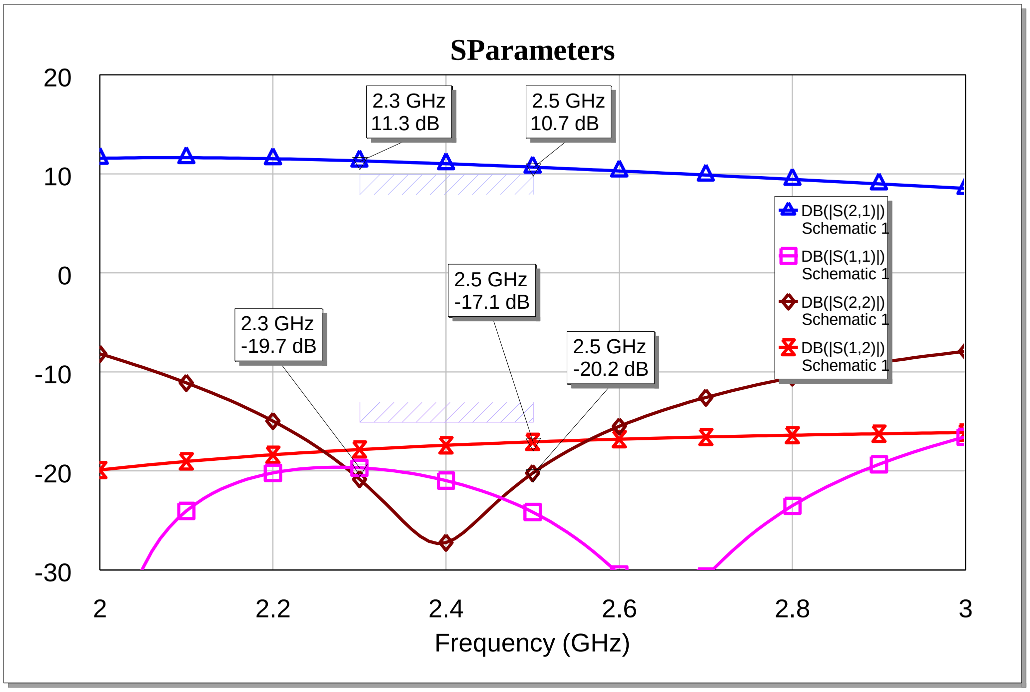


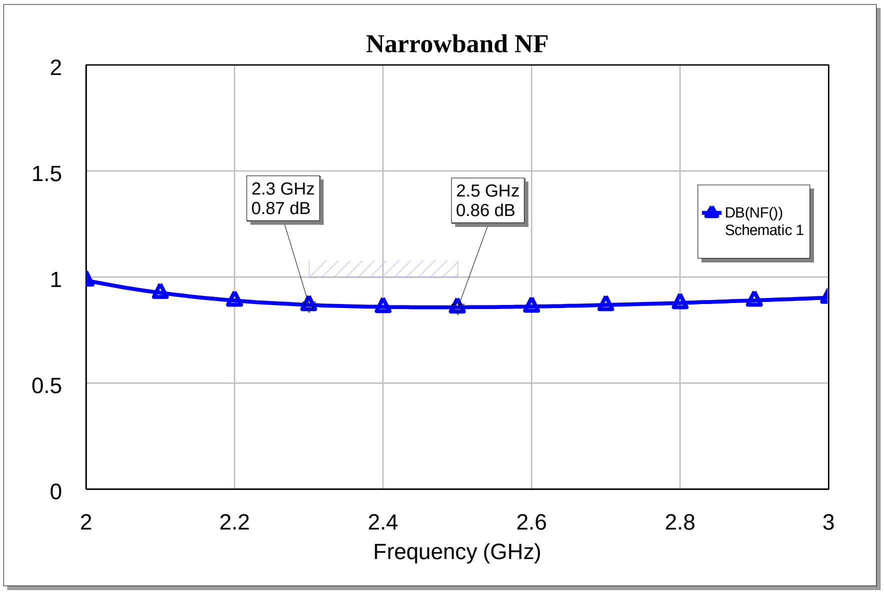
For DC power consumption, at 15 mA bias, the voltage drop across the 50 ohm resistor is 0.75V and the resistor consumes 11 mW. Similarly, the current draw through the 2000 ohm shunt resistor is 1.5 mA and the resistor consumes 4.5mW. This power consumption is unnecessary and could be eliminated. A capacitor in series with the 2000 ohm resistor would eliminate its power consumption, and an inductor in parallel with the 50 ohm resistor would eliminate its.

For RF, the 50 ohms is effectively in series with the output load. However, the output matching network presents the output 50 ohm load as approximately 200 ohms with impedance transformation, so the impact of the series 50 ohms is not as significant as it might initially appear, but simulation showed that there was a cost of approximately 1.5 dB of gain. This would also subtract from the output compression and intercept points of the device.

An attempt was made to bypass the 50 ohm resistor but the resonance of the bypass inductor adversely affected the high-frequency stability, defeating the original point of the 50 ohm resistor. So the inefficiency was accepted, and as an ancillary benefit, the 50 ohm resistor does serve to deliver a more constant current as a function of active device variation.

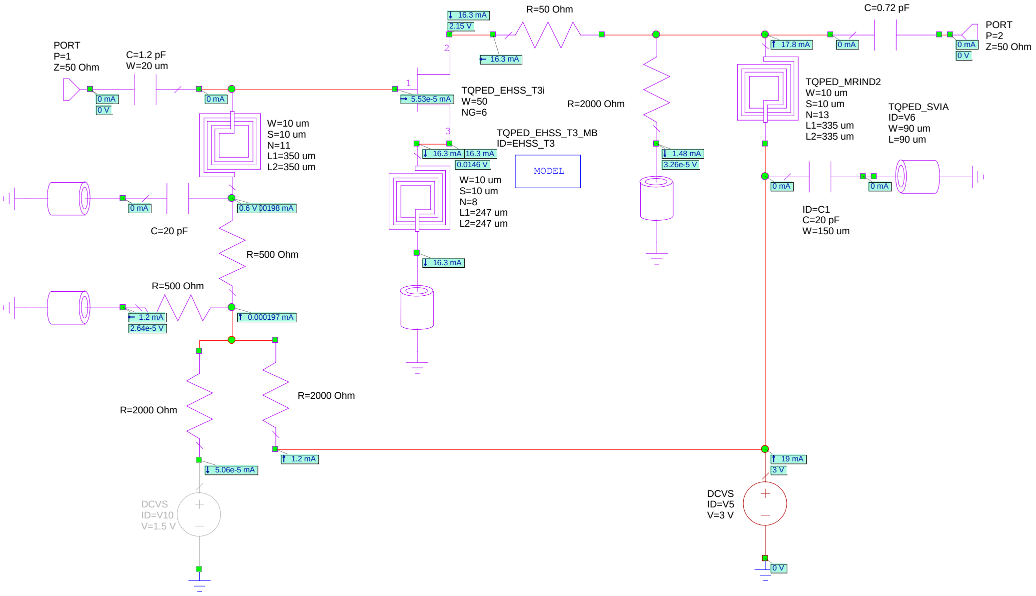
The final S-Parameters, after extracting the actual layout and tweaking the components to absorb the effects of the layout, are reflected in the following plot. Gain was 10.7 to 11.3 dB over the 2.3 to 2.5 GHz passband. Input and output return losses were ~ 20 dB and the reverse isolation was ~ 17 dB.   Noise figure was 0.87 dB after all final tweaking – a degradation of approximately 0.4 dB from NF_{opt}.

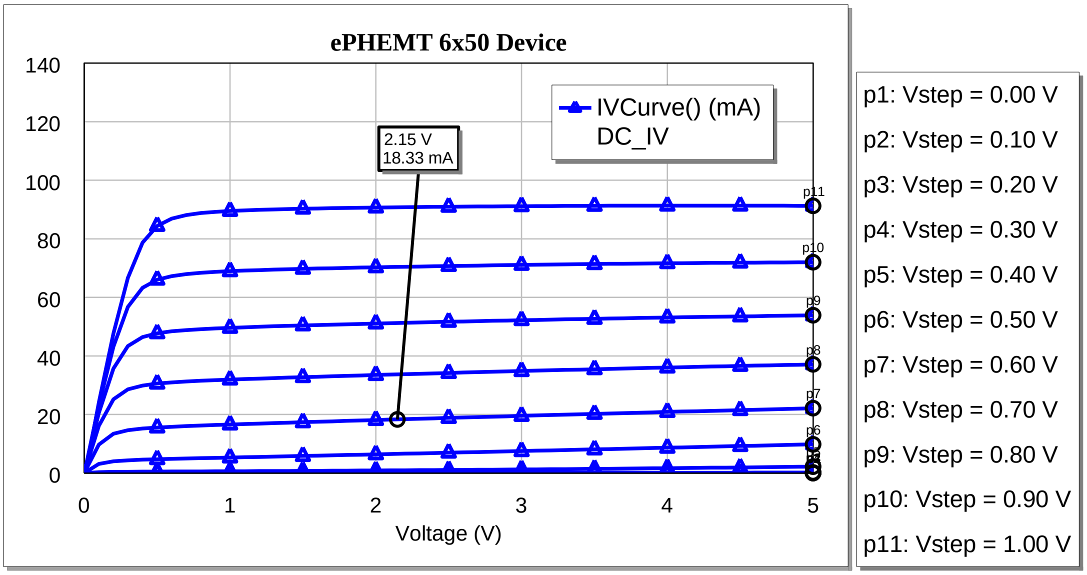




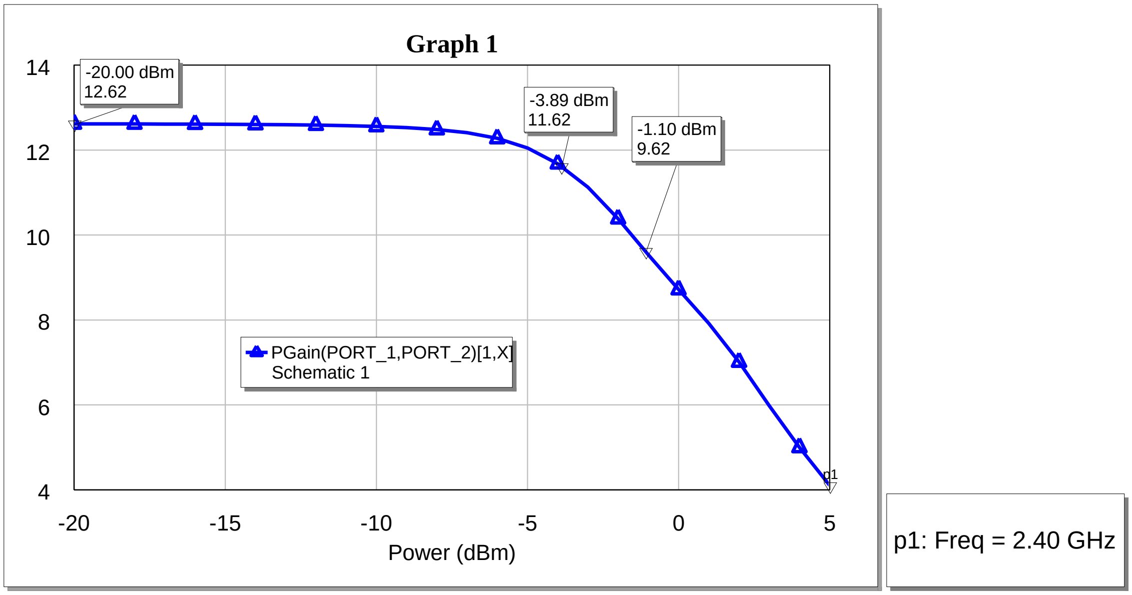
Bias was +3V / 19 mA, of which 16 mA was into the device. As already mentioned previously, 1.5 mA went into the output stabilization shunt resistor, and there was another 1.2 mA on the gate bias. A low frequency termination provided increased *low* frequency stabilization (f < 10 MHz), so some extra current was consumed in providing that low frequency path.

V_{ds}, with Vcc of +3V, is +2.15V and the gate is biased at 0.6V with a simple resistive voltage divider. An extra gate voltage was exposed in order to tweak the bias in order to account for the actual fabricated device which may draw more or less current at V_{gs} = 0.6V. An I-V curve is included showing the bias point is as expected (Vgs=0.6V and Vds=2.15V predicted ~ 18mA).



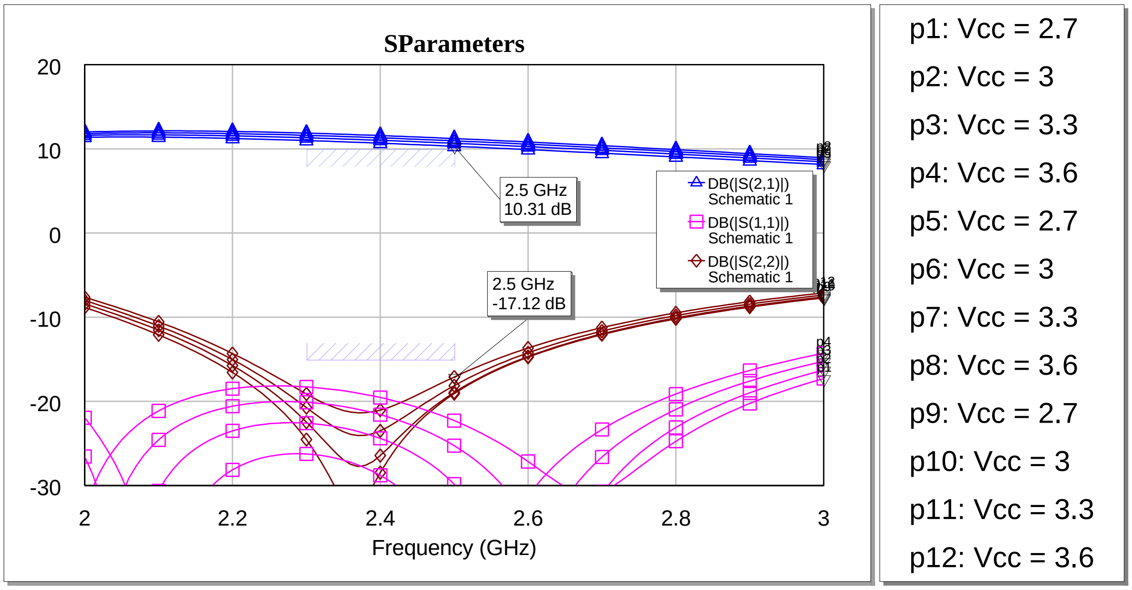


A power sweep was performed at 2.4 GHz to find P-1 dB. [Note: the small signal gain when driven from a power sweep source was 12.6 dB whereas the S-Parameter gain from a linear port was only 11 dB, and this discrepancy was never understood.] Using the 12.6 dB gain as the reference, P-1 dB occurred with an input of -3.9 dBm (output P-1 dB of +7.7 dBm). As a reference point, P-3 dB occurred at an input of -1.1 dBm (output of +8.5 dBm), showing that there is not much more output power to be had beyond P-1 dB (an extra 2 dB of drive only increased the output power by 0.8 dB).

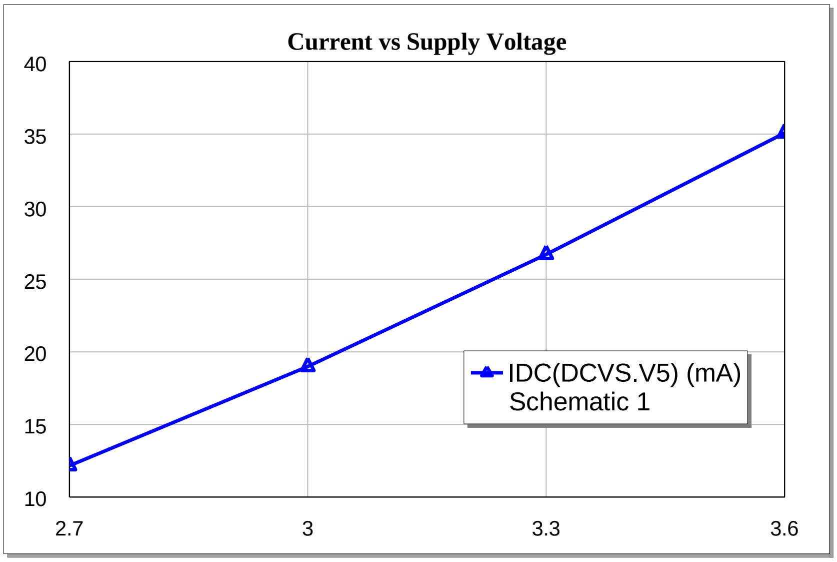


Simulations vs. Variations

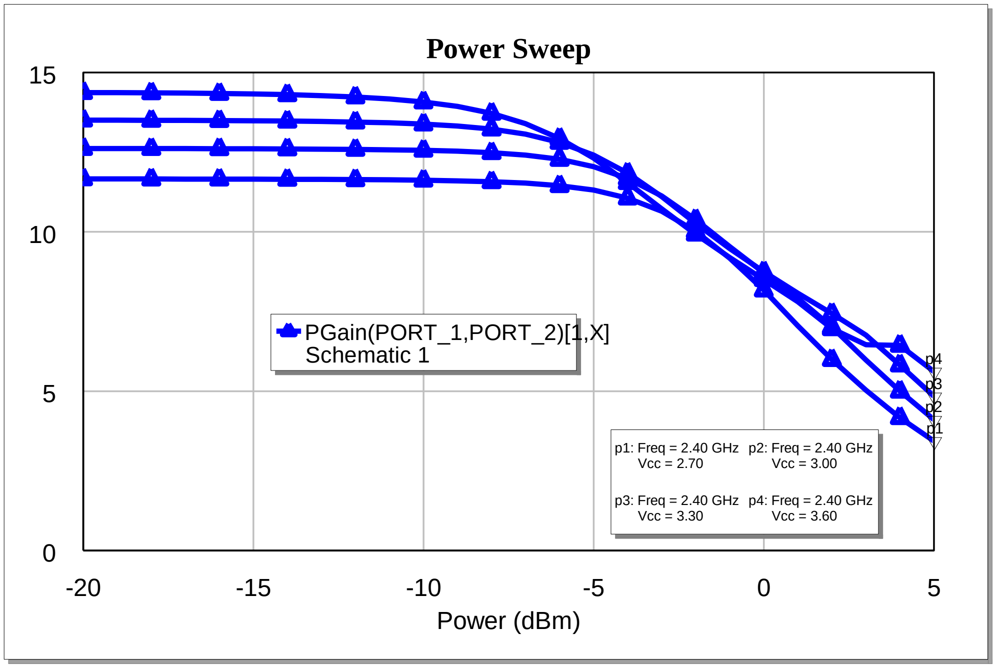
The design was tested against power supply variation from 2.7V to 3.6V. There was little variation in the S-Parameters, with the minimum gain only reducing to 10.3 dB and the worst return loss was 17 dB.



There was significant variation in the supply current as a function of supply voltage. This was expected, as the bias was a simple passive bias, a resistive divider of the supply voltage. The current varied from 12 mA to 35 mA for bias of +2.7V to 3.6V, respectively.

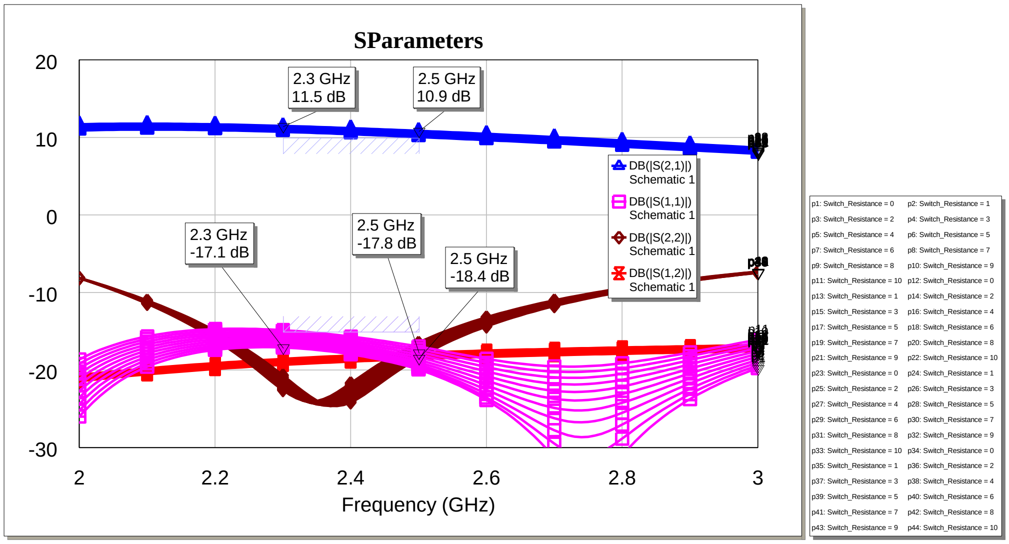


As mentioned earlier, there is a discrepancy between the gain when the source is a power sweep port instead of a linear sweep port, so the P-1 dB comparison as a function of power supply is not viewed as reliable. The power sweep showed the small-signal gain being as high as 14 dB, whereas the linear sweep gain was only as high as 11.8 dB.

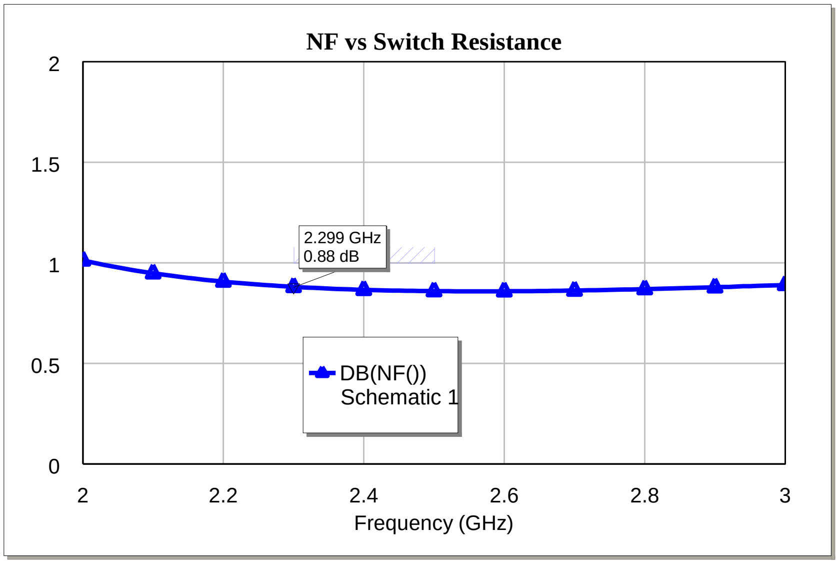


The design was simulated against variations in the source impedance. Specifically, it is likely that the LNA could be preceded by a transmit/receive FET switch with an ON resistance of a few ohms. A series resistance was swept from 0 to 10 ohms to model this effect.

Neither the S-Parameters nor the noise figure varied significantly. Gain stayed around 10 dB and the return losses were still > 15 dB each, so no redesign would be necessary to account for the increased source impedance presented by the preceding switch's ON resistance in series with the original source impedance of 50 ohms, although S11 could be improved slightly if desired.



Noise figure was virtually unaffected. While a series 10 ohm resistor certainly degrades the noise figure, the noise figure of the amplifier itself was not changed with the increased source impedance. Below is the LNA with a source impedance of 60 ohms; NF increased only 0.01 dB.

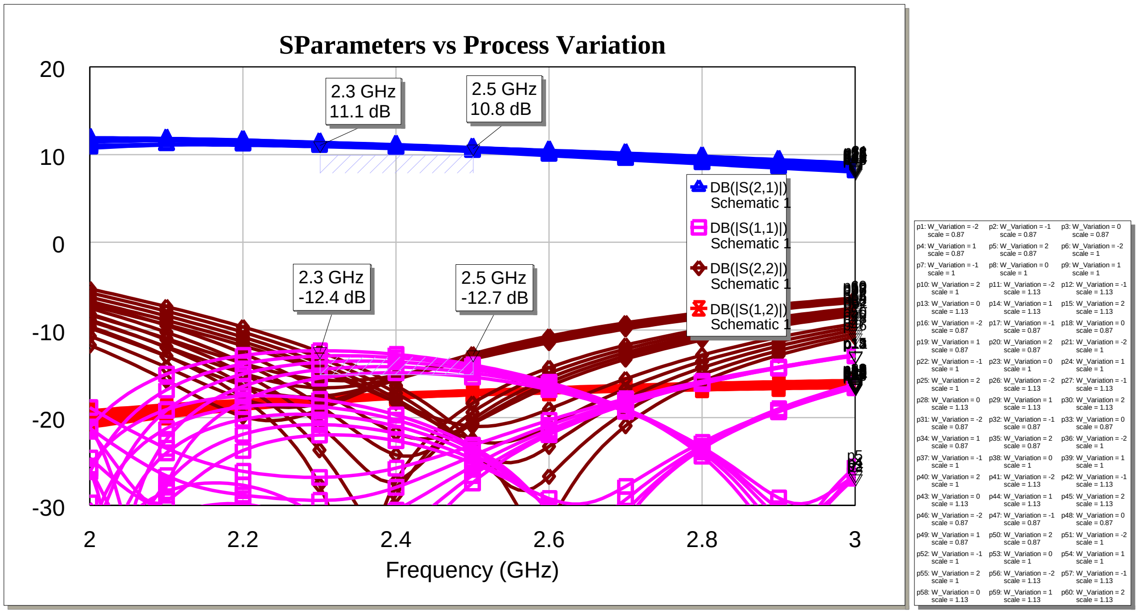


An attempt was made at simulating the process as a function of process variation. The width of the inductors and capacitors was set to be +/- 2 um from the nominal design and the S-Parameters were swept to reflect this variation.

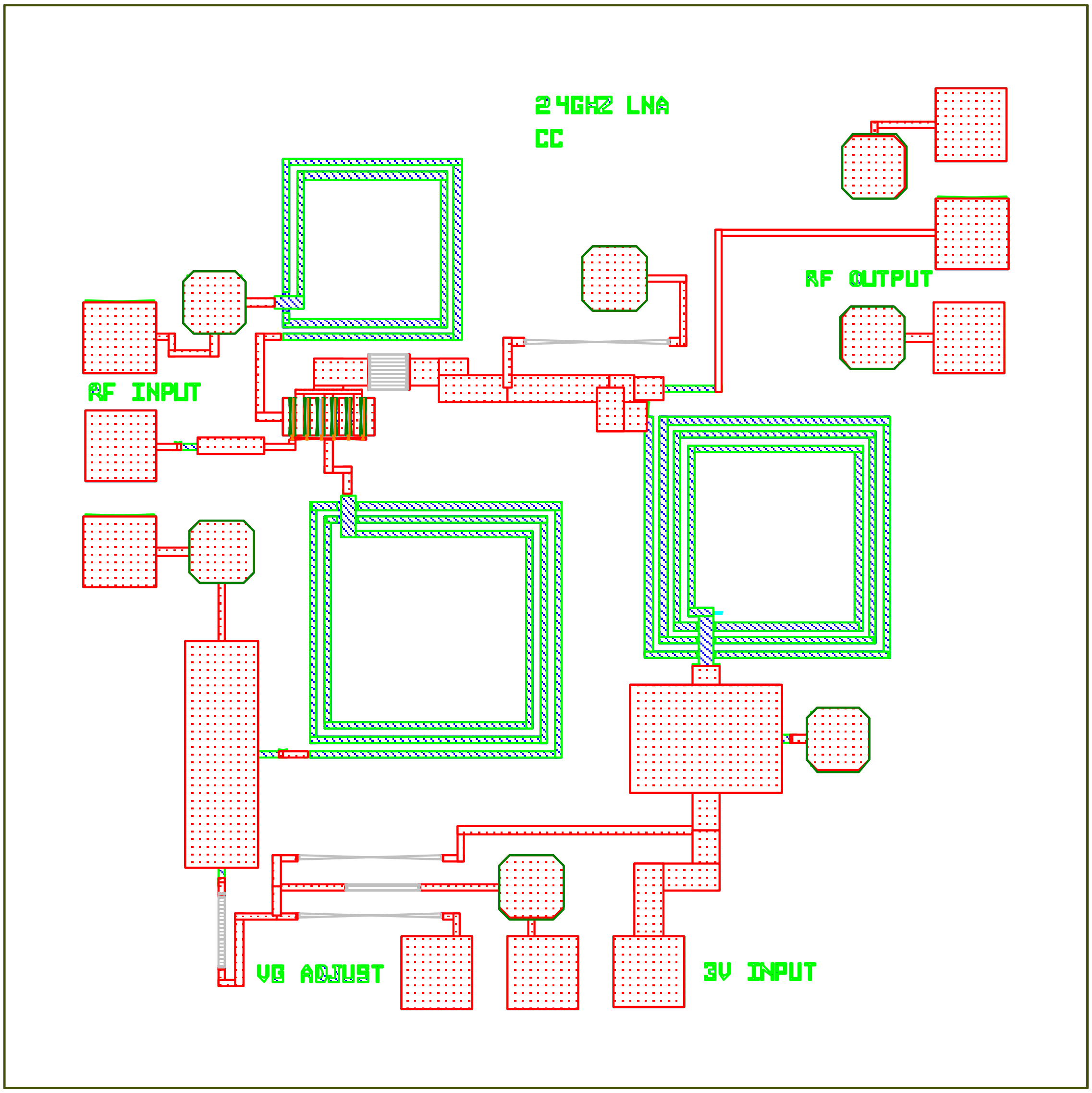
The choice of +/- 2 um was somewhat arbitrary, although it was based on the logic that if a feature size of 5 um was allowed, the tolerance could not be as bad as 5 um, and 2 um represented a significant variation as a percentage of an allowable feature size. The variations were assumed to be in the same direction for all components - either all increased or all increased by the same amount (and the validity of this assumption is not known). The resistors were not varied because there was little dependence on their actual values other than for bias (and the variation in bias due to resistor tolerance would be small compared to the significant variation which would occur for the +2.7V to +3.6V power supply variation, and the bias will be adjusted as necessary with the “Vg Adjust” pin).

Inductance values are mainly determined by the length. For example, an N=12 square spiral inductor with 300 mil length and width is 4.47 nH with 10 um width and 10 um spacing but only increases to 4.55 nH with 8 um width and 12 um spacing, a variation of < 2%.

The capacitance values are more strongly affected, as the capacitance is directly proportional to the area. A representative capacitor might have been 20 um X 50 um, so a variation of +/- 2 um represents a variation of almost 15% and this variation dominated the attempted Monte Carlo variation. However, the match was broadband enough to accommodate this variation and still achieve return losses of better than 12 dB – sufficient to only negligibly affect the gain.



The final layout is given below. The inductors provide a general reference for where the circuits are; the upper inductor is the source inductor, the lower-left inductor is the input matching inductor, and the right-most inductor is the output matching inductor. The layout was relatively straightforward, although the 50 ohm stabilization resistor (which became a 50 ohm bias resistor) was initially undersized. It was 10 um wide and the TQPED process specifies the NiCr resistors as being rated for 1.5 mA / um, and there was simply no reason to design at the limit. The use of Metal0 (red) as the main routing layer would not normally be recommended, as the current handling is much reduced as compared to Metal1 and Metal2, but since the currents here are small, it is acceptable (and simplified routing, as capacitor connections always have one side connected to Metal0).



Test Plan

Test Equipment Required:

- Network Analyzer (S-Parameter Sweep)
- Signal Generator / Spectrum Analyzer or Network Analyzer (Power Sweep)
- Noise Diode / Spectrum Analyzer (Noise Figure Measurement)
- ~ 20 dB of additional RF gain with characterized noise figure performance
- Two RF Probes (RF Input and RF Output)
- Two DC Probes (Vcc and Vg Adjust)

1. Starting at Vcc=0V, step up the supply voltage towards +3.0V, keeping track of the current draw. If the current approaches 19 mA (total, of which 16 mA will be into the device) before Vcc = +3.0V is achieved, utilize the "Vg Adjust" pin to override the passive on-chip gate bias and lower the gate voltage, ultimately allowing Vcc to be +3.0V with current of 19 mA. Similarly, if Vcc = +3.0V results in a current draw lower than 19 mA, utilize Vg Adjust to increase the gate voltage to achieve +3.0V / 19 mA operation. Note: while LNA was designed to be unconditionally stable, it would be recommended to terminate input and output into 50 ohms; an unexpected oscillation could affect the bias.
2. Once properly biased, sweep the amplifier on a network analyzer with an input power of approximately -20 dBm (small signal relative to expected compression point). A sweep utilizing the full bandwidth of the network analyzer should be performed in order to verify out of band stability.
3. A power sweep shall be performed, either using the network analyzer in single-frequency continuous wave (CW) mode or using a signal generator and a spectrum analyzer, to find P-1 dB. This should be verified at 2.3, 2.4, and 2.5 GHz.
4. The noise figure of the device shall be characterized. With only ~ 10 dB of gain, additional amplification will be required to overcome the noise figure of the spectrum analyzer, with the amount of additional gain required dependent upon the spectrum analyzer's performance (i.e. internal preamp or not).

Summary and Conclusions

Revisiting the original specifications and goals:

Parameter	Specification	Goal	Design
Operating Frequency	2.3 to 2.5 GHz	2.3 to 2.5 GHz, same specs	
Gain, S21	10 dB < Gain < 12 dB	Same	10.7 – 11.3 dB
Gain Variation (Ripple)	< 1.0 dB	< 0.5 dB	0.6 dB
NF	NF < 1.0 dB	NF < 0.8 dB	0.87 dB
S11	< -10 dB	< -15 dB	< -19 dB
S22	< -15 dB	< -20 dB	< -20 dB
Power Supply Requirements	Single Supply, +3.0V	+3.0V to +3.6V operation	Little variation in S-Parameters
Power consumption	< 50 mW	Same	< 60 mW
Input P-1 dB	-3.5 dBm	Same	-3.9 dBm
Output P-1 dB	+6.5 dBm	Same	+7.7 dBm
Stability	"Stable" – no obvious issues, especially near operating frequency	Unconditionally Stable, entire frequency range	Unconditionally Stable, entire frequency range

The priority specifications of gain ~ 10 dB with a NF of < 1.0 dB were met. However, there is some room for improvement. Specifically, the resistive stabilization network consumes DC power (~ 9 mW) and the resistors are not bypassed at the operational frequency of 2.4 GHz, reducing gain, output power capability, and overall efficiency. Initial efforts of bypassing the resistor resulted in a high-frequency resonance so the resistors were not RF-bypassed.

Accepting an inferior input return loss would have allowed a slight improvement in noise figure (most likely < 0.1 dB improvement) and would also have allowed higher gain (less source inductor feedback).

The input P-1 dB specification was missed slightly, but the output P-1 dB was higher than spec. This was due to the unknown difference in simulated gain when driven from a power sweep source instead of a linear sweep.

The bias current variation as a function of power supply voltage, acceptable for now in a lab environment where it can be adjusted, would need to be reduced with active biasing techniques.

I would like to thank AWR / Microwave Office for the use of their IC design software and for the support from Gary Wray. I would also like to thank Triquint Semiconductor for allowing these circuits to be fabricated.