

HPA MMIC Design—Final Project

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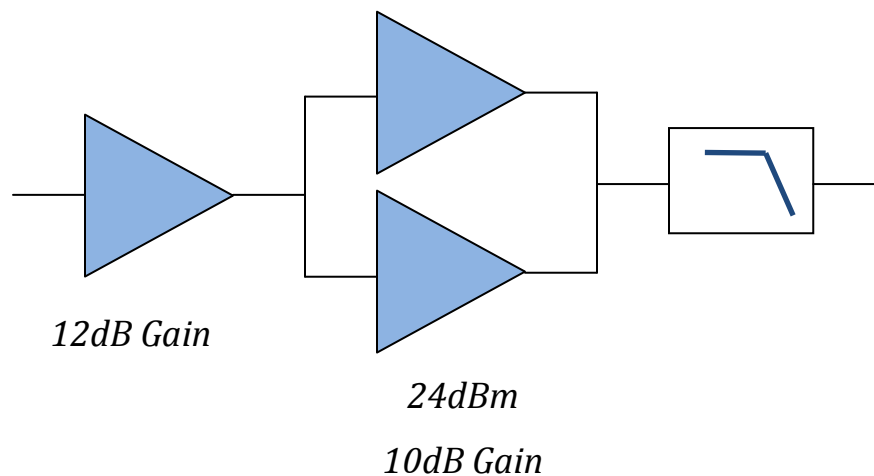
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Abstract: 24dBm

This document describes a 24dBm power amplifier, with 20dB gain, designed for 2.40 to 2.50GHz. It consists of three 6 x 140 μ m depletion PHEMPTs, each biased at +3V drain voltage and -0.25V gate voltage. Each FET draws about 110mA. The driver stage operates linear. The output stage consists of two FETs connected in parallel. A lowpass filter on the output stage reduces the 2nd and 3rd Harmonic to less than -30dBc. The bandpass filter impedance was chosen so that it transforms 50 ohms to the desired load line impedance for the HPA stage.

The circuit was designed with Microwave Office software using Triquint MMIC component libraries.



Design Goals

The design goals for the power amplifier are summarized in Table 1. The -30dBc harmonics requirement was self-imposed.

Operating Frequency	2.40 – 2.50 GHz
Compressed Output Power	24dBm
Small Signal Gain	22dB
Compressed Gain	20dB at 24dBm Output Power
Input Match	15dB
Output Match	10dB
2 nd and 3 rd Harmonics	-30dBc at 24dBm Output Power
Power Added Efficiency (PAE)	30%
Drain Voltage	+3V
Stability	Unconditionally Stable

Table 1: Power Amplifier Design Goals

Design Steps

1. Determine number of stages and bias point for each amplifier to achieve desired output power and efficiency. (Limited to +3V supply.) Efficiency is maximized by using fewer stages.
2. Design compressed power stage.
 - a. Design DC bias circuit.
 - b. Select output matching network to achieve load line that maximizes output power.
 - c. Include lowpass filter as part of OMN to suppress harmonics.
 - d. Stabilize FET with series and shunt resistors at gate.
3. Design linear driver stage
 - a. Design DC bias circuit.
 - b. Stabilize FET with series and shunt resistors at gate.
 - c. Determine desired load line that maximizes output power.
4. Design intermediate matching network so the input to the power stage presents the ideal load line to the driver stage.
5. Design the input matching network for the driver stage.
6. Verify stability, power out, gain, input match and other requirements of complete power amplifier.

Amplifier Topology and Bias Point

Efficiency is maximized by using fewer amplifier stages. Linear output power is maximized by only compressing the power stage. Two stages is an obvious choice, since 10dB gain per stage is typical and practical. A simple power budget helps determine the requirements for the two stages. The power stage is assumed to have 10dB power gain at 2dB compression. The driver stage is allotted 12dB gain.

If we want the driver amp to operate 2dB below compression, it will need to have a P1dB of at least $16.3\text{dBm} + 2\text{dB} = 18.3\text{dBm}$. If the driver stage consists of two FETs in parallel, each FET must have a minimum output power of $24.3\text{dBm} - 3\text{dB} = 21.3\text{dBm}$. Therefore, it is reasonable to use the same FET at the same bias point for both stages, but with the output stage having two FETs in parallel.

Achieving approximately 30% power added efficiency, will limit the drain current to each FET to a little less than 100mA. Efficiency could probably be improved slightly by reducing the drain bias current to the driver amp, but for simplicity, I chose to bias all three FET identically.

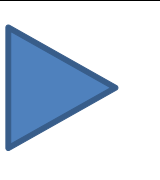
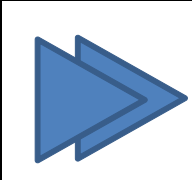

			
	Driver	Power Amp	Low Pass Filter
Gain	12.0 dB	10.0 dB	-0.3 dB
Cum Gain	12.0 dB	22.0 dB	21.7 dB
Compression	0.0 dB	2.0 dB	0.0 dB
Pout 4.3 dBm	16.3 dBm	24.3 dBm	24.0 dBm
Pout 0.0027 W		0.27 W	0.25 W
Ibias	100 mA	200 mA	
Vbias	3.00 V	3.00 V	
Pdc	0.30 W	0.60 W	
Pout	0.25 W		
Pdc	0.90 W		
PAE	27.6%		

Table 2: Power Budget

IV curves for a 6x140μm depletion PHEMPT show that $V_{gs} = -0.25V$ achieves I_{ds} of approximately 100mA at $V_{ds} = 3V$. This FET (6x140 depletion PHEMPT) and this approximate bias point ($V_{gs} = -0.25V$, $V_{ds} = 3V$, $I_{ds} = 100mA$) are used for all three FETs in the power amplifier.

The dynamic load line at 2.45GHz for the driver stage in the complete power amplifier (when the power stage is at 24dBm) is superimposed on the FET IV curve. The driver stage is operating linearly, as desired.

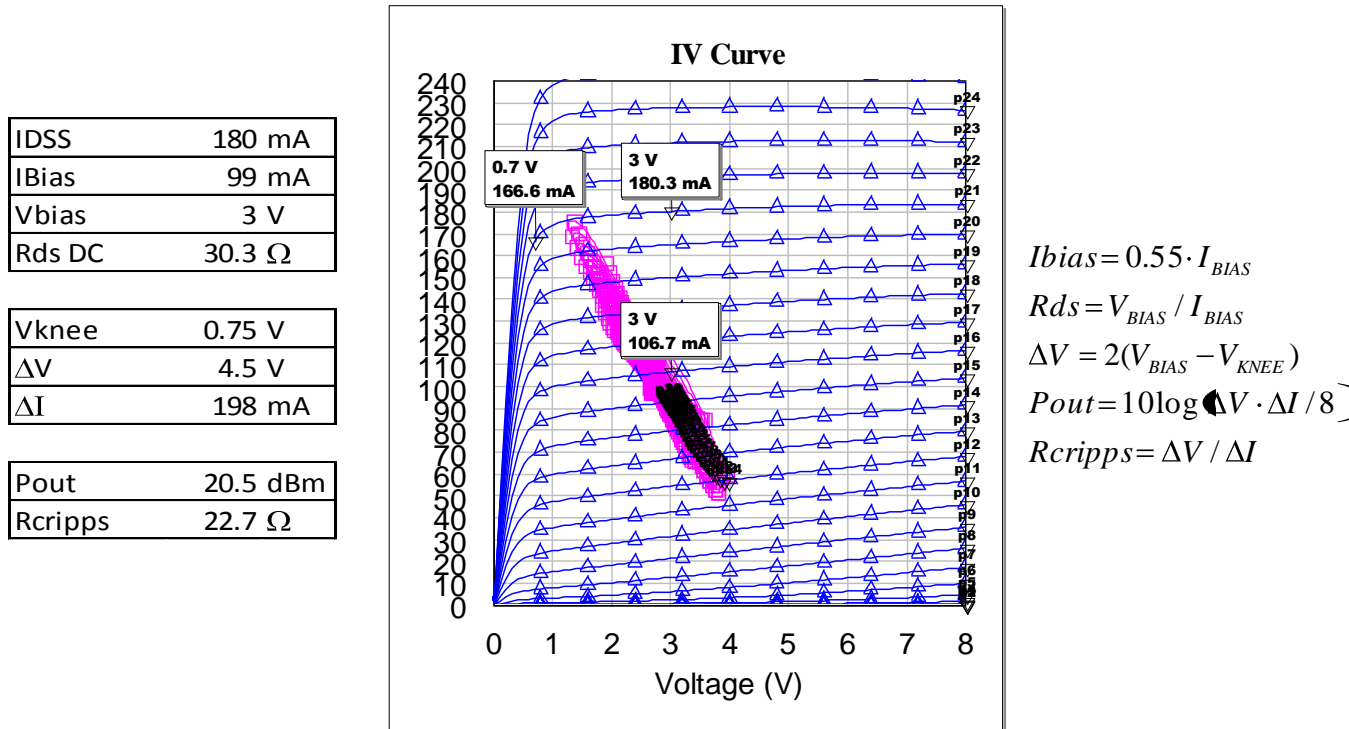


Figure 1: IV curve for 6x140μm FET with Driver Stage Dynamic Load Line

Power Stage

The IV curve for two 6x140μm FETs in parallel is shown in Figure 2. The DC bias condition for the two parallel FETs is shown in the schematic of Figure 3: Power Stage with Bias, and Stabilizing Resistors. We should expect an output power of about 23.5dBm with this power stage. The FETs should be sized slightly larger, but I decided to stick with the 6x140μm FETs. The load line of the power stage in the complete power amplifier is superimposed on the IV curves of Figure 2. Driven deeper into compression, it does achieve an output power >24dBm

IDSS	360 mA
IBias	198 mA
Vbias	3 V
Rds DC	15.2 Ω

Vknee	0.75 V
ΔV	4.5 V
ΔI	396 mA

Pout	23.5 dBm
Rcripps	11.4 Ω

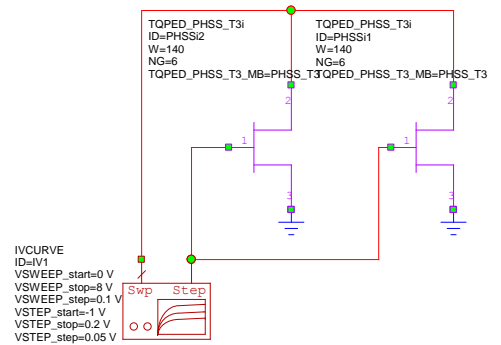
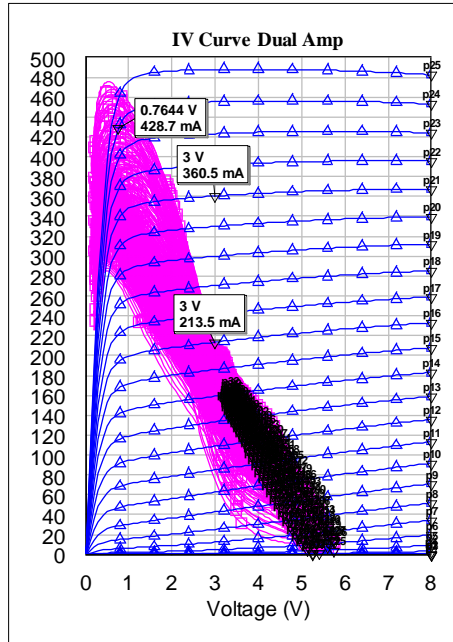


Figure 2: IV Curve for Power Stage

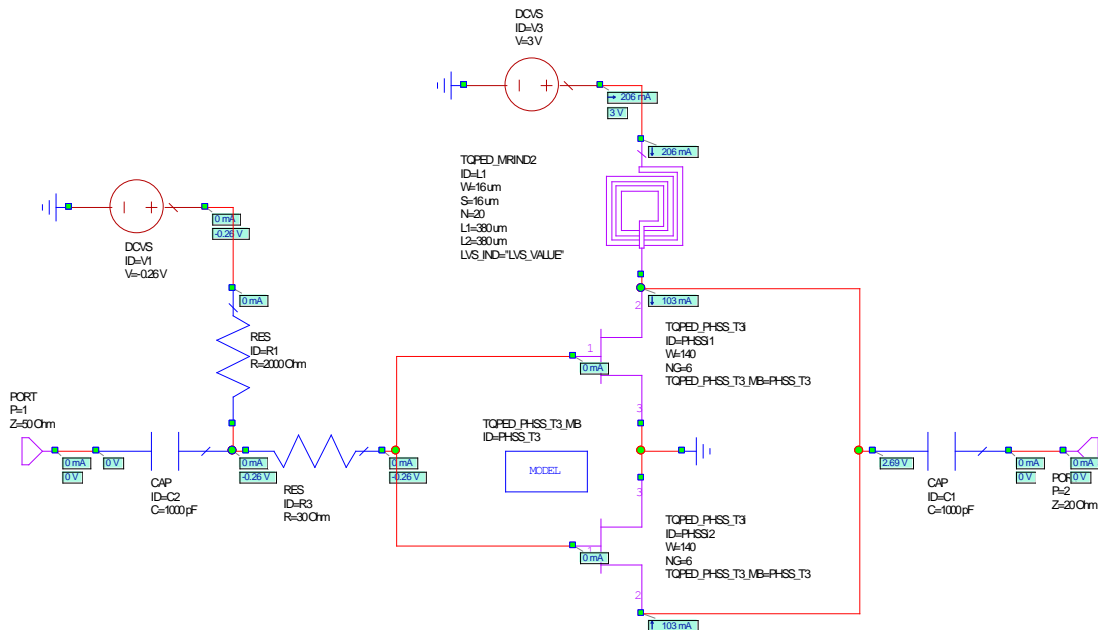


Figure 3: Power Stage with Bias, and Stabilizing Resistors

R_{ds} and C_{ds} for the two FETs in parallel are approximately 17.5Ω and 1.19pF as shown in Figure 4. To maximize output power, with $V_{ds} = 3\text{V}$, the power stage wants to see a load of $R_{cripps} = 15\Omega$. R_{cripps} and R_{ds} for the power stage are approximately equal, so we should expect a decent output match for the power amplifier. The output reactance is partly resonated out by the inductor in the V_{dd} bias circuit as is shown in Figure 5.

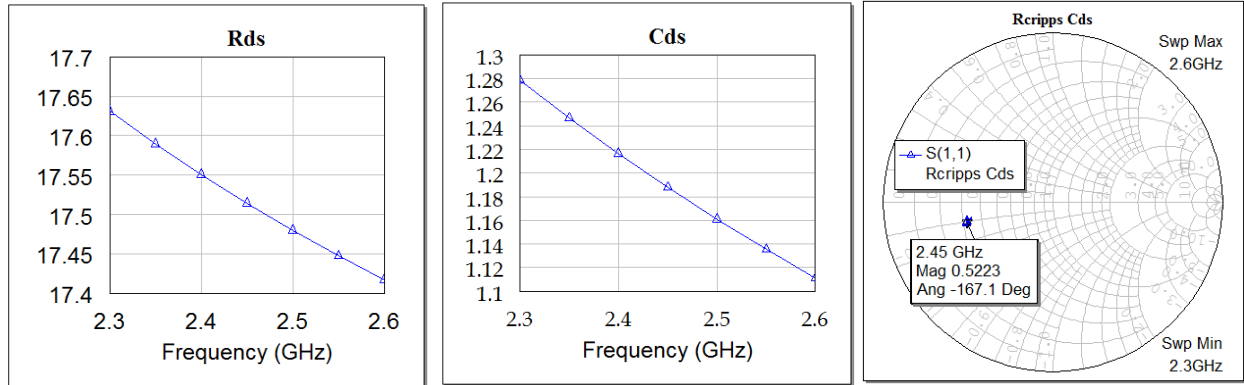


Figure 4: Rds and Cds for the Parallel 6x140µm FETs.

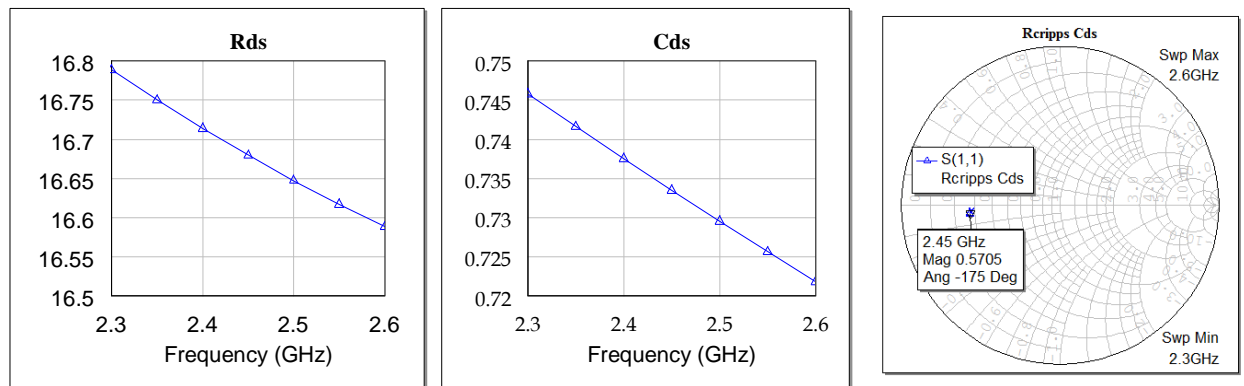
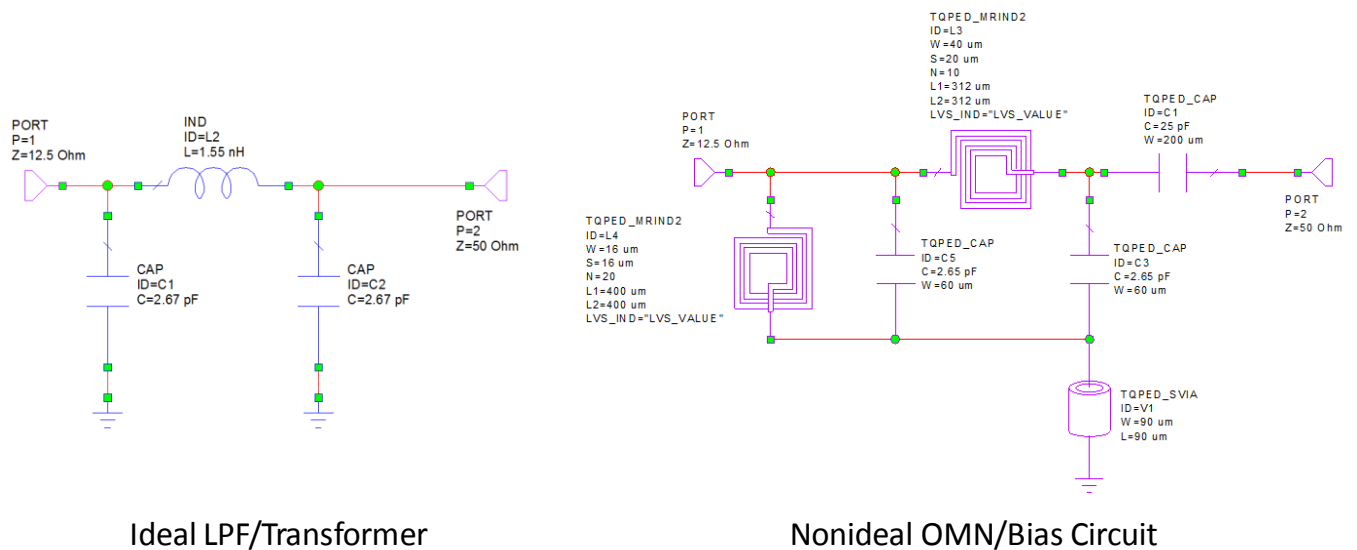


Figure 5: "Rcripps and Cds" with Vdd Bias Inductor Included

The power stage output matching network is a (maximally flat) lowpass filter whose impedance was selected to transform the 50Ω port to the desired load line. But, the lumped element low-pass filter is not simply a transmission line equivalent. For a lowpass T configuration transmission line equivalent, the inductors and capacitors have the same impedance $g_1=g_2=g_3=1.0$. For the lowpass filter, the inductors and capacitors have different impedances; $g_2=2.0$ for the inductors and $g_1=g_3=1.0$ for the capacitors.

Figure 12 shows the low pass filter / transformer with ideal lumped elements and the output matching network / bias circuit with Triquint MMIC elements. Performance is shown with the circuits driven by a 12.5Ω source. The output matching network / bias network has in-band return loss of approximately 20dB, in-band insertion loss of approximately 0.4dB, 10.3dB attenuation of the 2nd harmonic, and 18.6dB attenuation of the 3rd harmonic. Since $R_{ds} = 17\Omega$, not 12Ω , the OMN / Bias network should have been optimized for a 17Ω source. This is why the power stage has a 10dB match, instead of a 20dB match.



Ideal LPF/Transformer

Nonideal OMN/Bias Circuit

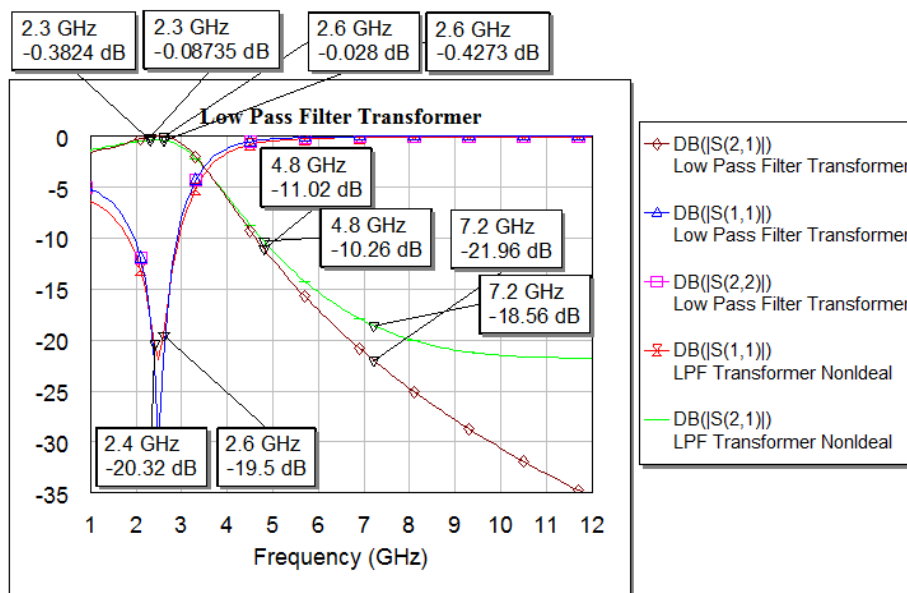


Figure 6: Output Matching Network: A LPF / Transform

The input matching network and gate stabilization resistors for the power stage are shown in Figure 7. Stability circles and mu stability parameters for the power stage are shown in Figure 8. Above 4.8 GHz, the input stability parameter is almost exactly 1, since the LPF is highly reflective outside the passband.

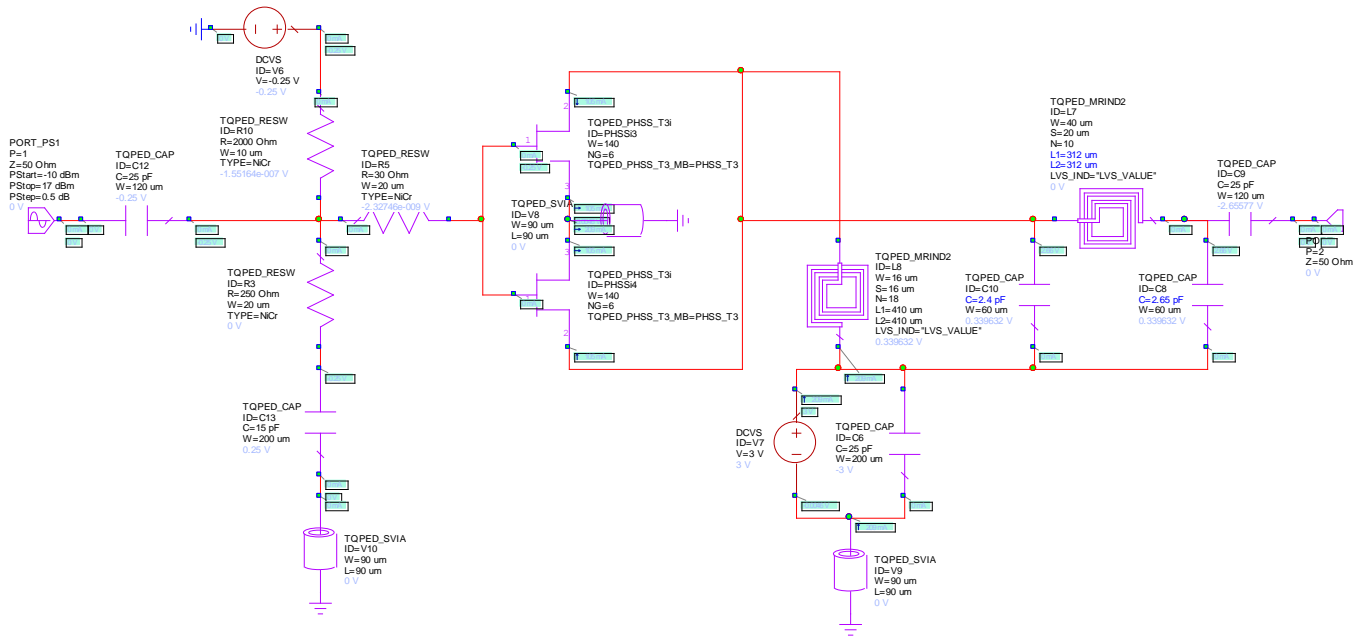


Figure 7: Power Stage with OMN and Gate Stabilization

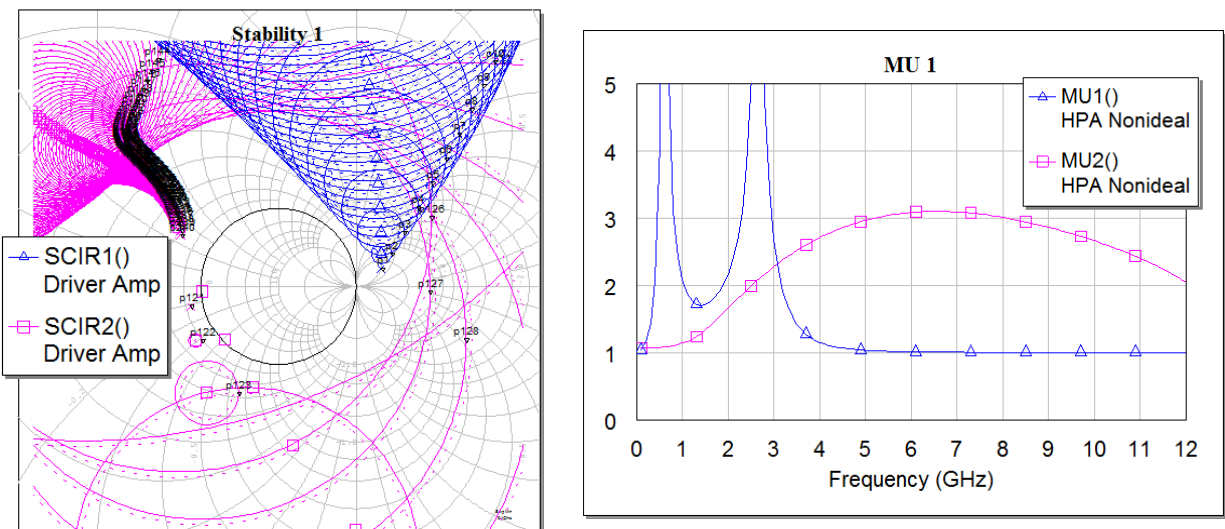
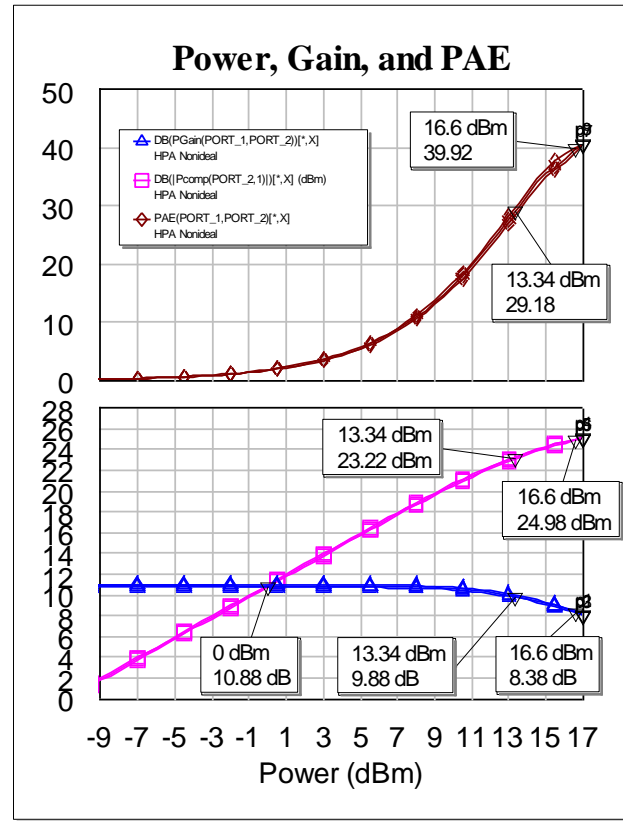
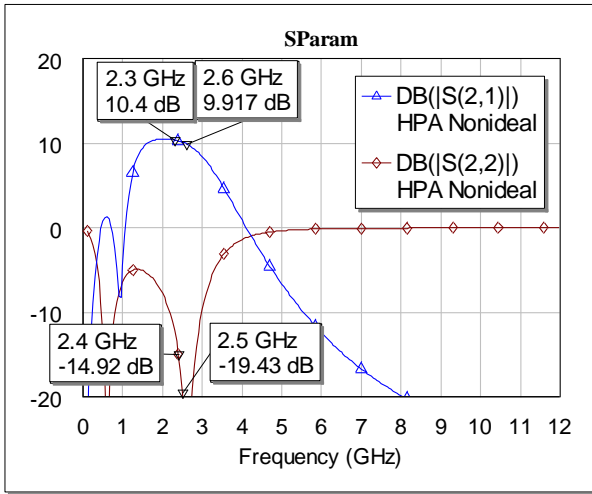


Figure 8: Stability Circles and Stability Parameters for Power Stage

The predicted output power of the power stage is approximately 25dBm and 8.4dB gain at 2.5dB compression, as shown in Figure 9. Power added efficiency approaches 40%. The 2nd and 3rd harmonics are -30dBc and -45dBc.



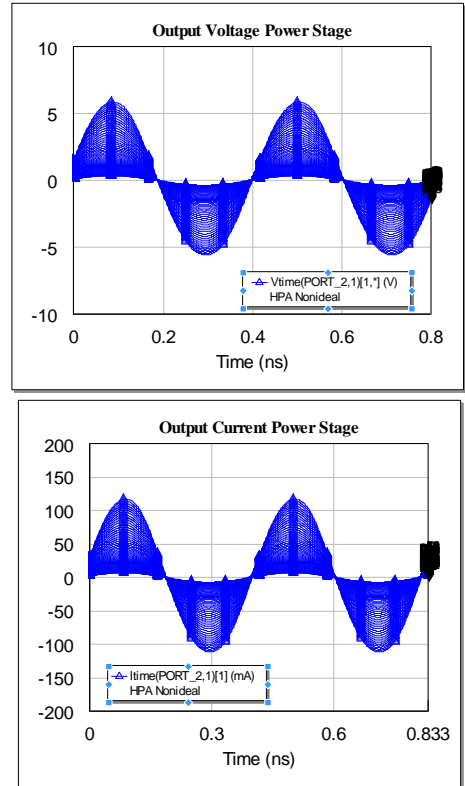
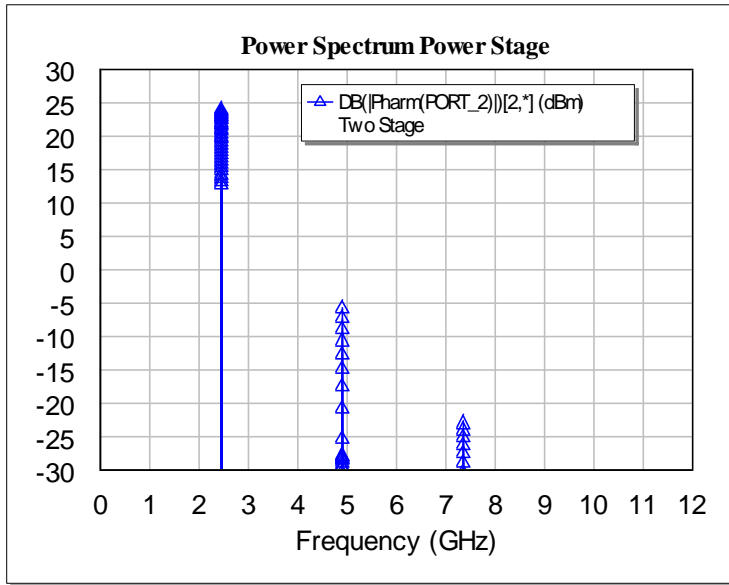


Figure 9: Power Stage Predicted Performance

Driver Stage

The driver FET with gate stabilizing resistors is shown in Figure 10. The FET is unconditionally stable from 0.1 to 12 GHz. It outputs about 16dBm power with about 12dB of gain when it is 0.5dB compressed. So, it is adequate to drive the power stage.

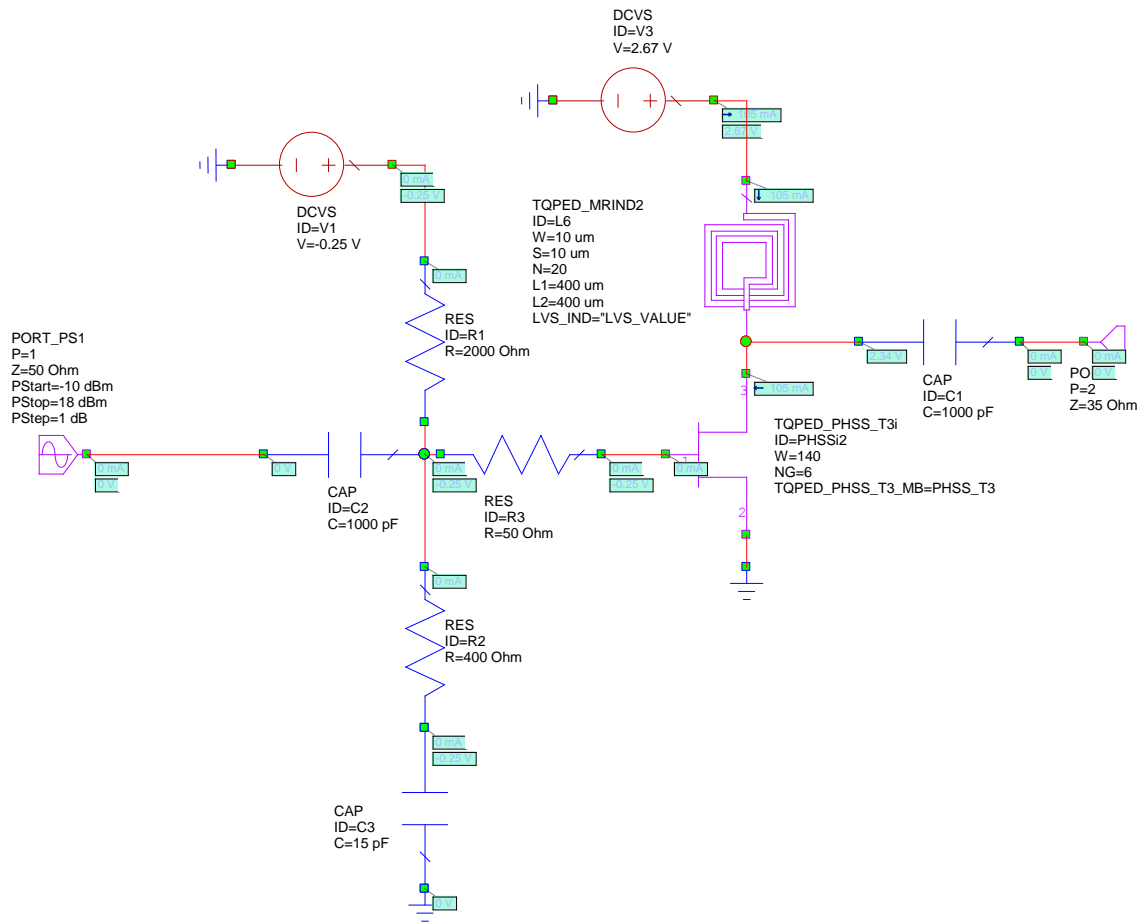


Figure 10: Driver Stage with Input Gate Stabilization

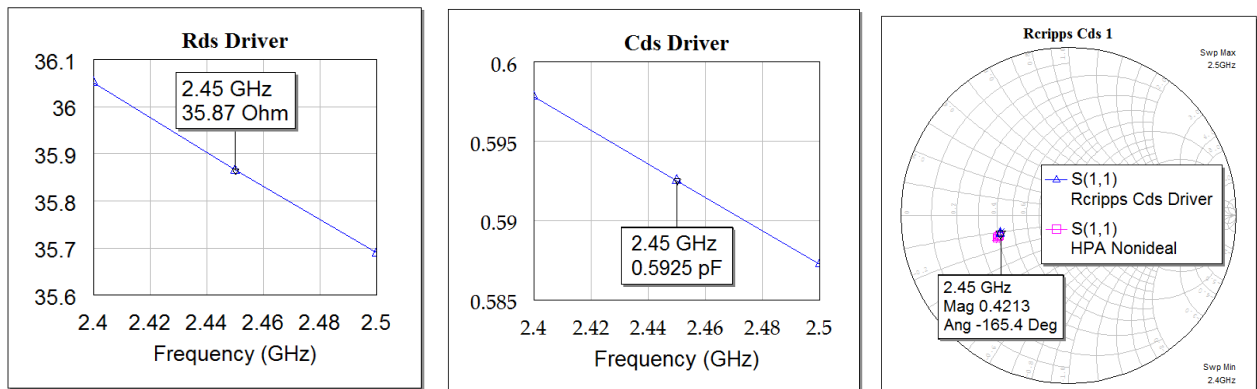


Figure 11: Rds and Cds for the Driver Stage

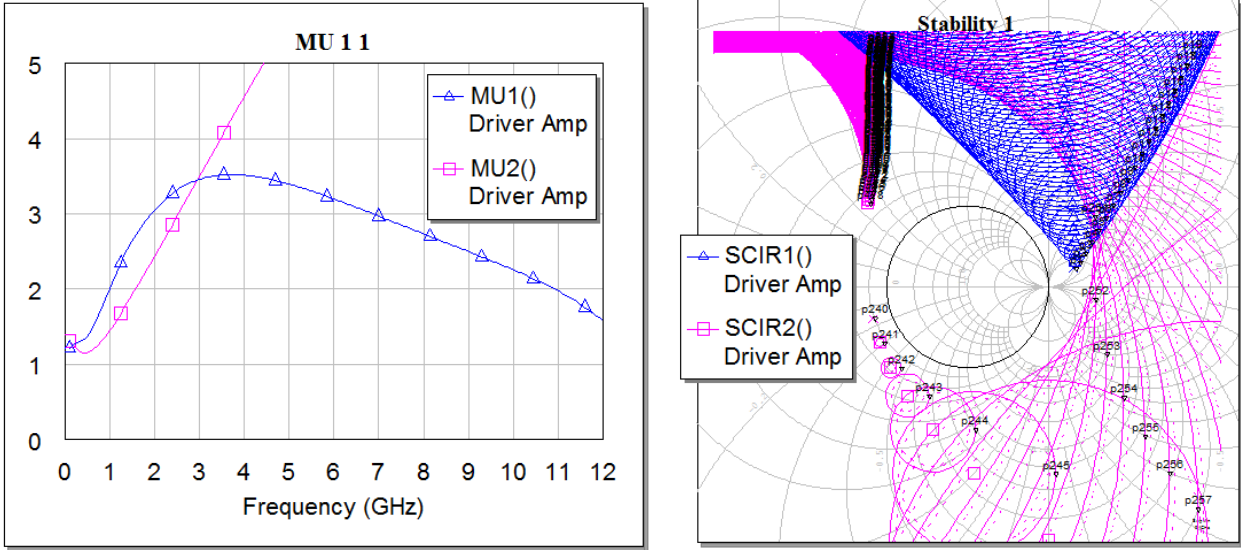


Figure 12: Stability Circles and Stability Parameters for the Driver Stage

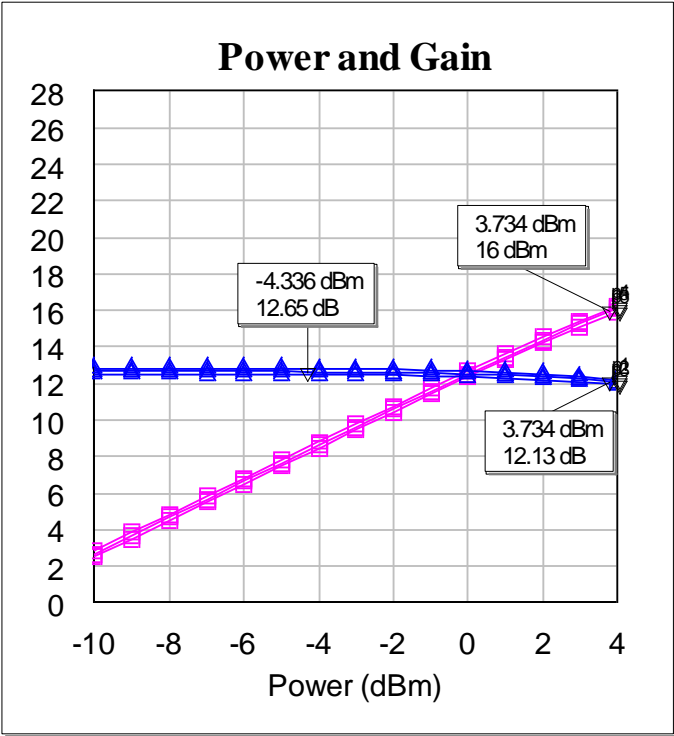


Figure 13: Output Power and Gain for the Driver Stage

Intermediate Matching

The intermediate matching circuit makes the input of the driver stage look like the ideal load line for the driver stage.

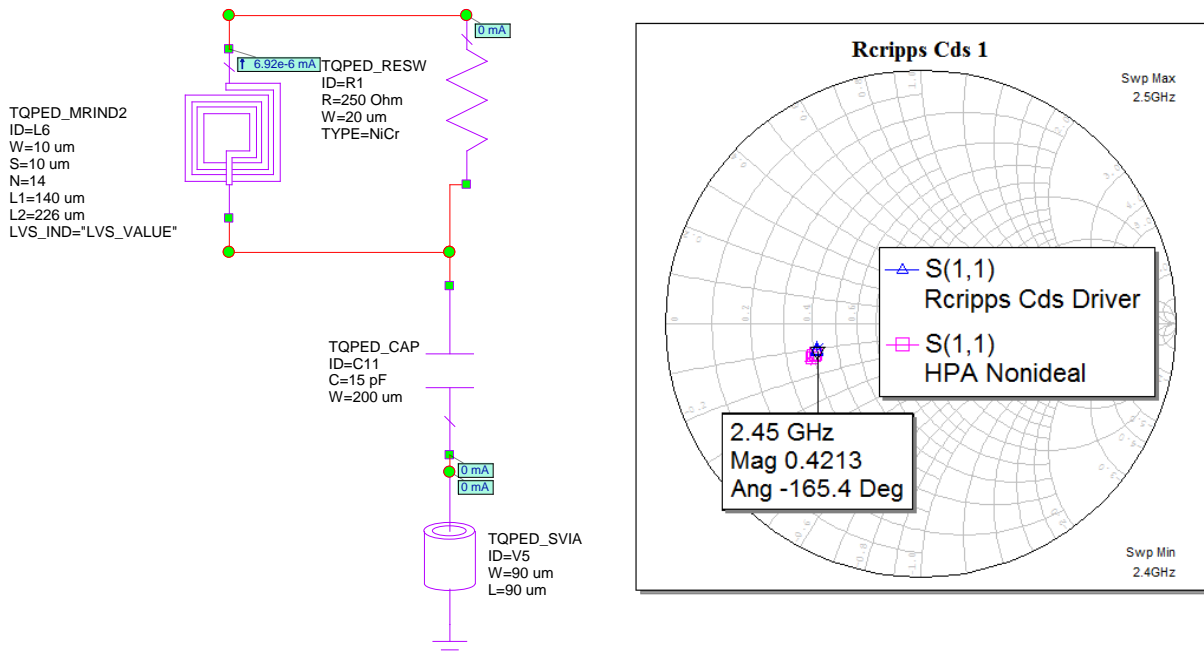


Figure 14: Intermediate Matching

The Complete Power Amplifier

The schematic and layout for the complete two stage power amplifier are shown in Figures 15 and 16. Somehow I forgot a filtering capacitor on the V_{gg} input. (Originally, I had one, but it was accidentally discarded during the layout process.) The inductor in the OMN / LPF consists of 40 μ m wide conductors to minimize loss.

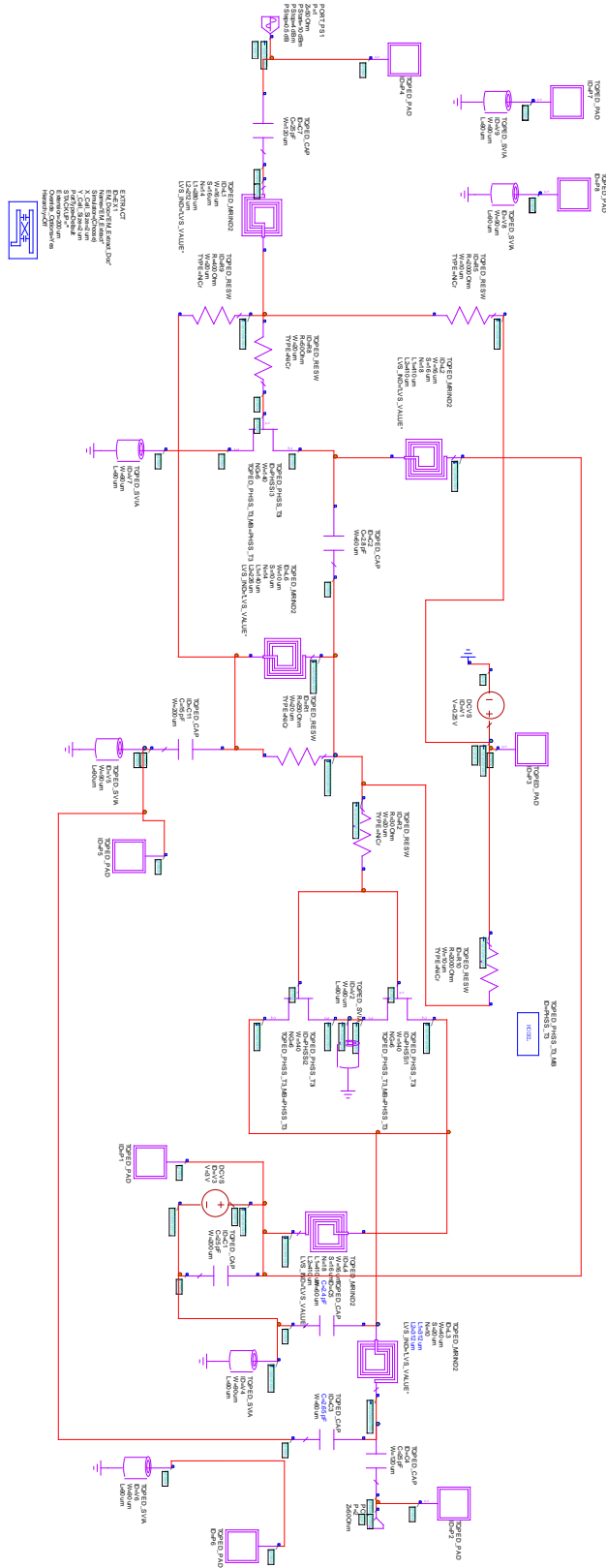


Figure 15: Schematic for Complete Power Amplifier

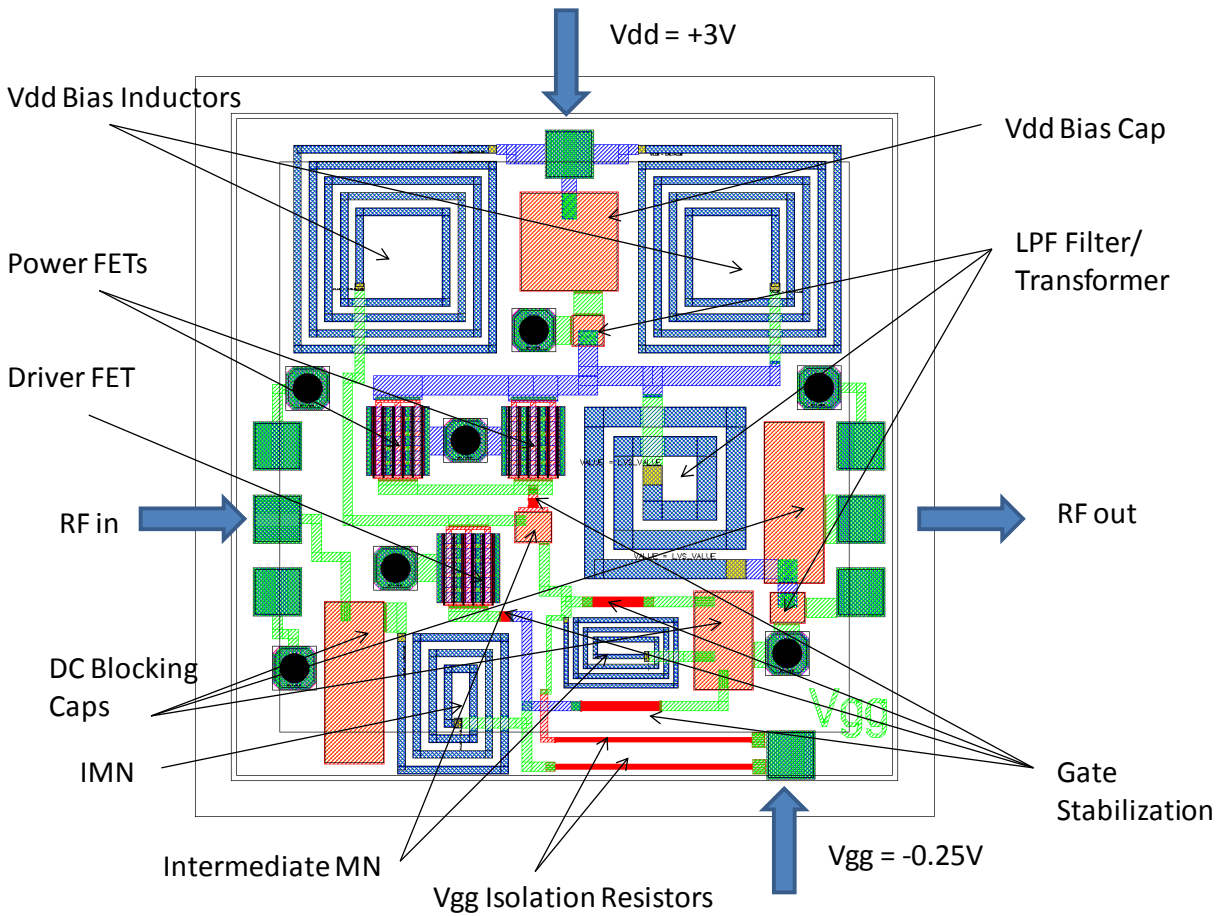


Figure 16: Layout for Complete Power Amp

Predicted Performance of Two Stage Amplifier

Simulations predicted 25dBm output power with 20.4dB gain at 2.5dB compression. The 2nd and 3rd harmonics are approximately -30dBc and -45dBc. The amplifier is unconditionally stable.

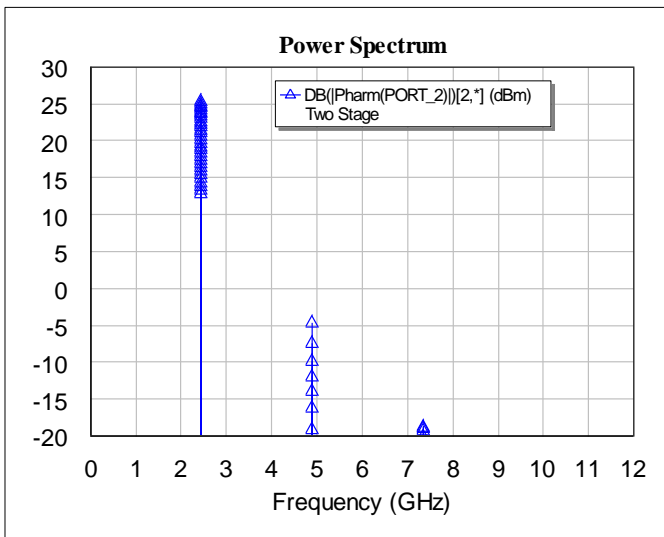
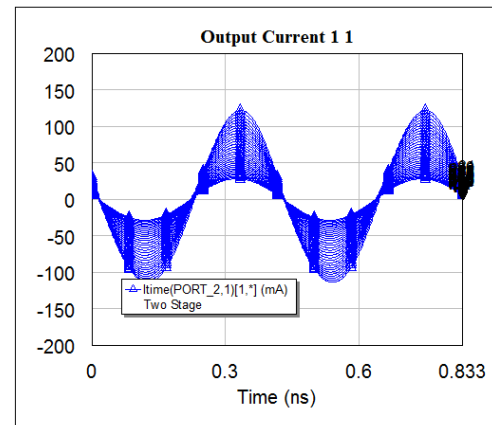
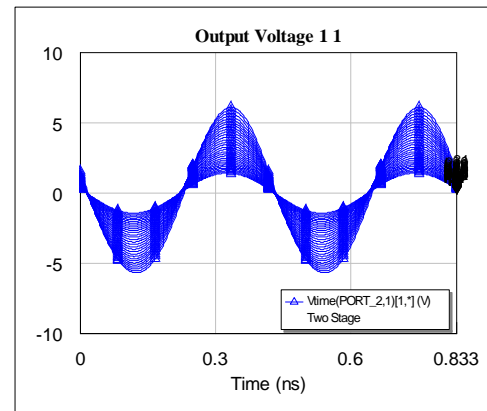
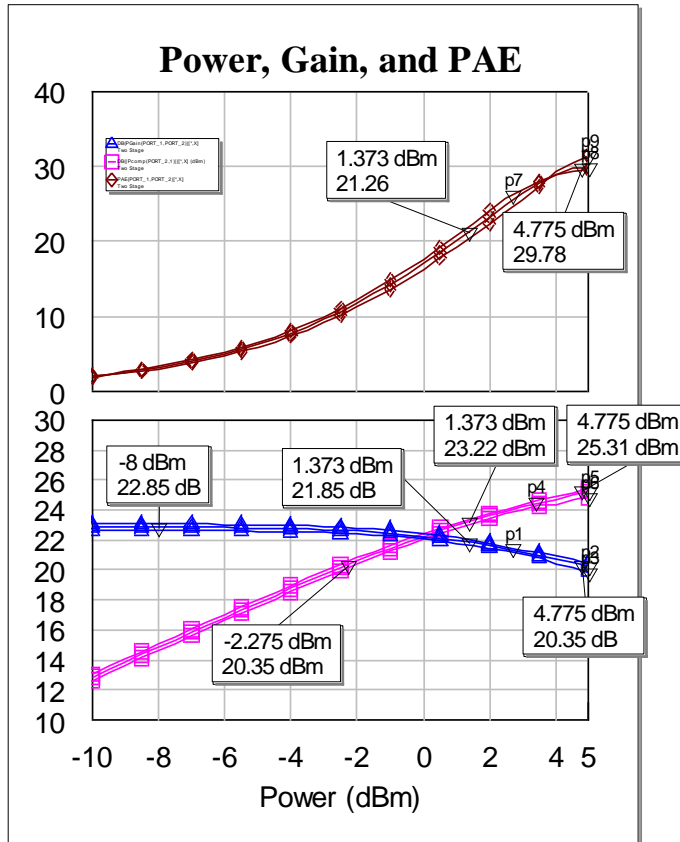


Figure 17: Predicted Power Out, Gain, Harmonics, and Efficiency

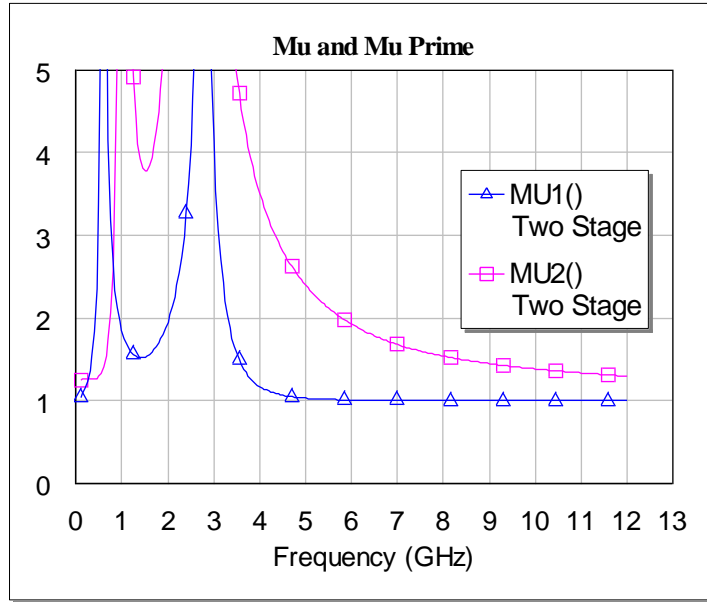


Figure 18: Stability of Complete Power Amp

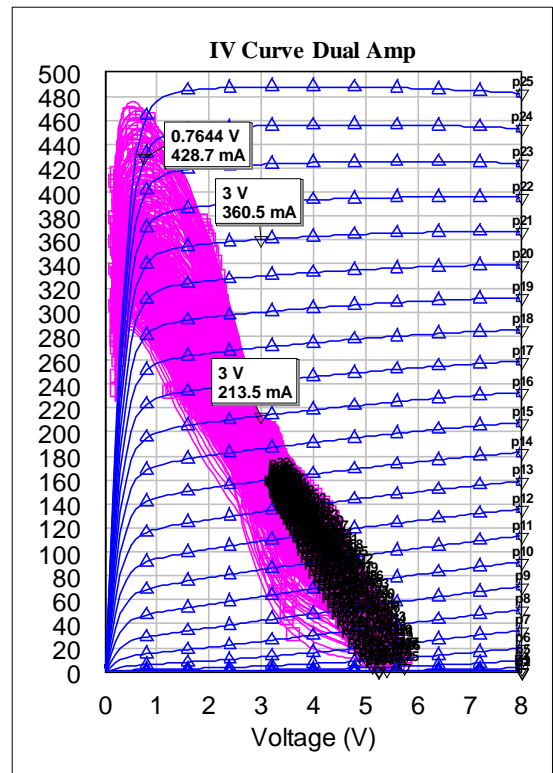
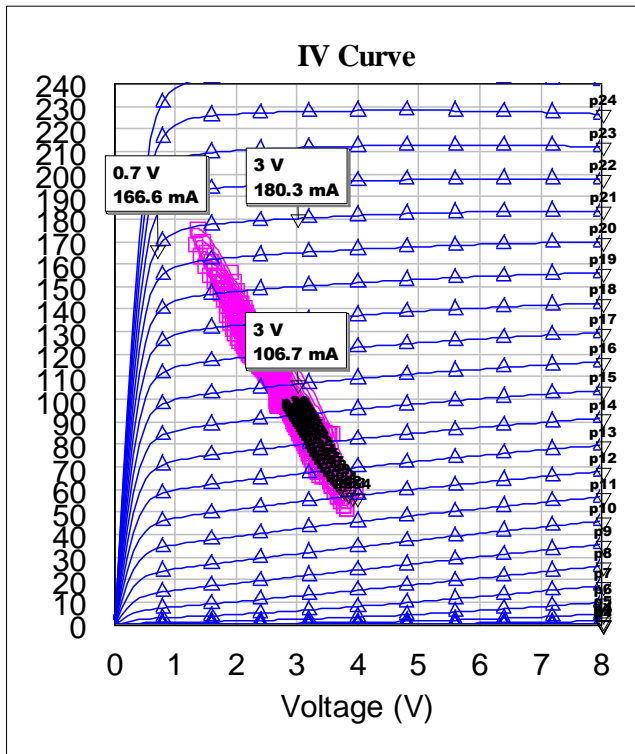


Figure 19: IV Curves for the Two Stages in the Complete Power Amp

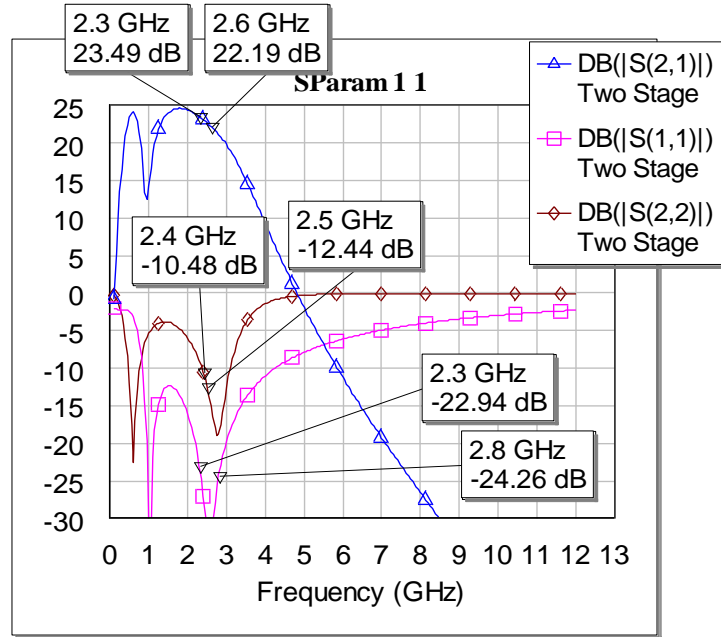


Figure 20: S Parameters

Summary and Conclusions

Simulations predict the power amplifier will meet its performance requires, except efficiency. It has about 29% PAE. If time permitted, I would redesign the amplifier with a little more margin, run tolerance studies and plot load pull contours.

Also, somehow the Vdd filter capacitor was omitted from the schematic and the layout, and a redesign would fix this omission.

	Requirement	Simulation
Operating Frequency	2.40 – 2.50 GHz	2.40 – 2.50 GHz
Compressed Output Power	22dBm	24.8dBm
Small Signal Gain	22dB	22.8dB
Compressed Gain	20dB at 24dBm Output Power	20.8dB
Input Match	15dB	22dB
Output Match	10dB	10.5dB
2 nd and 3 rd Harmonics	-30dBc at 24dBm Output Power	-30dBc 2 nd , -45dBc 3rd
Power Added Efficiency (PAE)	30%	29% at 24.8dBm
Drain Voltage	+3V	+3V
Stability	Unconditionally Stable	Unconditionally stable

Test Plan

1. Connect 50Ω load to RF output port.
2. Connect -0.25V to V_{gg} .
3. Connect $+3\text{V}$ to V_{dd} .
4. Connect -20dBm at 2.45 GHz to RF input port. Measure gain, input match, and output match. Observe stability.
5. Increase RF input power to -10dBm . Measure gain and observe stability.
6. Increase RF input power to $+6\text{dBm}$ in 1dB increments. Measure output power. Calculate gain. Stop when the amplifier is 3dB compressed.

