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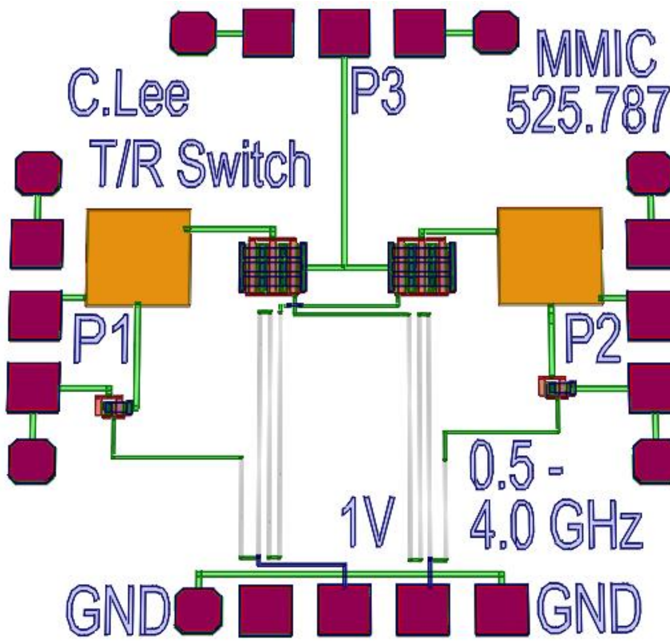

Monolithic Microwave Integrated Circuit
Course 525.787

Broadband Tx/Rx Switch: Final Report

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Abstract

A broadband monolithic microwave integrated circuit (MMIC) Tx/Rx switch is presented in this paper. The switch exhibits very low insertion loss (IL<0.5 dB) parameters for the RF ISM Bands of 2.4 GHz – 2.5 GHz. Simulations performed using Microwave Office (AWR corp.) exhibit a insertion loss of <0.8 dB for the RF frequency range from 0.5 GHz to 4.0 GHz and <0.5 dB for the ISM Bands mentioned above. The MMIC switch fits on a 60 mil x 60 mil GaAs chip with a +1V power supply. The transition between transmit (Tx) and receive (Rx) paths are controlled using two logic control BITS, either +1V "on" or 0V "off", to turn a path on and off. Enhancement (E-mode) pHEMTs are used for the switch and are to be fabricated by TriQuint Semiconductor Inc.

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1.0 Introduction

The broadband Tx/Rx switch was designed as a part of an S-band transceiver as depicted in Figure 1, System Block Diagram. It will be used to receive and transmit data within the ISM band frequencies of 2.4 GHz to 2.5 GHz. The broadband versatility of this switch allows for it to be used for multiple ISM bands. The switch covers the wireless communications service (WCS) frequencies from the lower ISM band range of 902 MHz to 928 MHz to the upper ISM band range of 2.4 GHz to 2.5 GHz. The design of this switch was tailored for low voltage-low power applications such as battery operated mobile devices. The design utilizes two control BITs for independent enable/disable operations of the Tx/Rx paths. This report details the design, simulation, layout, and test plan for the switch design.

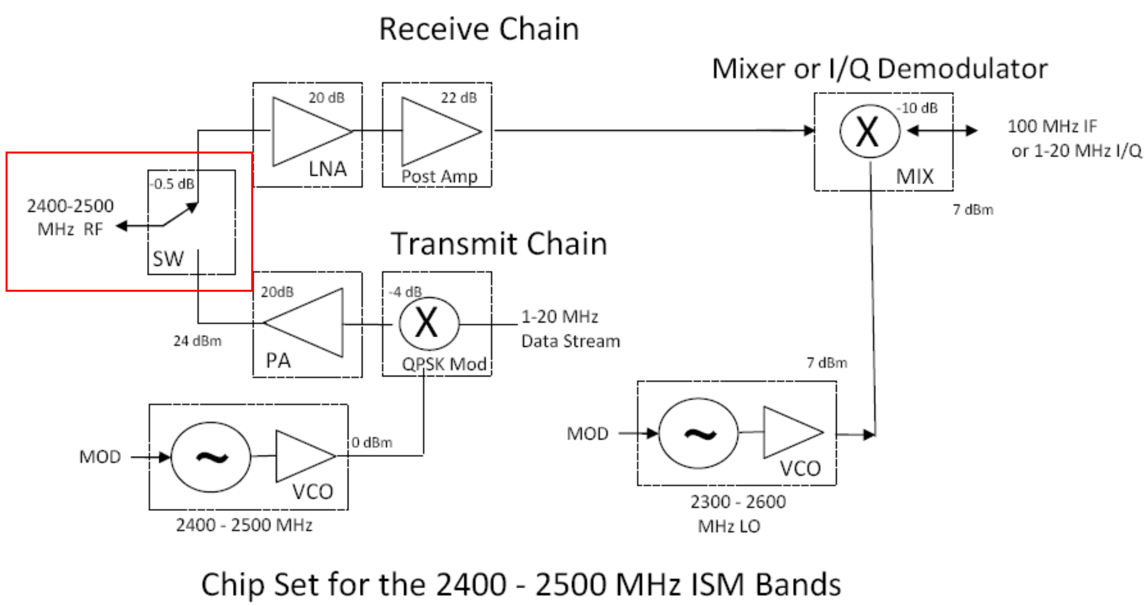

Figure 1. System Block Diagram

2.0 Design

The design for this switch was first modeled as a pure resistor when in the "ON" state and a capacitor when in the "OFF" state as shown in Figure 2.

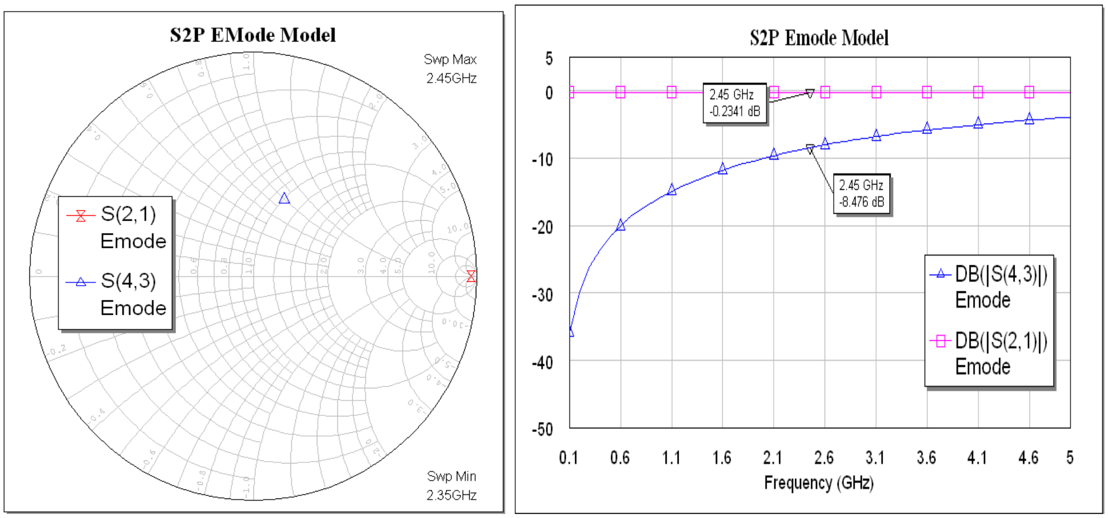

Figure 2. "ON" state-S21 measurement, "Off" state- S43 measurement

2.1 Circuit Approach

A single pHEMT device was size appropriately to match the "ON", "OFF" state RF characteristics shown in Figure 2.

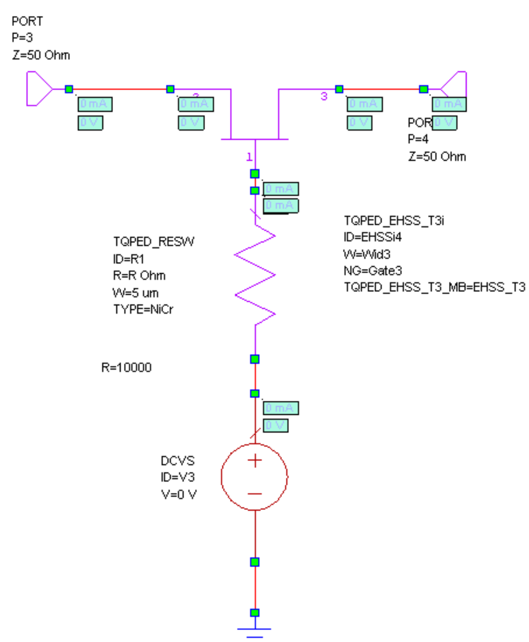

Figure 3. pHEMT device, sized to match RF performance of Figure 2.

2.2 Design specifications

Table 1, below shows the specifications for this design. These values were estimate "target" values set as an initial goal. With time permitting, these specifications would generally be improved upon. The mind set was to achieve these specifications first.

Specification	
Frequency range	2.4 to 2.5 GHz
Insertion Loss	<0.5 dB
Tx/Rx Port Isolation	20 dB
Power handling	20 dBm
Size	60mil X 60mil
Control Logic	3V supply

Table 1. Design specifications

2.3 Trade-offs

Two circuit typologies where initially simulated with varying results. Circuit A incorporated external input (IMN) and output matching networks (OMN) shown in Figure 4A. The simulation (not provided) for this typology met the IL <0.5dB using ideal microwave elements for the specified bandwidth, however, sharply increased once outside the specified bandwidth. Once lossy elements were introduced this typology failed the IL specification for the specified bandwidth. This typology was bandwidth limited since the IMN/OMN circuits were tuned for a center frequency of 2.45 GHz. The benefit to this typology was good input/out matching (-60 dB return loss).

Ultimately the design chosen (circuit B) was to incorporate the IMN/OMN into the pHEMT devices. By sizing the pHEMT devices appropriately the IMN/OMN could be achieve to a limited degree. The benefit from this typology provided for a greater bandwidth and less IL across the greater bandwidth. Once real elements were introduced, the IL was relatively maintained and still met the specified IL for the given bandwidth. Circuit B is shown in Figure 4B.

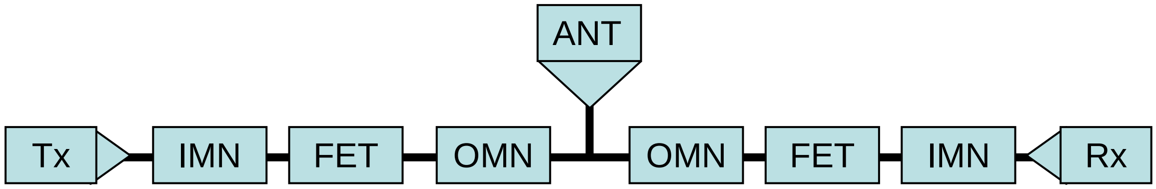

Figure 4A, Circuit A Block Diagram

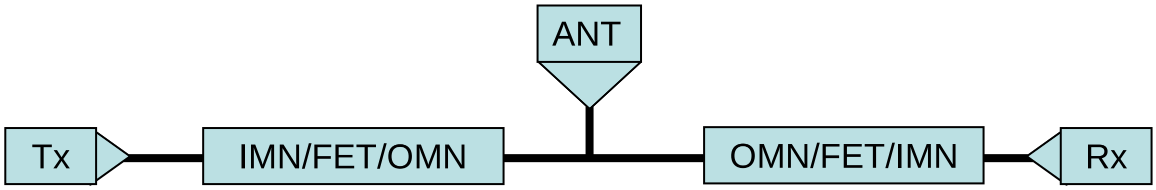

Figure 4B, Circuit B Block Diagram

3.0 RF Performance

Shown below are the simulation results for the pHEMT Model, Ideal Switch Model and Real Switch.

3.1 pHEMT Model Performance

Figure 5 shows the RF performance for the "sized" pHEMT device itself. The simulated IL for the "sized" pHEMT was 0.23 dB at a center frequency of 2.45 GHz, when turned "ON".

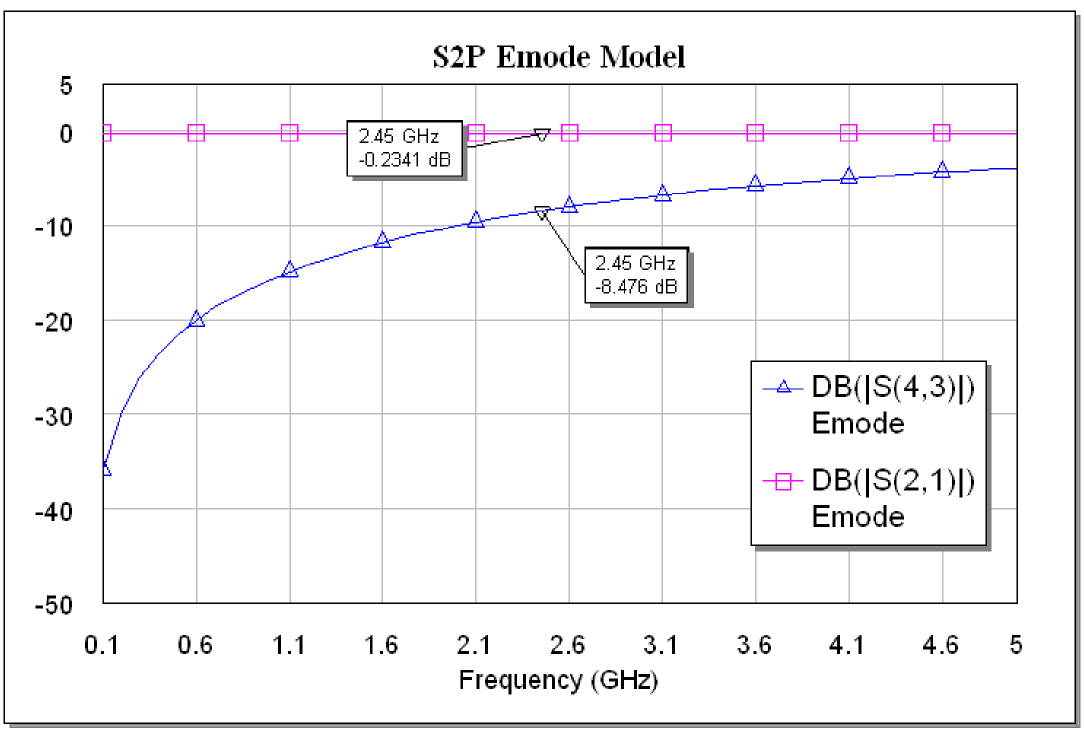

Figure.5. S-parameter performance of the "sized" pHEMT model. S21-"ON"; S43-"OFF"

3.1.1 Ideal Switch RF Performance Results

Figure 6 shows the RF performance for the Ideal Switch. With the Tx path "ON", Rx path "OFF", the simulated IL for the Ideal switch was 0.43 dB. The Isolation from Tx/Rx Ports was ~26.5 dB.

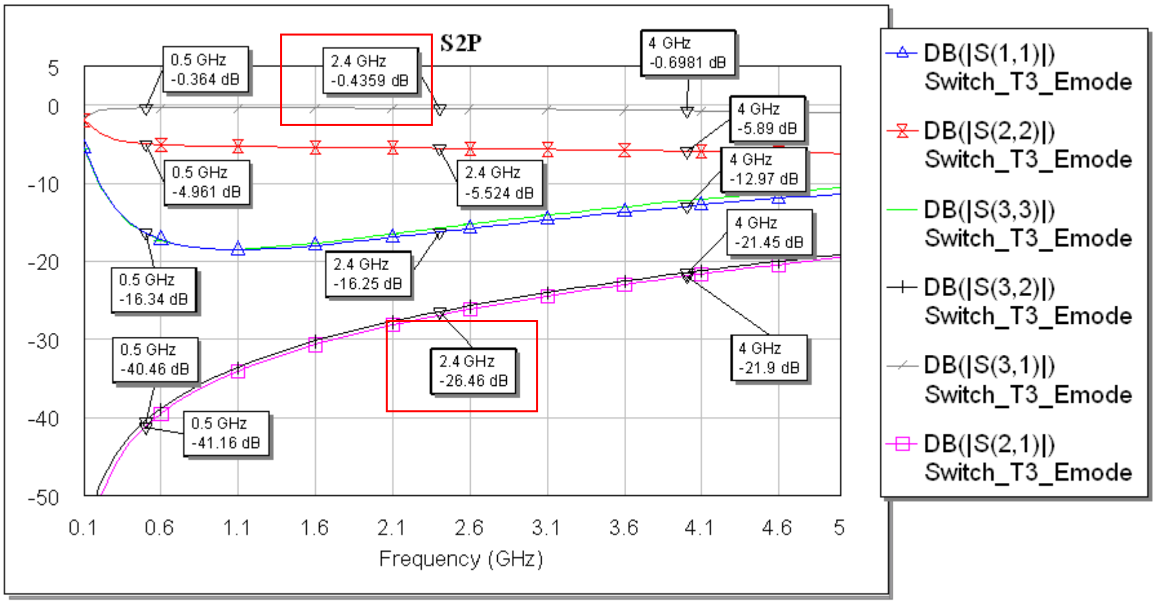

Figure 6. RF simulation results of Ideal Tx/Rx Switch. Tx = Port 1, Rx = Port 2, ANT = Port 3 Tx "ON", Rx "OFF"

3.1.2 Real Switch RF Performance Results

Figure 7A, 7B, and Table 2 summarizes the results of the real element switch circuit. With the same Tx/Rx settings as the Ideal switch for Figure 6, the real switch's IL was 0.45 dB, a delta of 0.02 dB. The isolation also changed from ~26.5 dB to ~25.4 dB, a delta of 1.1 dB.

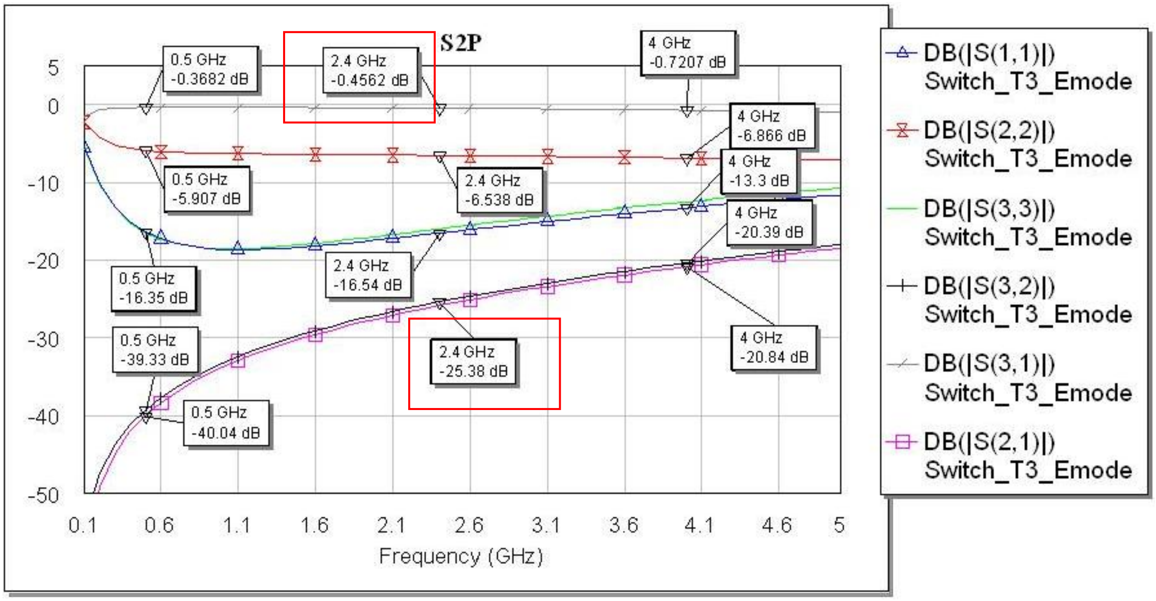

Figure 7A. RF simulation results of real Tx/Rx Switch. Tx = Port 1, Rx = Port 2, ANT = Port 3 Tx "ON", Rx "OFF", Reciprocal values were verified with Rx "ON" and Tx "OFF".

The power handling capability for this switch was simulated to be fairly linear up to Pout = 20 dBm.

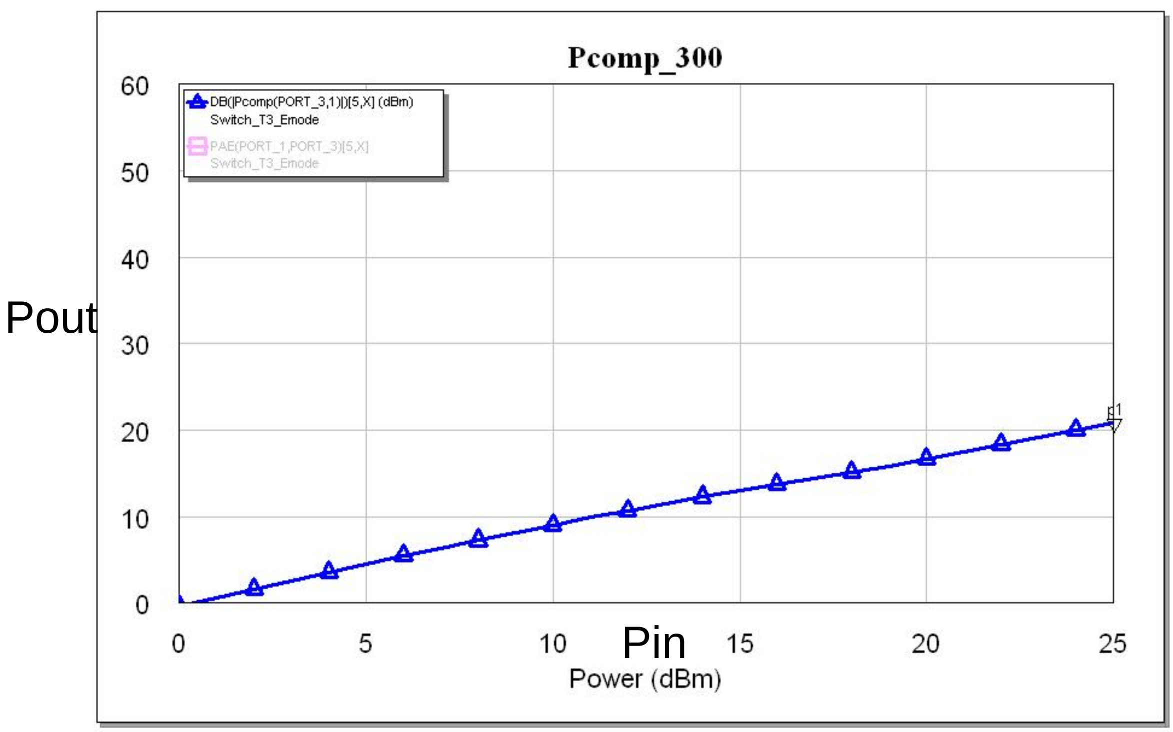

Figure 7B. Power handling results of Tx/Rx Switch.

Highlighted in Table 2 are the specification goals as well as the simulated final results. For the specified frequency range, the IL met its requirement of <0.5 dB. From 0.5 GHz to 4.0 dB GHz, the IL increased linearly from 0.3 dB to 0.7 dB. The Isolation decreased from 40 dB to 20 dB across frequency.

Specification		Simulation Results	
Frequency range	2.4 to 2.5 GHz	2.4 to 2.5 GHz	0.5 to 4.0 GHz
Insertion Loss	<0.5 dB	0.45 dB	0.3 to 0.7 dB
Tx/Rx Port Isolation	20 dB	25 dB	40 to 20 dB
Power handling	20 dBm	20 dBm	20 dBm
Size	60mil X 60mil	60mil X 60mil	60mil X 60mil
Control Logic	3V supply	1V, 0V control	1V, 0V control

Table 2. Specification Vs simulation results.

4.0 Tx/Rx Switch Schematic

Figure 8 below shows the schematic for the Tx/Rx Switch. The switch composes of a DC blocking capacitor in series with a shunt FET and series FET for each Tx/Rx path. The shunt and series FETs were sized to appropriately best match the input and output to a 50 ohm load, while maintaining the low IL. Per each Tx/Rx path, the shunt and series FETs are in opposite states, i.e. when one FET is “ON”, the other is “OFF”. This feature was incorporated to increase isolation from Tx Port to Rx Port and vice versa. For example, when the Tx series FET is “ON”, we have a “thru” path from the Tx Port to the Antenna Port, since the Tx shunt FET is “OFF”. At the same time, the Rx series FET is “OFF”, creating a “RF Block”. Any unwanted signal that leaks through from either Tx or Antenna Ports to the Rx Port is shorted to ground since the Rx shunt FET is “ON”. Port 1 = Tx, Port 2 = Rx, Port 3 = Antenna.

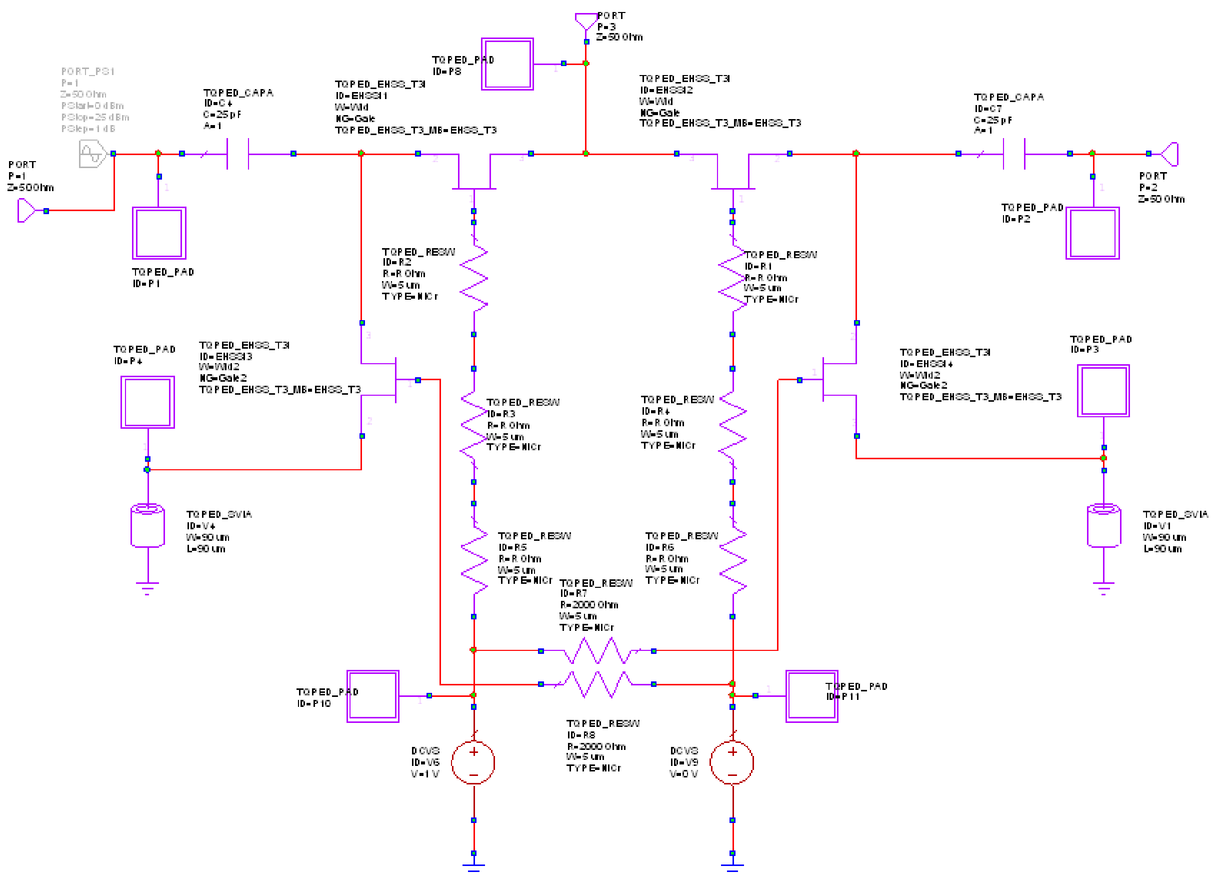

Figure 8. Schematic of the Tx/Rx Switch.

4.1 Final Layout

Figure 9 shows the final layout of the Tx/Rx Switch. With Port 1 or Port 2 as Tx or Rx and Port 3 as Antenna Port. The BIT logic port is shown as well.

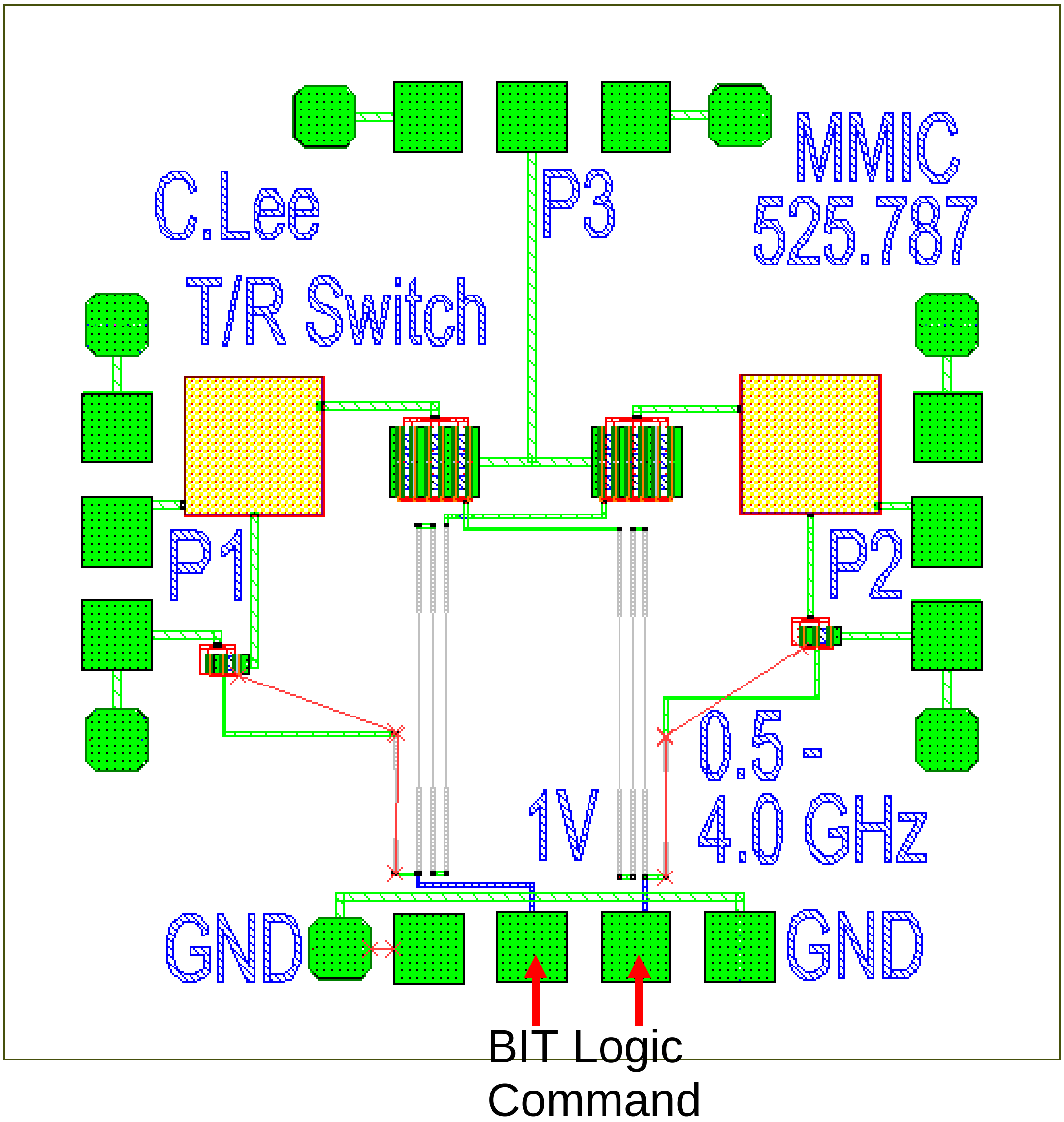

Figure 9. Layout of the Tx/Rx Switch.

5.0 Test Plan

The test plan for this switch assumes that the tester has the knowledge of performing a full 2-port SOLT calibration of the VNA/ test equipment and therefore the calibration process will not be explained here. The test equipment required for testing this switch are:

1) Network Analyzer capable of measuring and recording s2p parameters up to 4.5 GHz
2) DC power for Logic Command
3) Probe station for the device under test (DUT).

5.1 Test Equipment Configuration

Figure 10, shows the test setup required for performing the required RF tests.

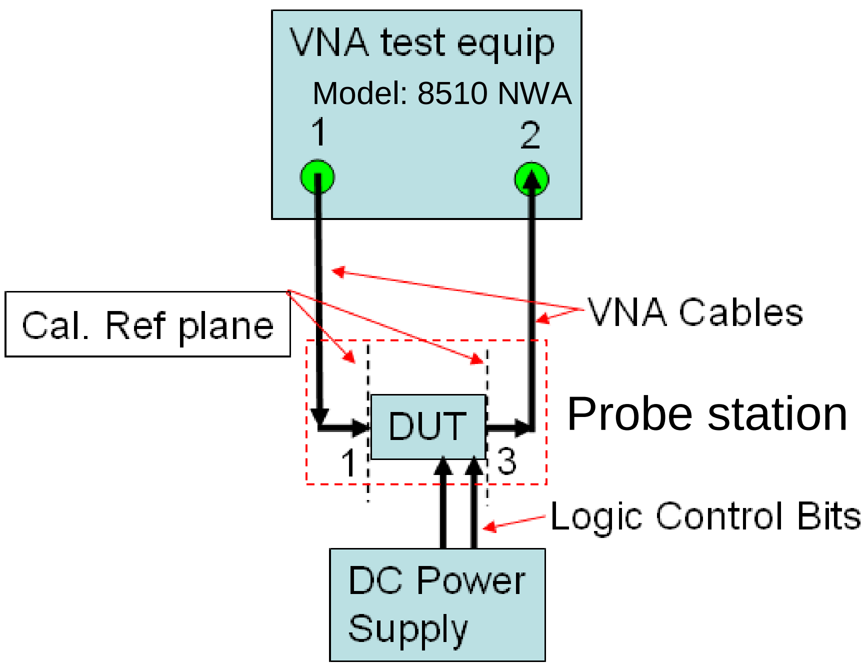

Figure 10, Test setup diagram.

5.2 RF Tests

Setup the NWA to sweep from DC (or the minimum frequency of the NWA) to 4.5GHz with 1601 pts, RF Input Power level of 0 dBm, IF BW of 5kHz, sweep time of 2 sec. Perform a full 2-Port SOLT calibration on the test setup shown in Figure 10.

5.2.1 Insertion Loss Tests

1) Connect the VNA cable attached to Port 1 of the VNA to “Port 1 of the DUT”.

2) Connect the VNA cable attached to Port 2 of the VNA to “Port 3 of the DUT”.

3) Terminate “Port 2 of the DUT” to a 50 ohm Load.

4) Turn on the DC power supply and apply the control bit command “10” to turn the Tx path “ON” and Rx path “OFF”.

5) Record the S-Parameters of the DUT into an s2p file. Save with appropriate name to indicate Tx path is “ON”.

6) Repeat step 1 with “Port 2 of the DUT”.

7) Repeat step 3 with “Port 1 of the DUT”.

8) Repeat step 4 with the control bit command “01”.

9) Repeat step 5 and save with appropriate name to indicate Rx path is “ON”.

5.2.2 Isolation Tests

1) Connect the VNA cable attached to Port 1 of the VNA to “Port 1 of the DUT”.

2) Connect the VNA cable attached to Port 2 of the VNA to “Port 2 of the DUT”.

3) Terminate “Port 3 of the DUT” to a 50 ohm Load.

4) Turn on the DC power supply and apply the control bit command “10” to turn the Tx path “ON” and Rx path “OFF”.

5) Record the S-Parameters of the DUT into an s2p file. Save with appropriate name to indicate Tx → Rx path Isolation.

6) Repeat step 4 with command “01”.

7) Repeat step 5 with and save with appropriate name to indicate Rx → Tx path Isolation.

6.0 Conclusion

A complete MMIC design for an S-Band Tx/Rx switch was presented. The specifications outlined in table 1 were met by appropriately “sizing” the pHEMT devices to compensate for input/ output mis-matches. The benefit of using sized pHEMTs allowed for broader bandwidth which is preferred for multiple RF frequency ranges. Another benefit for using this approach allowed for lower Insertion Loss since no additional microwave elements were needed. The trade-off for additional bandwidth and lower Insertion Loss was decreased input/output matching resulting in higher VSWR. All other specifications for the mixer were met as shown in Table 2 and section 3.1.2. Future improvement to this design could be to:

- Cascade frequency specific switches to improve the VSWR matching at various frequencies.
- Designing an inverter between 0V and 1V to be used in conjunction with the Logic command BIT signals so that only one control bit is necessary for controlling the Tx/Rx paths.
- Research the possibility of using different mode pHEMTs and switch topologies to reduce the switch loss while improving the VSWR performance.