S-Band Voltage Controlled Oscillator (VCO)

525.787.91 MMIC Design

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1.0 Abstract

This report details the design of an S-band voltage controlled oscillator on a Monolithic Microwave Integrated Circuit (MMIC). This design was carried out in AWR's Microwave Office but could also have been done in similar software such as Agilent's ADS. The final circuit fits on a 60 mils by 60 mils chip (or 1524 um by 1524 um) and uses components from the TRIQUINT library. To implement the VCO I used a pHEMT device with feedback to create a negative resistance circuit. I used a varactor to tune the oscillation frequency.

2.0 Introduction

This VCO was designed to be a component in the transmitter or receiver portion of a wireless communication system operating in the 2400 to 2500 MHz ISM bands. A system diagram can be seen below. The VCO is used as a tunable local oscillator for the modulator/demodulator of the system.

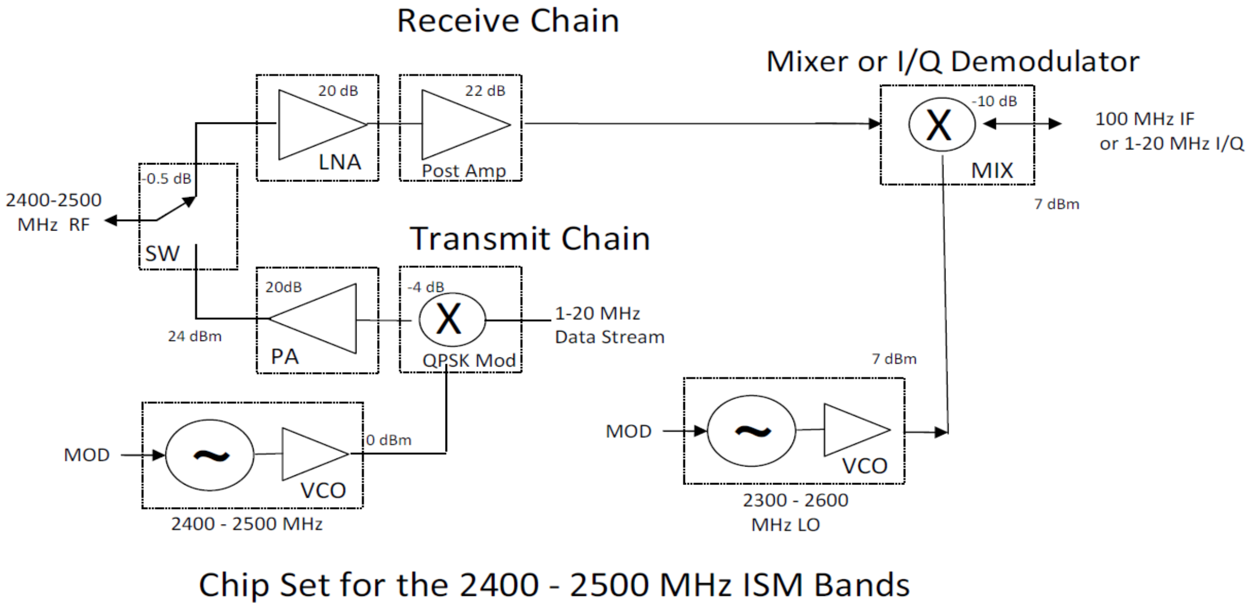


Figure 1: S-Band Communication System Diagram

To create a VCO, I started with an oscillating circuit. For the circuit to oscillate, it needs to have negative resistance. If the impedance of the circuit is $\boldsymbol{Z_N} = \boldsymbol{R_N} + \boldsymbol{j} * \boldsymbol{X_N}$ then $\boldsymbol{R_N} < 0$. If the circuit is to oscillate, the reflected waves should build on each other, so they must be in phase. This means $\boldsymbol{X_N} = \boldsymbol{0}.$ To this negative resistance circuit, I add a resonator in order to control the frequency of oscillation, as well as a matching circuit to match the negative resistance circuit to a load, which for my design was assumed to be 50 Ω (this will be looked into further in the conclusions section).

Since the resonator section of the circuit controls the frequency of oscillation, it will contain the varactor, or tunable capacitance. For the matching circuit, the impedance is $\boldsymbol{Z_L} = \boldsymbol{R_L} + \boldsymbol{j} * \boldsymbol{X_L}$. Assuming a series resonant circuit, as I did, the rule of thumb for start-up conditions of oscillation is that the magnitude of the resistance of the oscillating circuit be at least three times greater than the resistance of the load. Thus we want $|\boldsymbol{R_N}| > 3 * \boldsymbol{R_L}$ and we want any phase components to cancel so $\boldsymbol{X_N} = -\boldsymbol{X_L}$.

3.0 Design Approach

There are several different design approaches for a VCO. One popular approach includes using a Colpitts architecture for the oscillator, which uses two capacitors as voltage dividers to provide the feedback to the transistor. Similarly, the dual of the Colpitts is the Hartley, using two inductors instead of capacitors. Since this is my first attempt at designing a VCO I wanted to choose a design approach that was simple and one that was intuitive to me. The approach I used was based on tutorials and previous MMIC course VCO designs, and is described below.

Figure 2: Overall Design Approach Diagram

3.1 Design Specifications

- Tuning Frequency: S-Band from 2300 – 2600 GHz
- Supply Voltage: Battery Powered, < 3.0 – 3.6 Volts
- Tuning Voltage: 0 – 2 Volts
- Size: 60 mils by 60 mils ANACHIP

3.2 Destabilize the Transistor

The first step I took in designing the VCO was to destabilize the pHEMT to allow it to oscillate. To accomplish this I added a small resistance between the pHEMT source and ground. This adds a feedback path from drain current to gate-to-source voltage. Doing this increases S12 to greater than one, thus creating a negative resistance circuit.

I looked into using either a depletion mode or an enhancement mode pHEMT, considering current drawn, operating voltage, and bias circuits. I settled on using a depletion mode pHEMT with the benefit of an extremely simple destabilized circuit. Since there already must be a resistor between the source and ground of the pHEMT, there will be some positive voltage at the source. Since the depletion mode pHEMT can have negative gate-to-source bias, the gate of my destabilized circuit can simply be grounded. This makes the gate-to-source slightly negative, which if chosen correctly can give the correct bias. Below are the IV-curves for a D-mode pHEMT with 300 um total gate width (6 X 50).

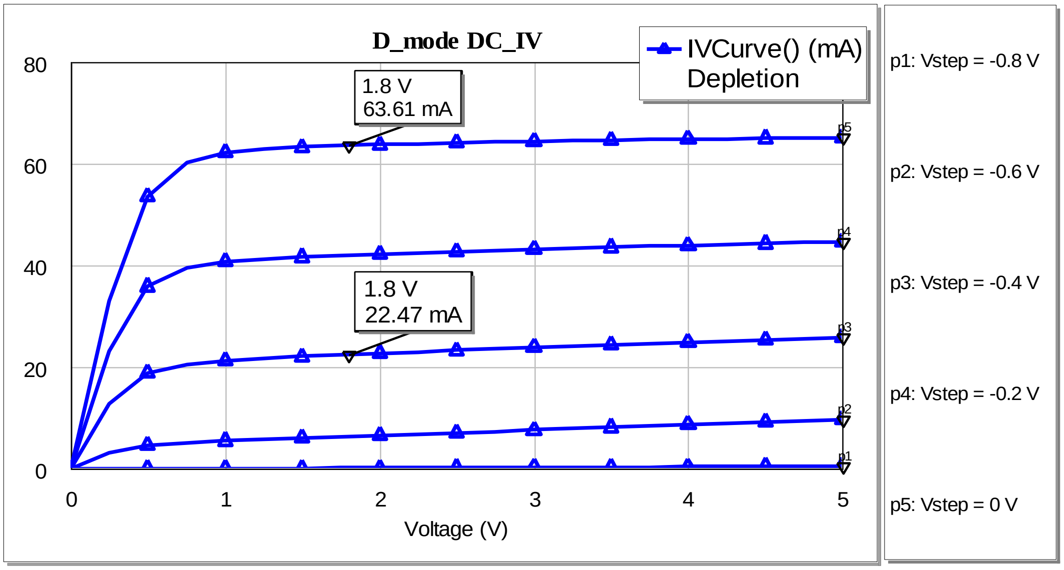


Figure 3: DC IV-Curve for 300 um gate Depletion Mode pHEMT

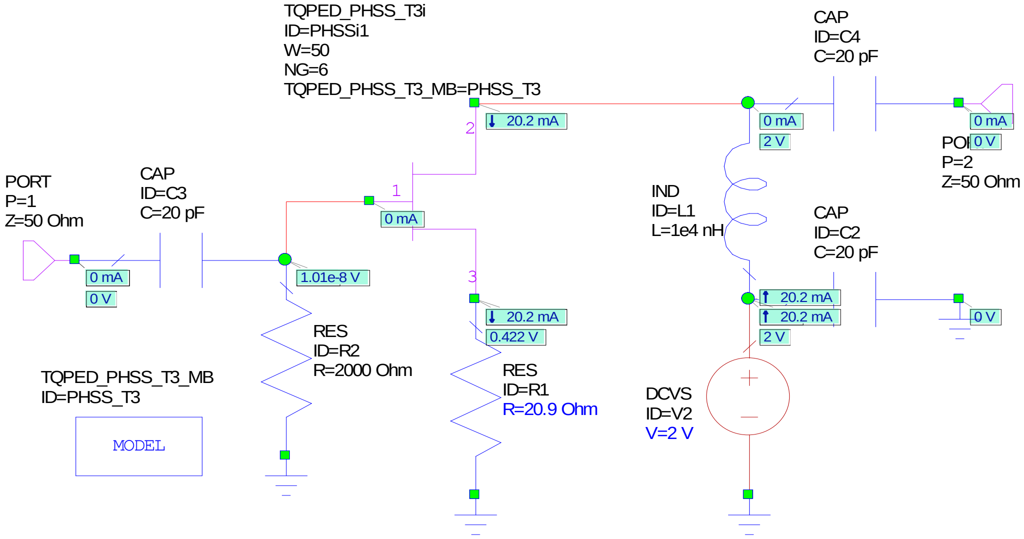


Figure 4: Destabilized pHEMT with Source Resistor and Grounded Gate

As seen from the annotated circuit above, a 20.9 Ω source resistor creates 0.422 V at the source when the pHEMT in powered with 2 Volts. With the gate grounded through a 2 kΩ resistor, the gate-to-source voltage is -0.422 Volts, which from the IV-curve draws around 20 milliamps. Also, as the simulations show in the design approach section, a 20.9 Ω source resistor provides enough destabilization for our oscillation condition at the frequency band of interest.

3.3 Varactor

As mentioned previously, the varactor is used to tune the frequency of oscillation for the circuit. In this case, I used a reverse biased diode to act as the variable capacitance for frequency tuning. To create the diode, I tied the drain and source of a pHEMT together. Then the gate is grounded and a voltage is applied to the drain as shown below.

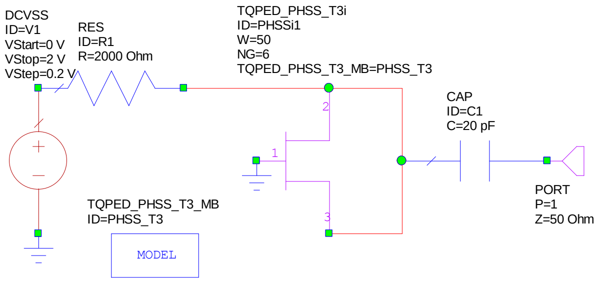


Figure 5: Varactor Circuit

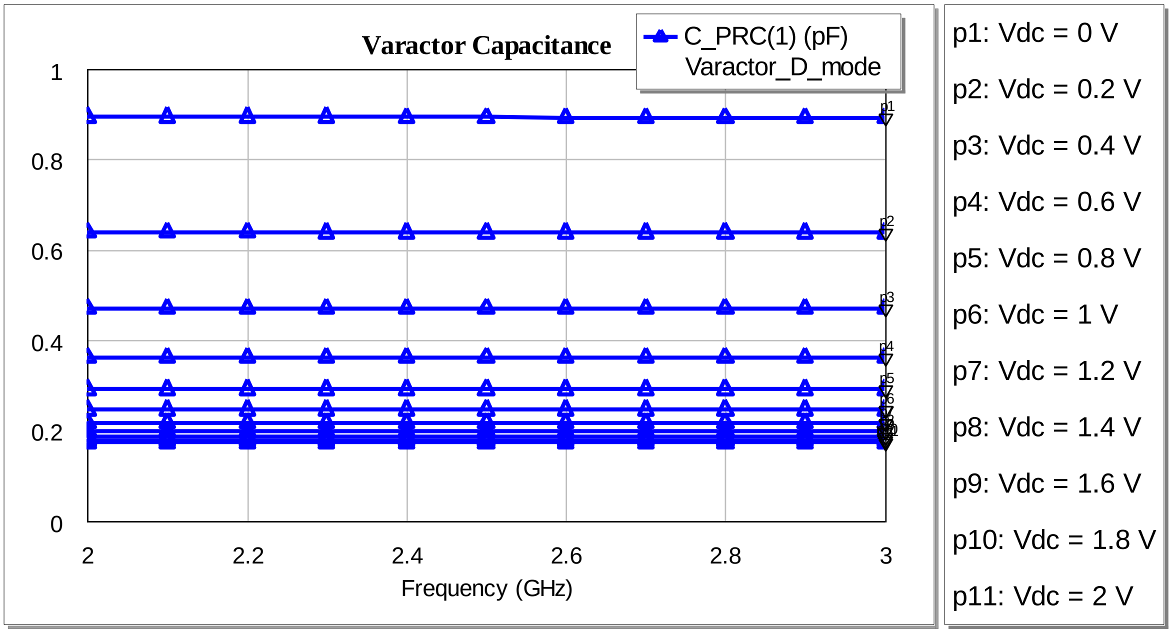


Figure 6: Varactor Capacitance across 2 Volt tuning voltage

In the varactor circuit, a 2kΩ resistor is placed between the power supply and the diode since it draws little current. Also a large capacitor is placed at the port to block the DC component from getting to the rest of the circuit. In the capacitance graph, the varactor's capacitance varies between about 0.2 and 1.9 pF with an input voltage range of 0 to 2 volts, but has little variation between 1.6 and 2.0 volts.

3.4 Tune Gate and Drain Circuits

The goal in adding the gate and drain circuits is to maximize the magnitude of the reflection from the oscillating circuit, and to bring the phase to 0. Initially, ideal transmission lines are placed at the gate and drain, and then replaced with inductors and capacitors as needed. As the simulations show in the next section, the gate transmission line can be replaced with a single inductor. To replace the drain transmission line, I used the lumped element equivalent low pass pi network. The circuit is shown below with both ideal transmission lines and their equivalent lumped element circuit.

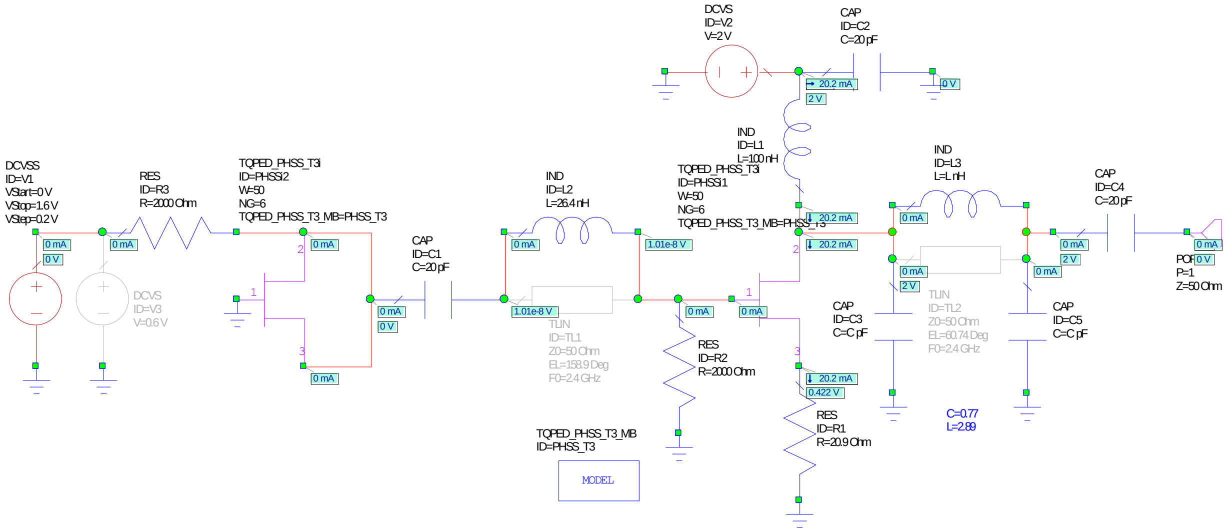


Figure 7: Full Destabilized Active Circuit

3.5 Matching Circuit

With the varactor and gate and drain transform circuits added, the active portion of the circuit is complete. The next step is to design a matching circuit, to match the active circuit's impedance to a 50 Ω load, to ensure oscillations can start up. Note that I designed the matching circuit for a 50 Ω load, but since this VCO is designed to fit into a system, the matching circuit could be designed for whatever load it will be connected to, in order to transfer maximum power from the VCO to the rest of the system.

As the simulations will show, the full active circuit has a resistance of about -25 Ω. This means the matching circuit should have a resistance of 8.3 Ω according to the equation $|\boldsymbol{R_N}| > 3 * \boldsymbol{R_L}$.

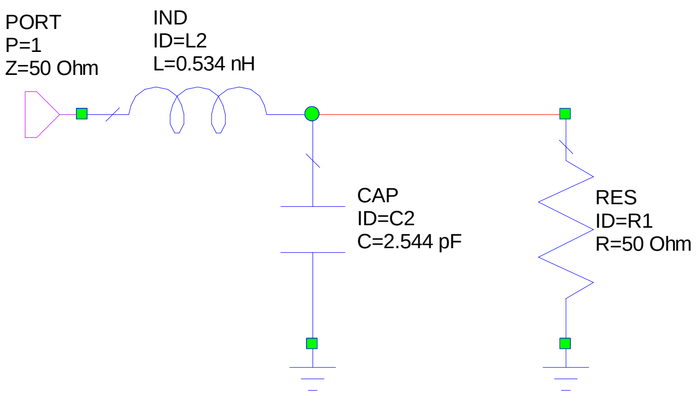


Figure 8: Matching Circuit

3.6 Replace Ideal Elements with TRIQUINT Elements

Once the matching circuit was added, and the VCO circuit was complete, the ideal elements were replaced with TRIQUINT elements one by one. Since the TRIQUINT capacitors and resistors are fairly close to the ideal model, they can be replaced with little impact on the overall simulation. However TRIQUINT inductors have a fair amount of loss associated with them compared to ideal ones, so more care must be taken in replacing them. For each inductor in my circuit, I checked the S-parameters for that section of the circuit when an ideal inductor was used. Then I replaced it with a TRIQUINT inductor and added shunt or series capacitance or inductance to tune the circuit as close to the original as possible.

In addition, it is convenient to have a shunt inductor in the drain circuit, as this is an ideal place to connect the DC power. With this in mind, I replaced the low pass pi network with two shunt inductors and two series capacitors by matching S-parameters.

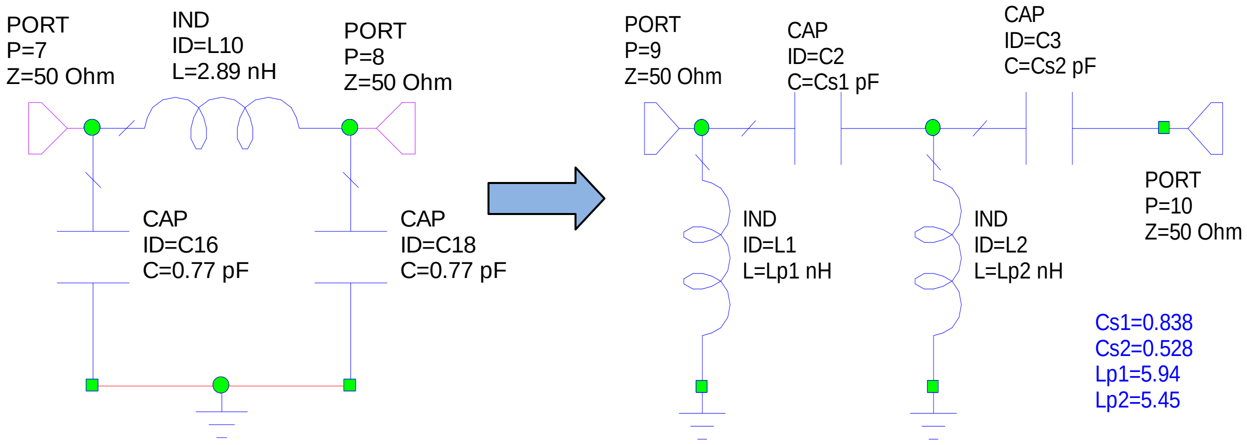


Figure 9: Tuned Equivalents for Drain Circuits

4.0 Simulations

This section will show the key simulations done throughout the design of the VCO.

4.1 Destabilized Transistor

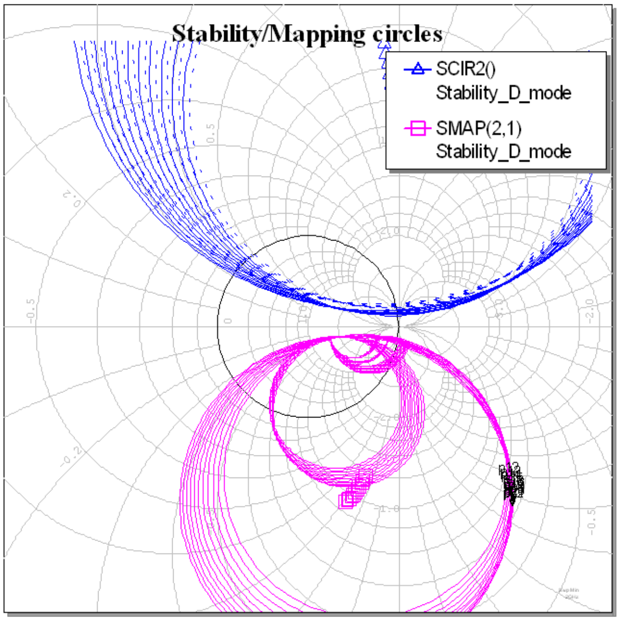


Figure 10: Stability and Mapping Circles for Destabilized pHEMT

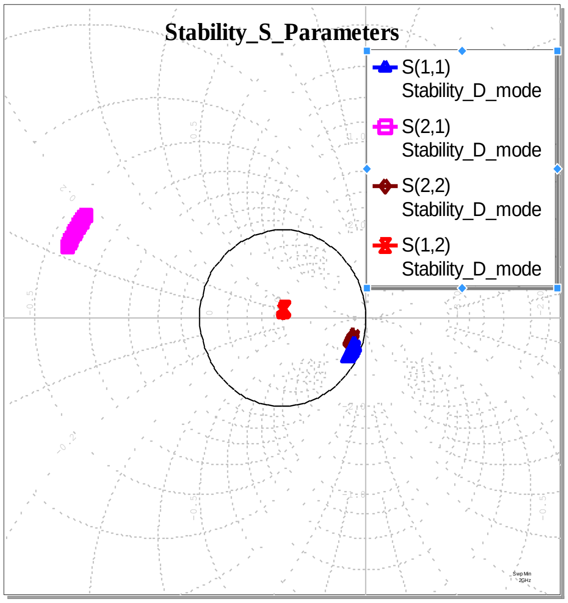


Figure 11: S-Parameters for Destabilized pHEMT

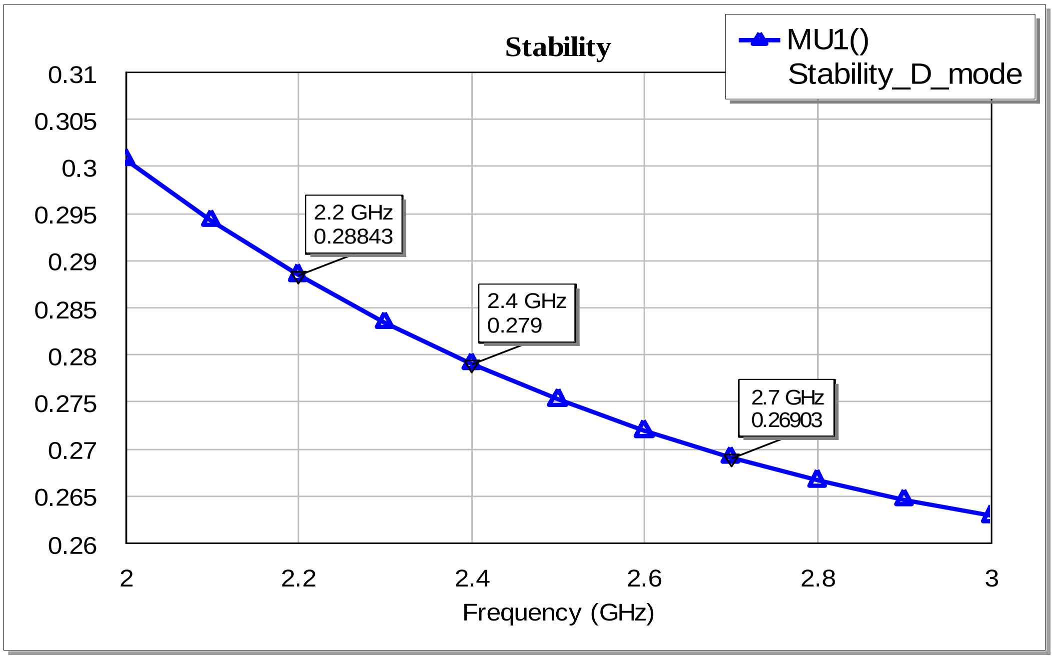


Figure 12: Load Stability Factor (Mu) for Destabilized pHEMT

Above are the simulations for the destabilized pHEMT using a series resistor between source and ground. From the S-parameters, the circuit has gain since S21 is clearly greater than one, but it still must be rotated into the unstable region shown in the stability circles. From Figure 9, the de-stable region for the circuit covers a large portion of the top half of the smith chart. Also the mapping circles are fairly large in magnitude. To check the maximum point on the output mapping circle, since MWO doesn't have a specific measurement for it, I use the load stability factor, Mu1. The inverse of this is the maximum output mapping circle. Going by the rule of thumb stated earlier, I am shooting for the maximum output mapping circle value to be three or greater. From the stability factor plot, Mu1 at 2.4 GHz is 0.279, with an inverse of 3.58, which is comfortably greater than 3. From this we see the 20.9 Ω source resistor will satisfy our start-up conditions for oscillation.

4.2 Gate and Drain Tuning

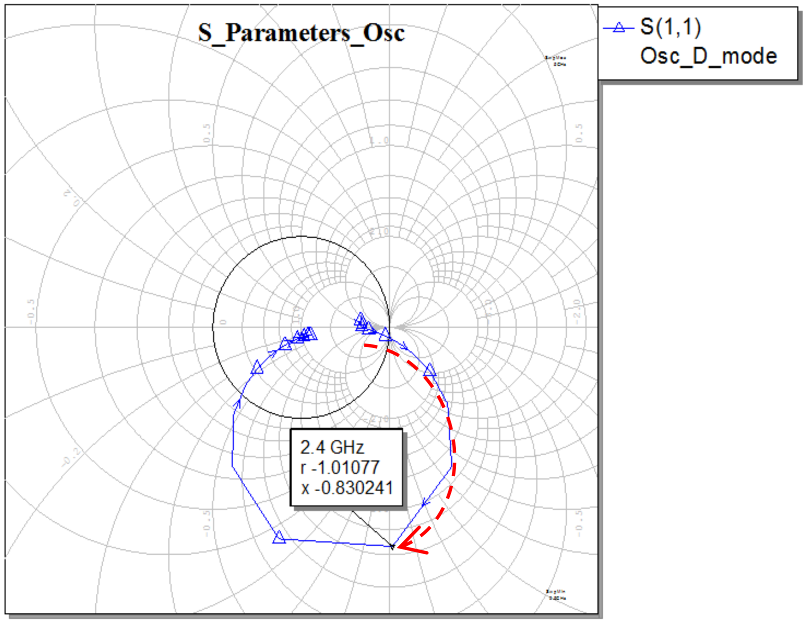


Figure 13: S11 for Destabilized pHEMT with Varactor and Gate Transform

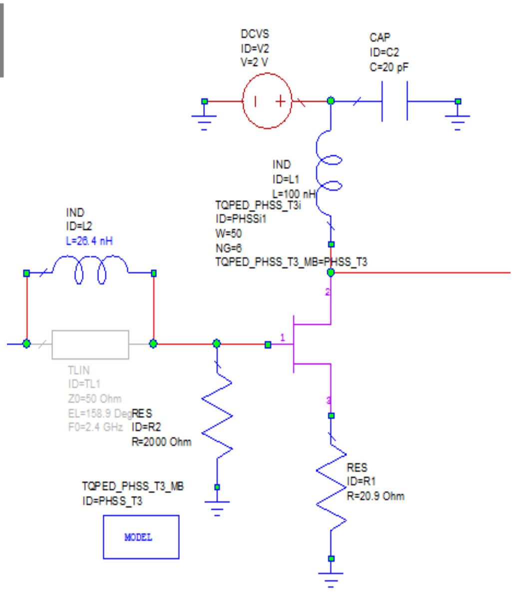


Figure 14: Destabilized pHEMT with Gate Transform

First the gate transform was tuned. Using the destabilized pHEMT circuit with the varactor and gate transmission line added, the reflection S11 was ploted. The gate transmission line was then tuned to get maximum magnitude. I then replaced the ideal transmission line with an inductor, tuning it to give approximately the same magnitude S11.

Next, an ideal transmission line was placed on the drain of the pHEMT to transform S11 so the reactive part of the impedance is zero. As shown in the figure below, the transmission line swings S11 around to the real axis of the smith chart.

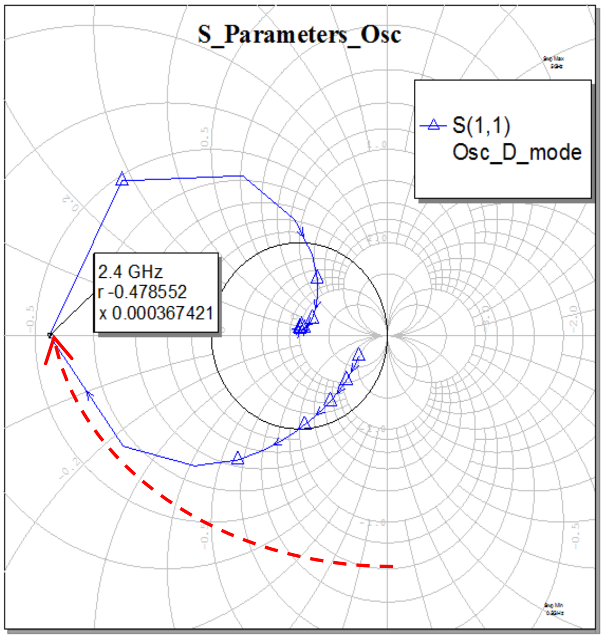


Figure 15: S11 for Destabilized Circuit with Gate and Drain Tuned

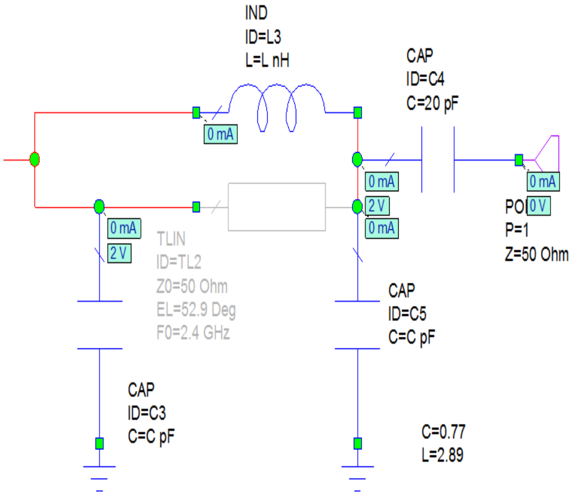


Figure 16: Drain Transform section added to Circuit

Once the correct length transmission line was found, I found the lumped element equivalent circuit using a low pass pi network.

With the gate and drain circuits added, I run a simulation to check the reflection at port 1 across a sweep of tuning voltages applied to the varactor. As seen below, each tuning voltage has a peak at a different frequency. The peaks are above one, which means it has the potential to oscillate. On the same graph is the angle of S11. The fact that the angle is -180 degrees at each of the peaks of S11 shows that the circuit will indeed oscillate at the frequency. Also note that the magnitude of the peaks slowly decreases as frequency increases. This inconsistency is fixed to a degree when the matching circuit is added.

Also below is the impedance of the oscillating circuit. As discussed in the design section, the matching circuit was designed based on the equation, $|\boldsymbol{R_N}| > 3 * \boldsymbol{R_L}$ given that $\boldsymbol{R_N} \cong \boldsymbol{-25}$.

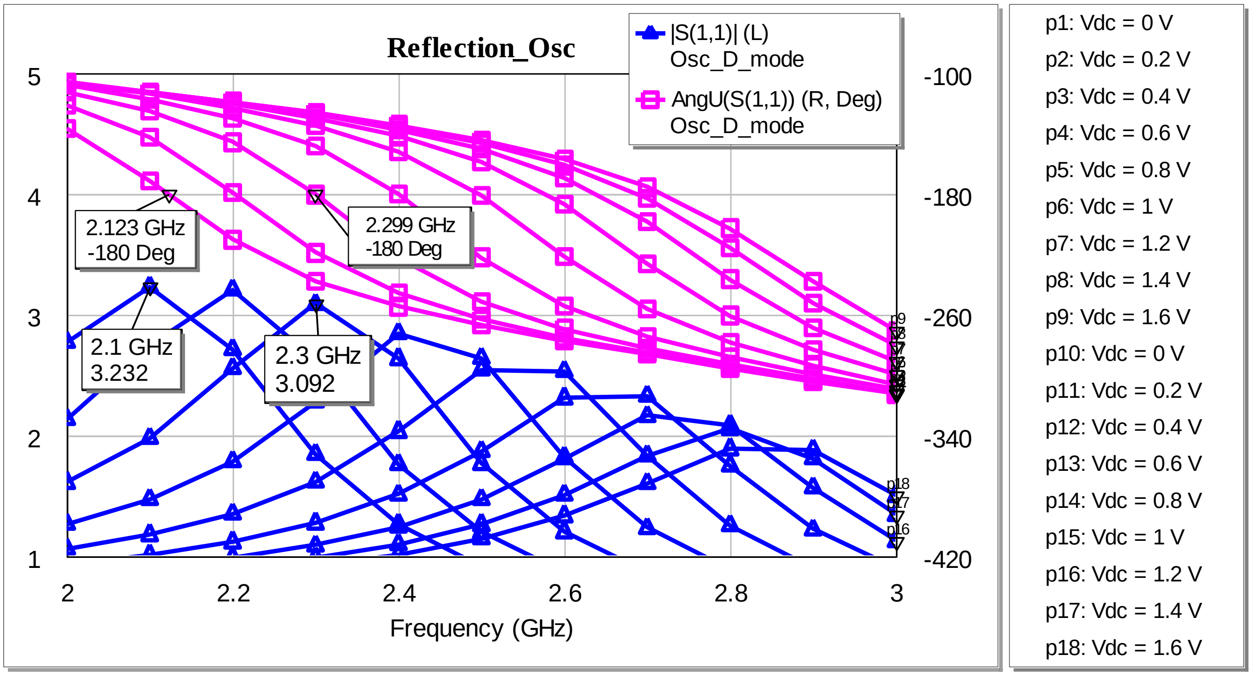


Figure 17: Magnitude and Angle of S11 for the Completed Active Circuit

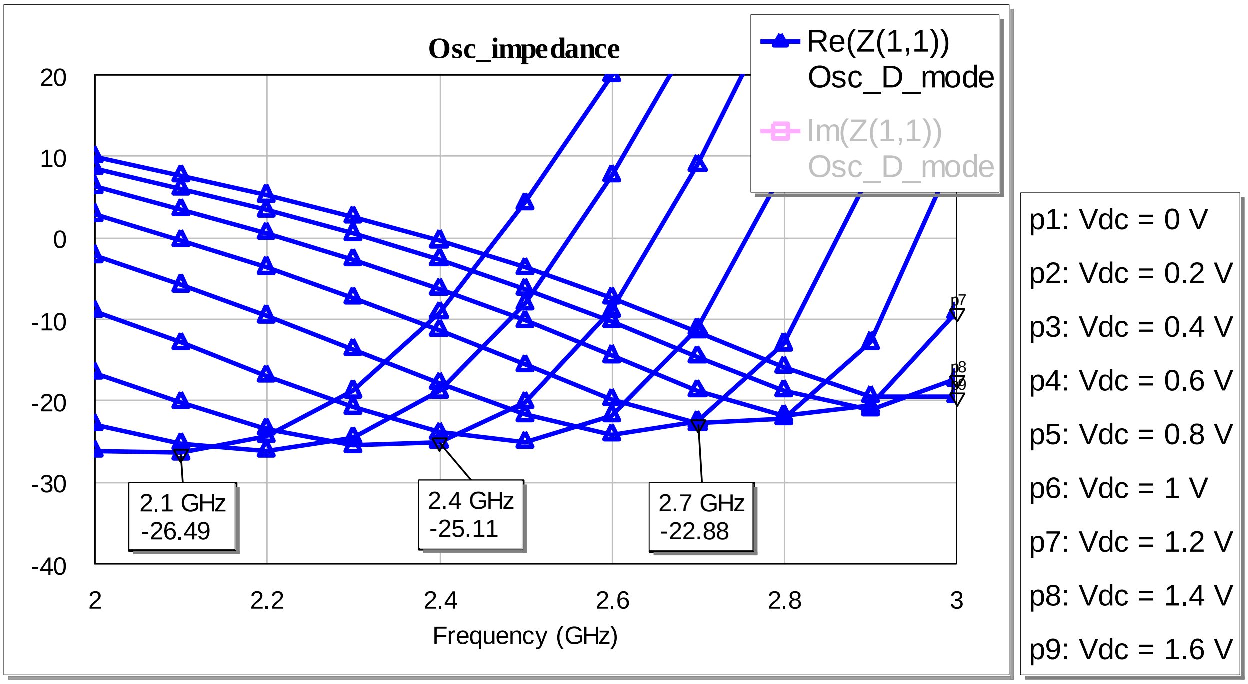


Figure 18: Real Component of Impedance for the Completed Active Circuit

4.3 Complete VCO Circuit: Active Negative Resistance Circuit with Matching Circuit

Below is the magnitude plot of S11 for the TRIQUINT element VCO circuit. A zoomed in plot is shown to see the magnitudes of the peaks while a wider frequency range plot is shown to verify that no out of band oscillations occur. Outside the 2 to 3 GHz range the magnitude S11 stays below 1.

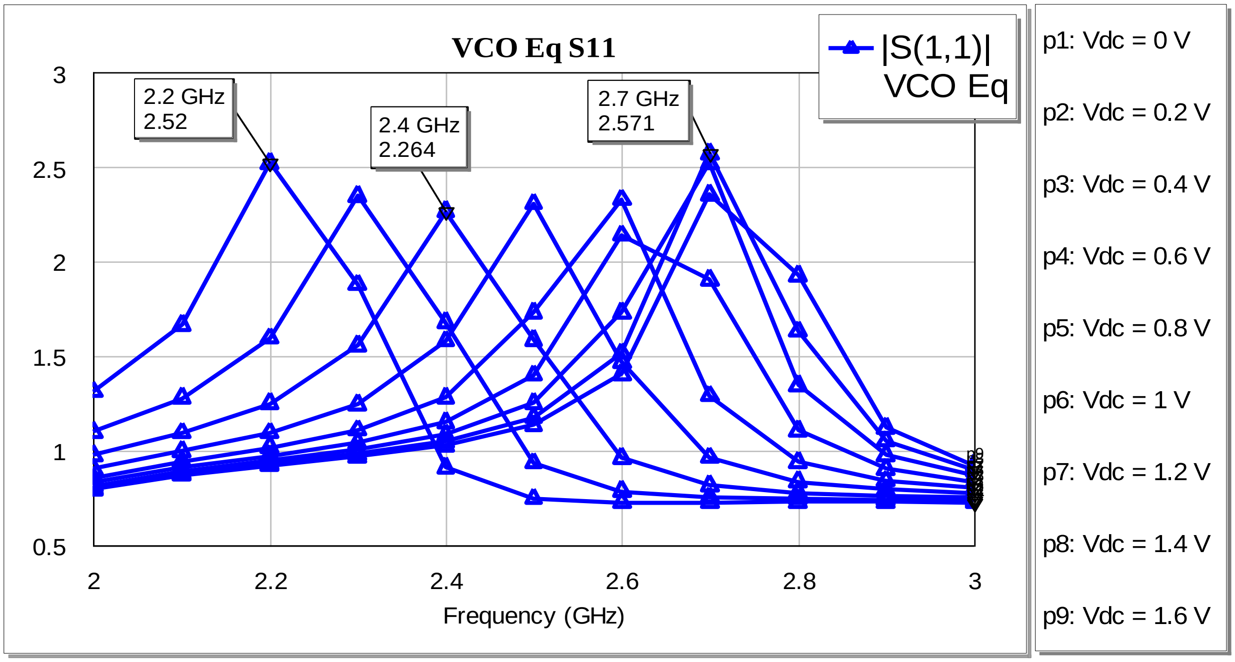


Figure 19: Magnitude of S11 for TRIQUINT Element VCO Circuit Frequency Range 2 – 3 GHz

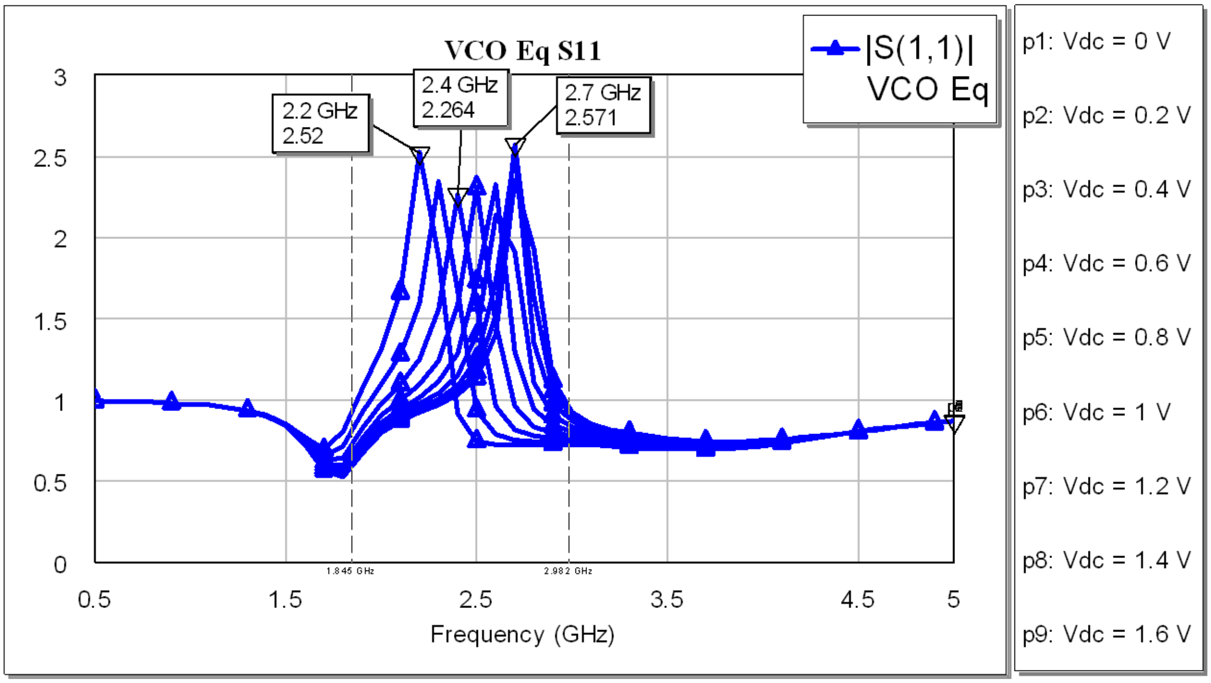
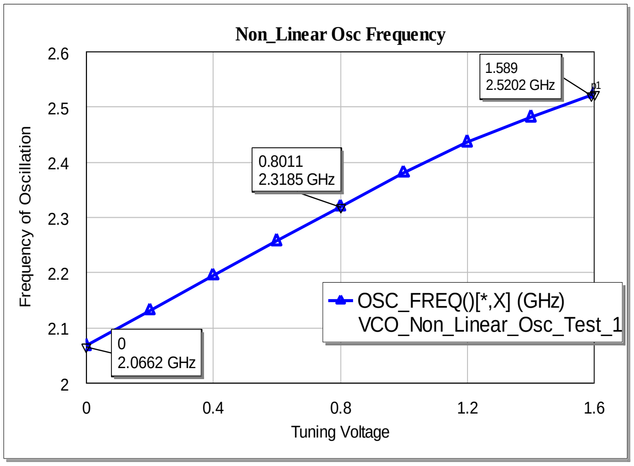


Figure 20: Magnitude of S11 for TRIQUINT Element VCO Circuit Frequency Range 0.5 – 5 GHz

4.4 Non-Linear Simulations

In addition to the linear measurements such as S-parameters and impedance, MWO also has the ability to do non-linear simulations. Specifically, with an element called OSCAPROBE, things such as oscillation frequency, power spectrum, and phase noise can all be measured. Interestingly, the oscillation frequency determined from non-linear simulations is slightly off from that determined by the S11 peaks. In fact all frequencies seem to be shifted down by about 0.2 GHz. This could be due to frequency drift while the oscillations are first beginning until they saturate at steady state. Below are graphs of oscillation frequency vs. tuning voltage and phase noise. Phase noise is below -111 dBc for frequencies of 1 MHz or more offset from the oscillating frequency.



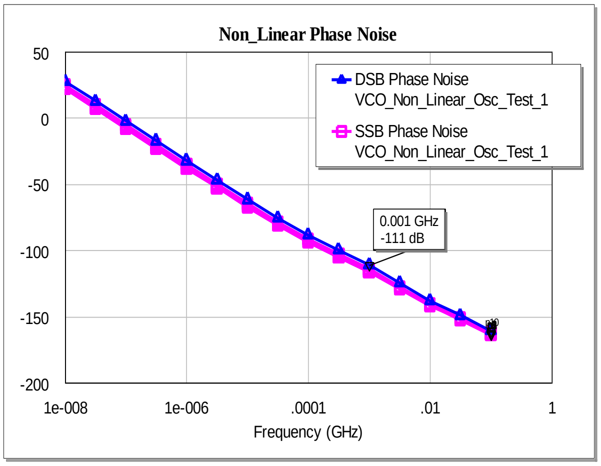
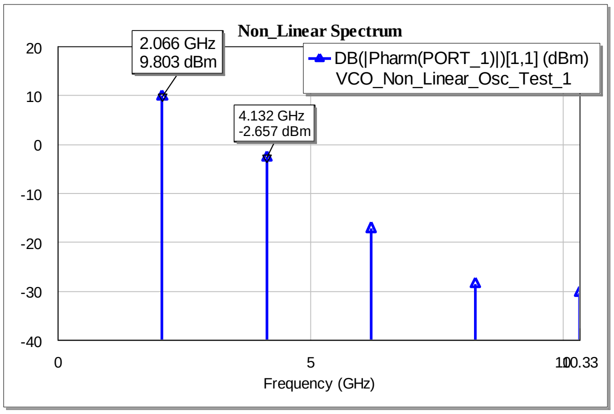


Figure 21: Non-Linear Simulation of Tuning Voltage vs. Osc. Freq

Figure 22: Non-Linear Simulation of Phase Noise



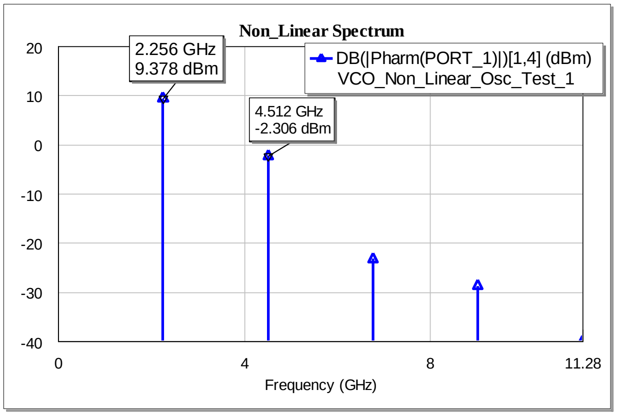


Figure 23: Power Spectrum for Tuning Voltage = 0 V

Figure 24: Power Spectrum for Tuning Voltage = 0.6 V

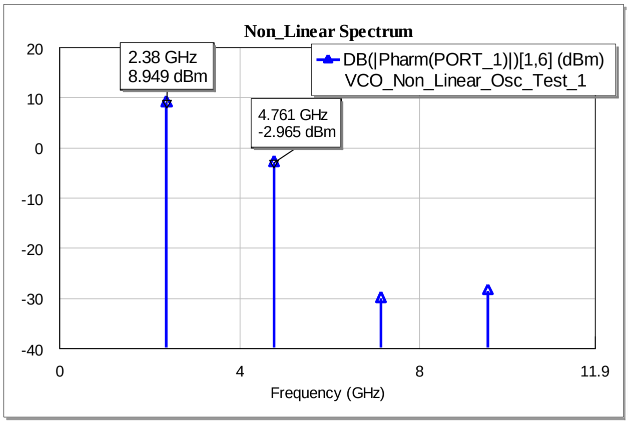


Figure 25: Power Spectrum for Tuning Voltage = 1.0 V

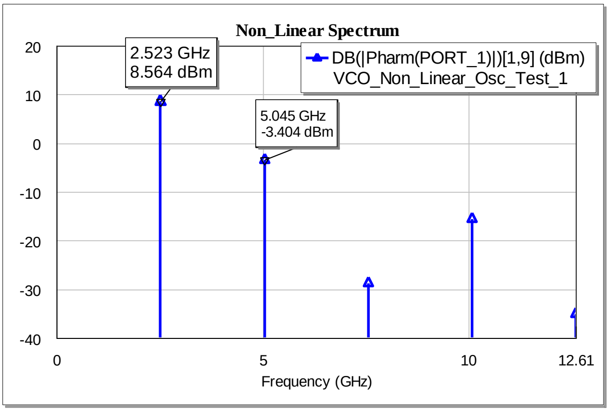


Figure 26: Power Spectrum for Tuning Voltage = 1.6 V

Shown above are the power spectrums for various tuning voltages. As seen in the simulations, the output power of the first harmonic varies between 9.8 and 8.56 dBm, decreasing as frequency is increased. Also note that the second harmonic has a power level of around 12 dB less than that of the first harmonic.

5.0 Final Circuit Schematic

The final S-band VCO circuit schematic is shown below. It is also annotated with voltages and currents at each node in the circuit. For comparison, I have also included a DC equivalent circuit, where all of the inductors are replaced with wires.

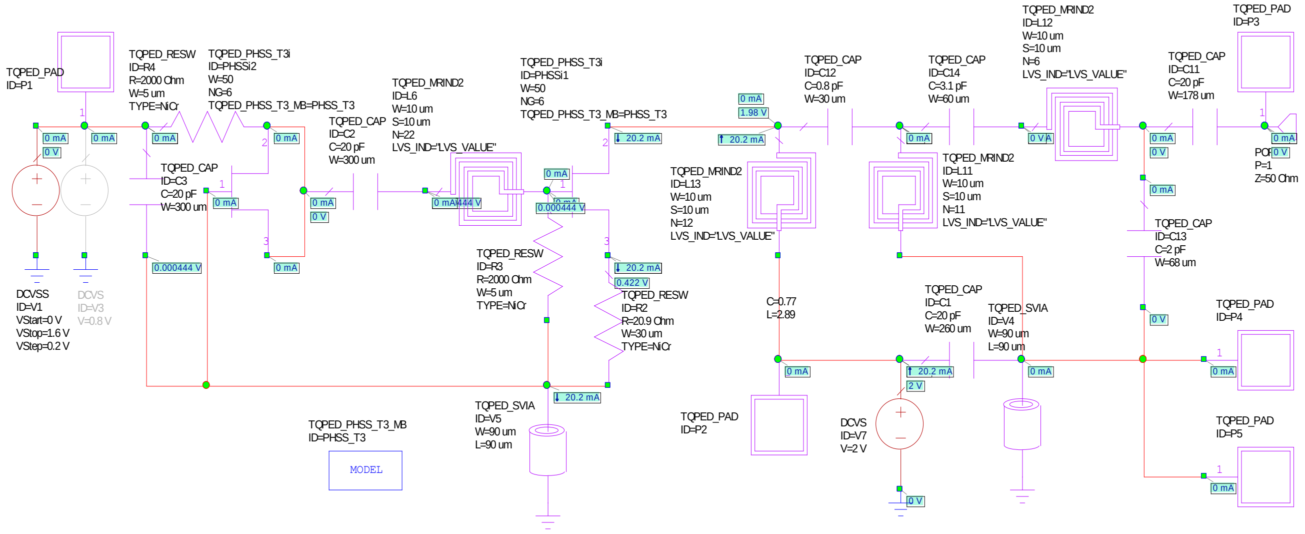


Figure 27: Final VCO Circuit Schematic

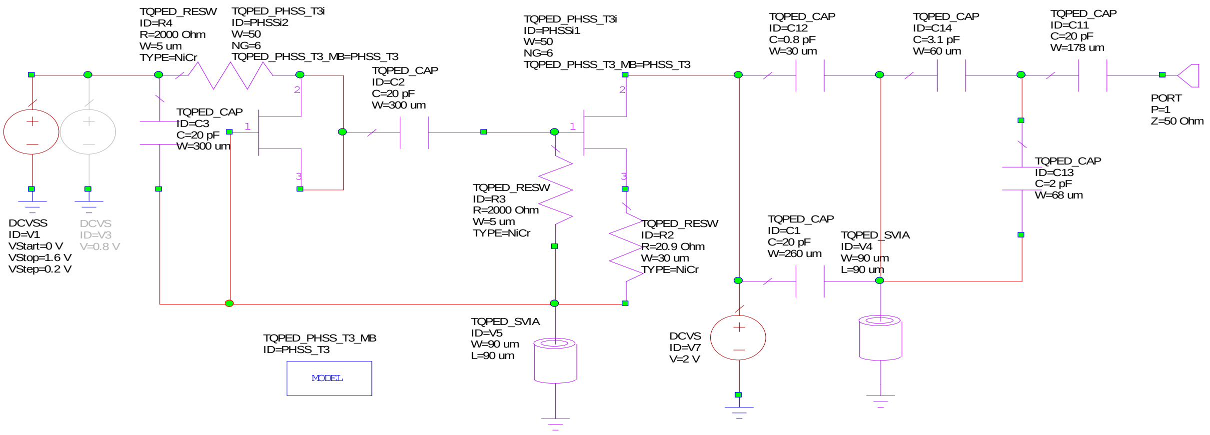


Figure 28: Final Circuit, DC Equivalent Schematic

6.0 Layout Plot

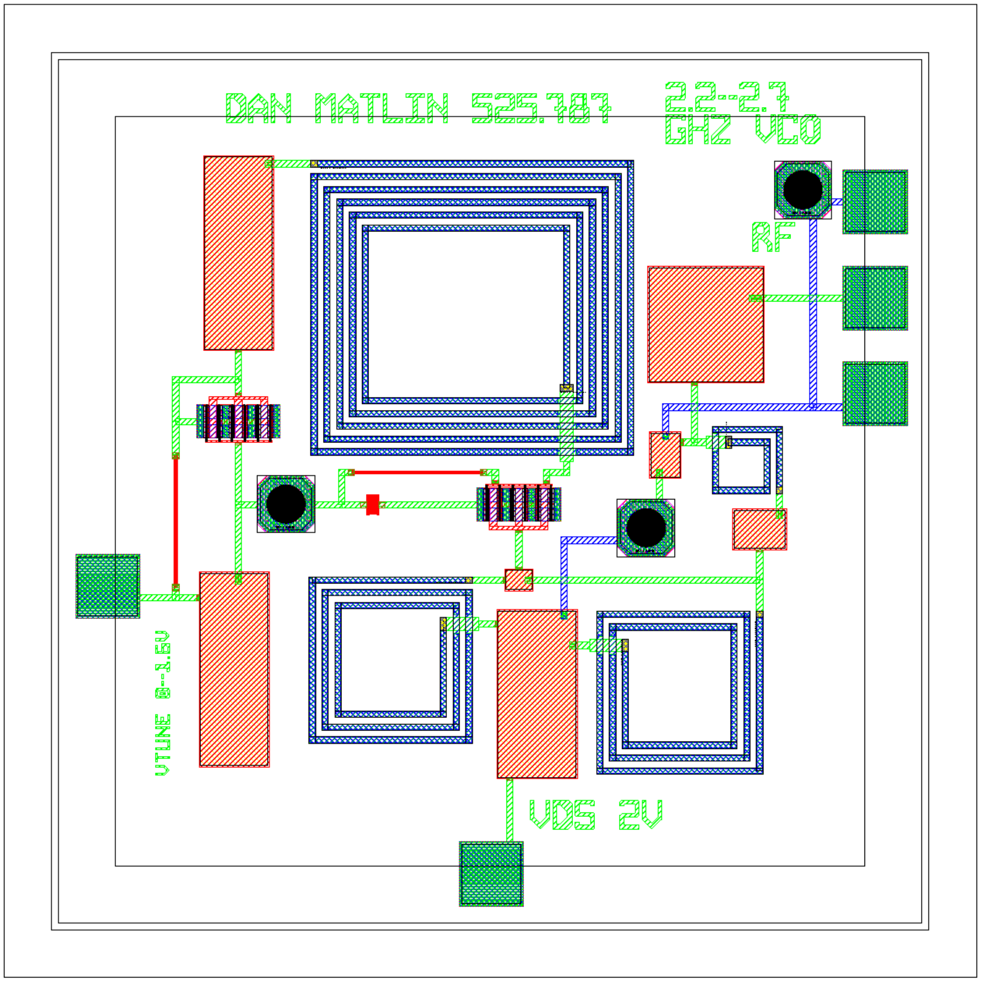


Figure 29: Final VCO Layout Circuit

The layout, like the schematic, was done in AWR's Microwave Office. Effort was taken to make the design reasonably compact to minimize the interconnect path lengths. For our stack-up, we have 3 metal layers available to us, metals 0, 1, and 2. Metal 0 is 0.5 um thick, while metal 1 is 4 times as thick at 2 um, and metal 2 is thicker still at 4 um. Most of the interconnect was done in metal 1, using metal 2 when needed to cross over an existing interconnect.

7.0 Test Plan

Once fabricated, this VCO circuit will be tested at the Johns Hopkins Dorsey center using equipment available in lab. On the circuit itself, there are five pads total for probing. Two of these pads are for DC supply, while the other three are ground-signal-ground for the RF signal generated by the circuit. For the tests that follow, two DC probes and one RF probe will be needed.

7.1 DC Check

As the initial check, the circuit should be tested to ensure there are no direct shorts to ground. Before power is supplied to the circuit, check that the "Vtune", "VDS", and RF signal pads are not shorted to ground.

Next, use a DC power supply and a single probe to supply the "VDS" circuit pad with +2.0 volts. With the power supply connected, measure the current being drawn by the circuit. The circuit should draw approximately 20 mA.

7.2 Oscillation Check/Analysis

With the chip still connected to +2.0 volts, connect the "Vtune" pad to an initial value of 0 volts. Using the RF probe, connect the RF pads to a spectrum analyzer. Set the spectrum analyzer to a frequency range of 1.5 – 3 GHz. Use the spectrum analyzer to determine the center frequency of oscillation for a tuning voltage of 0 volts. The oscillation frequency for 0 volts should be between 2.0 and 2.2 GHz (depending on the correctness of the linear/non-linear simulators). Using the spectrum analyzer, check the output power of the oscillating frequency. The power should be around 9.8 dBm or 9.5 mW. Perform the same oscillation frequency and power output measurements for various tuning voltages in the range of 0 – 1.6 volts. As frequency is increased, output power will decrease slightly, with a minimum of around 8.5 dBm or 7.08 mW.

Next, widen the spectrum analyzer's frequency range to 0.5 – 5 GHz to check for any out of band oscillations.

8.0 Summary and Conclusions

This report has detailed the design of an S-band Voltage Controlled Oscillator on a 60 mils by 60 mils MMIC chip. This particular design used AWR's Microwave Office for circuit simulations. The results of these simulations show that an S-band VCO can be fabricated on a compact chip using less than 3.0 volts to produce a tunable signal with approximately 9.5 mW of output power. A tunable frequency range of approximately 0.5 GHz is achievable with a tuning voltage of 0 – 1.6 volts. The main goal of fabrication is to verify the simulated results obtained throughout this design with experimental measurements.

While this VCO design was tuned for the best performance given the time constraints, it is certainly not perfect and there is always room for improvement. For example, with the interconnect added on the layout of the chip, the performance changes slightly. While this is not a major change, it would be helpful to tune out some of its effects, which I did not have time for in this project. Also, the fact that this device is supposed to fit into a larger system must be taken into account. Even though there wasn't enough time, the VCO could be optimized for the components it would be connected to in the system, namely the QPSK modulator or mixer/demodulator. In order to do this, the S-parameters for that component would be needed. Then, the VCO's matching circuit could be designed for the impedance of the component it will be connected to instead of 50 ohms.