

C Band MMIC LNA (Low Noise Amplifier)

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Project prepared for Microwave Monolithic Integrated Circuit

(MMIC) Design

Fall 2004 Class

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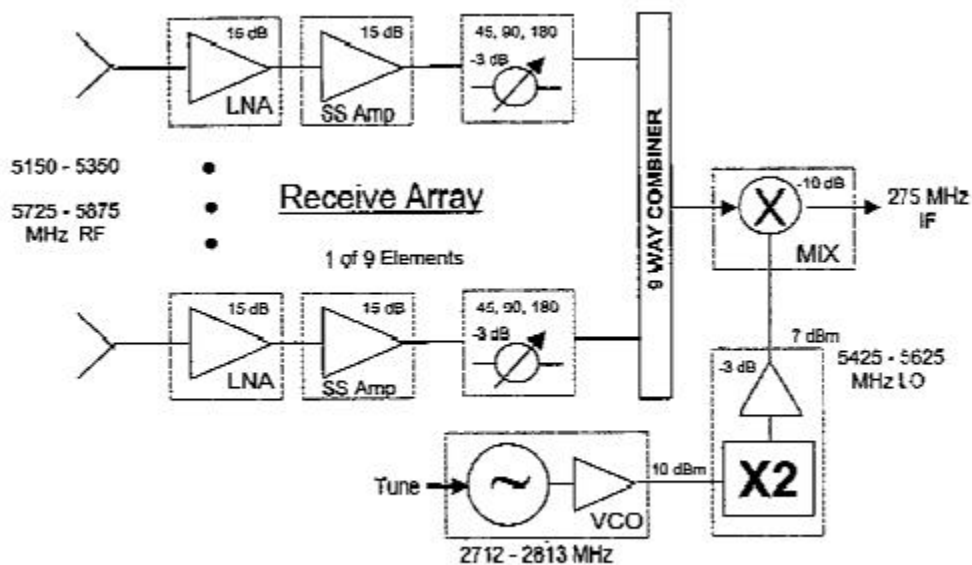
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Introduction

Low Noise Amplifiers (LNAs) are very important part of the receive chain in a microwave system. It is essential that a signal be amplified early in the receive chain while adding as little noise as possible because any noise injected by these components in a system is amplified by later stages along with the desired signal.

For this application, the C-Band Low Noise Amplifier will be the first device in the receive chain for the 2004 MMIC class design at The Johns Hopkins University. The project is a duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial scientific, and medical (ISM) frequencies. This LNA will be one of nine MMIC designs that make up the S Band Transceiver.

System Block Diagram: Figure 1.1



LNA Design Specifications

Frequency:	5150 to 5875
Bandwidth:	>800 MHz
Gain:	>15 dB
Gain Ripple:	± 0.5 dB goal
Noise Figure:	<4dB; 3dB goal
VSWR, 50 ohm:	<1.5:1
INPUT IP3:	>+5 dBm
Supply Voltage	± 5 Volts; 5 Volts only, goal
Size:	60 x 60 ANACHIP

Methodology of LNA Design:

Upon beginning this design, the gain and noise figure specifications were sought after first and then compromises were made to adjust the design accordingly to meet the other design specs. This LNA was designed to be a two-stage amplifier. Although it is possible to get substantial gain out of one stage of amplification, a one stage FET amplifier would probably have stability problems and be very hard to meet the VSWR spec because of the attenuation required to match the input and output. After being able to achieve the lowest noise figure attainable with considerable RF gain, another stage of amplification was added and tradeoffs were made to match the input and output of the circuit with the assumption that changes to S22 will not significantly affect S11.

Design tradeoffs:

Since there is always an emphasis on noise figure (NF) in a LNA design, it was preferred not to use any resistors in the first matching network of the design. Practical design techniques also make it less desirable to use large noisy inductors at the front end of an LNA, and therefore only one series inductor and a shunt capacitor were used to match the input of the FET. The result of that was a respectably low noise figure but a narrow bandwidth match at the input.

Another tradeoff with the LNA design was the gain roll off point vs. the VSWR of the design. It is very possible to have the gain roll off for the LNA to happen further away from the desired operating frequency of the design, however in doing that, the narrow band input match of the circuit moves in the opposite direction. Unfortunately the input matching network forms a low pass filter at the input of the circuit and the performance at the output directly correspond to the IMN.

Circuit Performance:

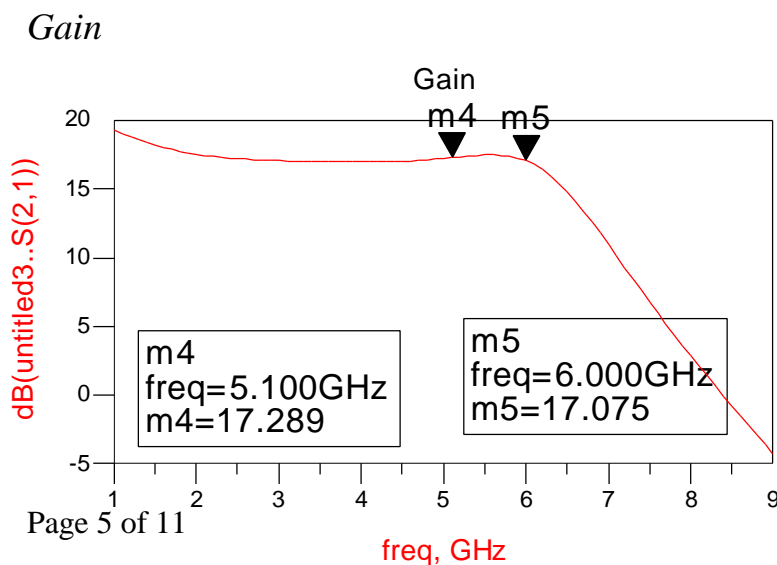


Figure 5.1

Noise Figure:

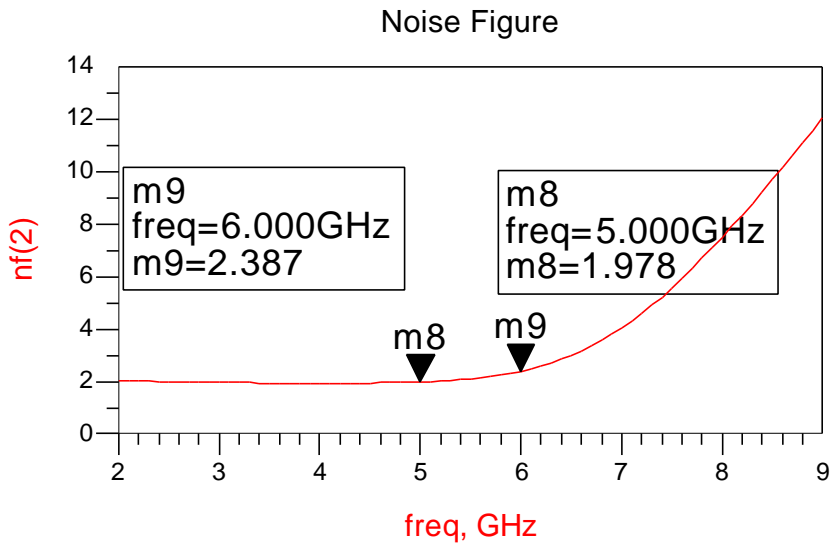


Figure 5.2

Input/Output Match

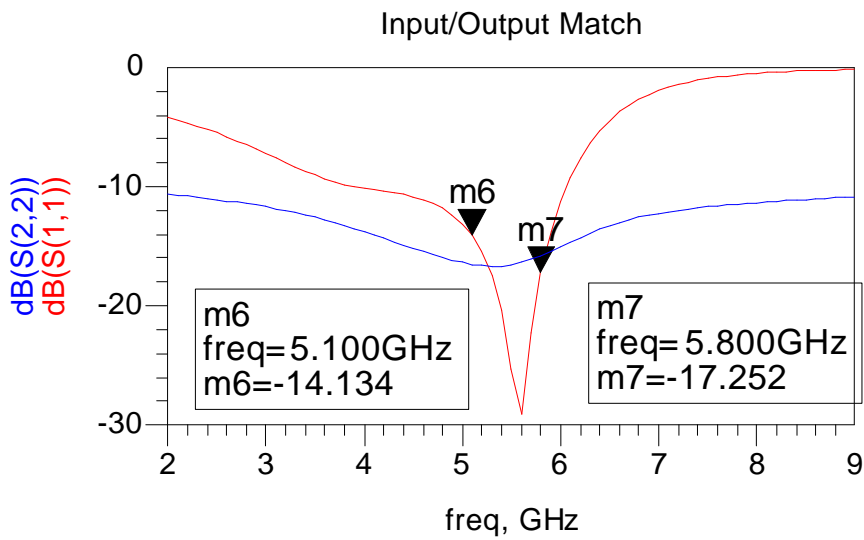


Figure 5.3

IP3

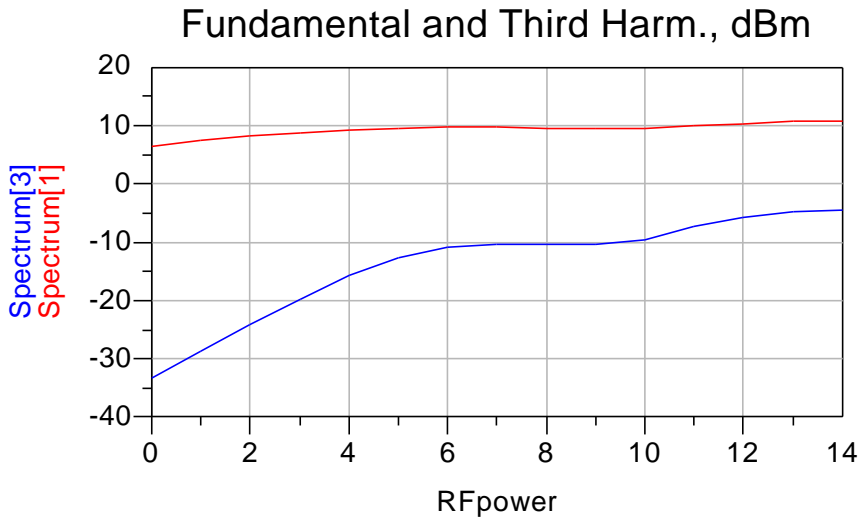


Figure 5.4

Design Specifications Vs Circuit Performance

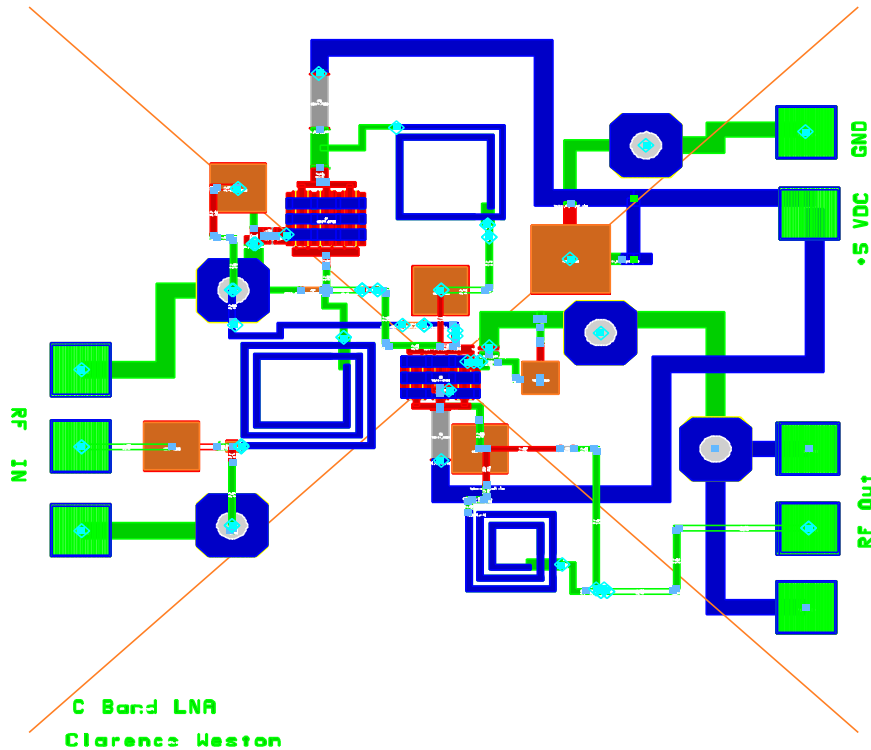
	Design Specifications	Simulated Performance
Frequency:	5150 to 5875	5150 to 5875
Bandwidth:	>800 MHz	>800 MHz
Gain:	>15 dB	>17 dB
Gain Ripple:	+0.5 dB	>0.5 dB
Noise Figure:	<4dB; 3dB goal	<2.3dB
VSWR, 50 ohm:	<1.5:1	<1.5:1
INPUT IP3:	>+5 dBm	>+15 dBm
Supply Voltage	+5 Volts; +5V Goal	+5
Size:	60 x 60 ANACHIP	60 x 60 ANACHIP

Drawbacks of LNA Design:

This Low Noise Amplifier (LNA) design shows a low tolerance for component variations especially at the input side of the amplifier. The lowpass type input matching network yields a practically flat gain response from 2 to 6 GHz, however the gain rolloff is very steep thereafter. The noise figure data also follows that trend, worsening continually shortly after the design frequency.

The flat gain response is helped to be achieved through the use of a small feedback capacitor from the input of the first FET to the input of the second stage. This capacitor helps with stability issues, tunes the high frequency rolloff point but unfortunately is also very sensitive to value tolerances. Also, because only two components were used to match the input side of the LNA, the IMN is very narrow band, that just covers the design bandwidth and without precise fabrication, it is very possible to miss the design frequency and end up with a relatively large mismatch at the front end.

LNA Layout:



Design Summary/Conclusion:

The specifications for this LNA design were challenging but achievable. There were many tradeoffs in the consideration for this design. Two of the more desirable features of this LNA is the flat gain response and broad band output match form 2 to 6GHz makes this design a very portable one in the since that an off chip tunable inductance at the input can have this amplifier operate over and 1GHz band of that 4GHz bandwidth.

Test Equipment

- 5 Volt DC Power supply
- Noise Figure Meter
- Agilent 8510 Vector Network Analyzer

Test Procedure

Turn On Procedure:

Connect the DC power supply to the DC pads on the MMIC. Slowly increase the voltage from 0 to 5 volts. (The amplifier should be drawing about 45mA.)

S-Parameter Measurement:

Calibrate the Network Analyzer from 1 to 10 GHz.

Position the input probes on the 'RF IN' GSG pad on the chip.

Position the output probes on the 'RF OUT' GSG pads on the chip.

Make all S-Data measurements and save them to a disk.

Noise Figure Measurements:

Calibrate the noise figure meter from 1 to 10 GHz.

Position the input probes on the 'RF IN' GSG pad on the chip.

Position the output probes on the 'RF OUT' GSG pads on the chip.

Make all S-Data measurements and save them to a disk.