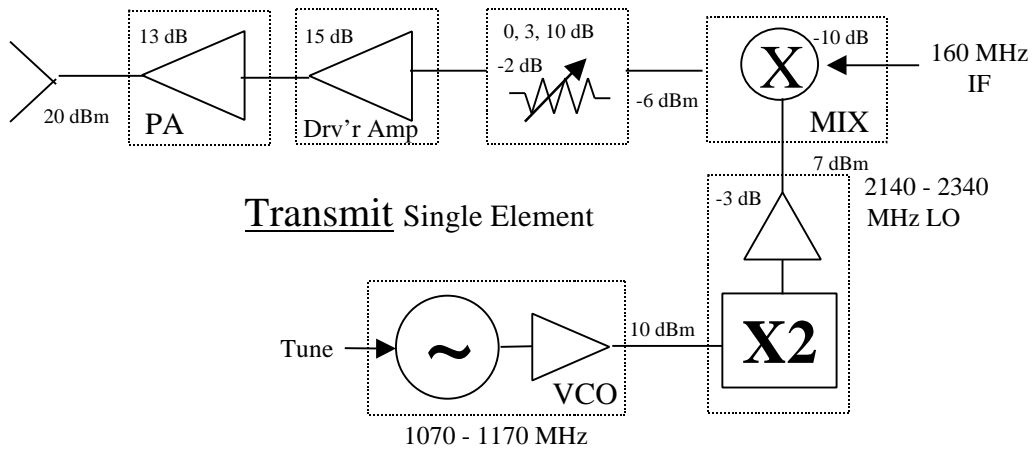
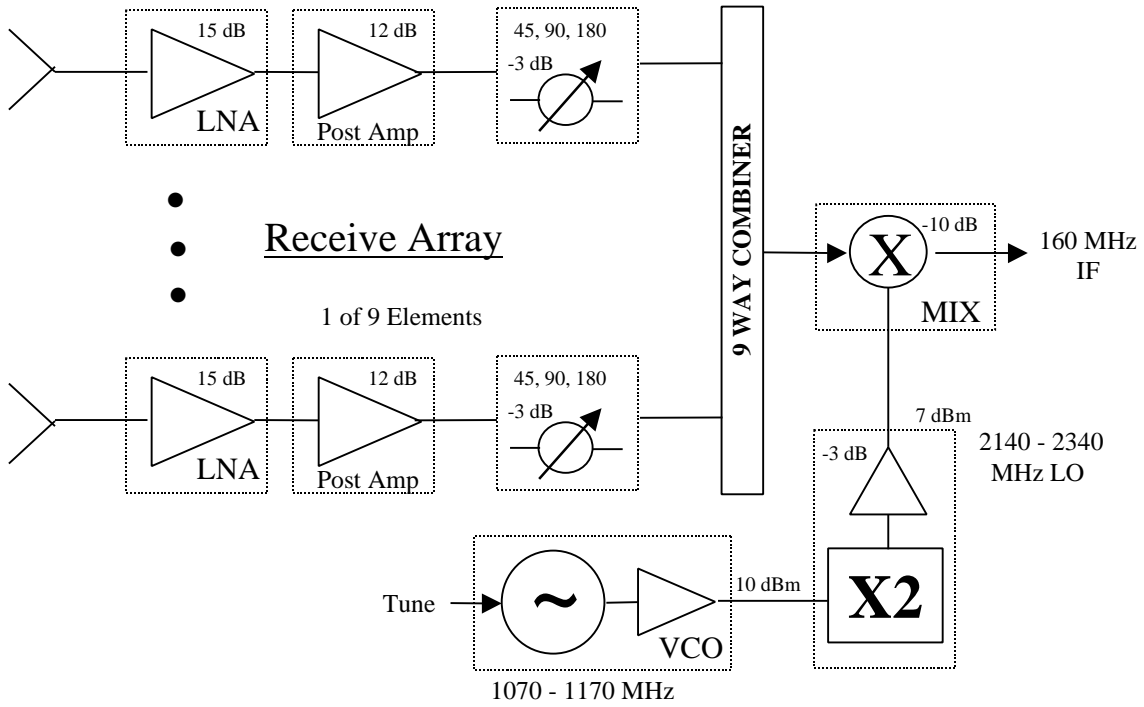


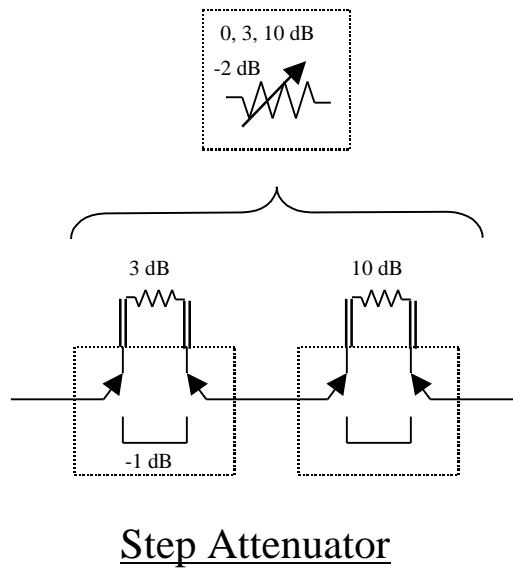
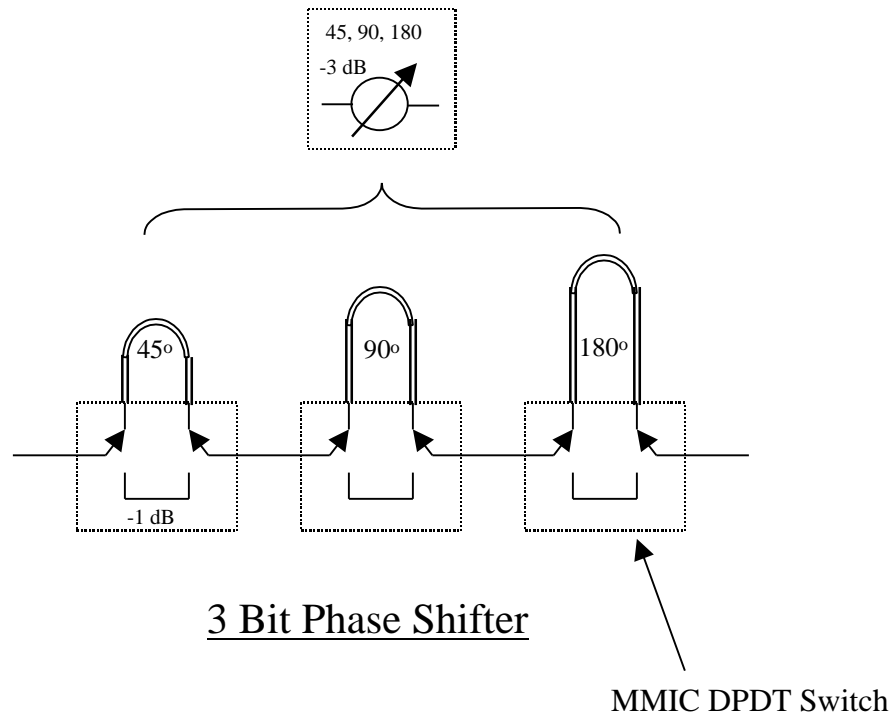
## **MMIC DESIGN EE 525.787 FALL 2002**

### **STUDENT PROJECTS**

This year's project for the MMIC Design class at The Johns Hopkins University is a duplex transceiver employing a receive array for the S-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies. The frequency conversion scheme uses an S-band frequency converter, which produces a 160 MHz IF signal that carries the modulation. The modulated 160 MHz IF is upconverted to S-band in the transmit mode. The frequency converter consists of a mixer, VCO, and frequency doubler. The VCO operates from 1070 to 1170 MHz, which when doubled is 160 MHz below the WCS and ISM frequencies. S-band DPDT switches are employed to implement a 3 bit phase shifter for the receive array with off-MMIC lengths of transmission line. Transmit level control is implemented with the DPDT switches and off-MMIC attenuator chips. Each element of the receive chain array consists of an LNA and a post amplifier in cascade, followed by a phase shifter. The transmit path employs a driver amplifier feeding a 100 milliwatt power amplifier. Nine unique MMIC designs make up the S-band transceiver. Each design is to be contained on a 60 mil square die in the TQS TRx process. The proposed block diagram is shown below.



Chip Set for the 2305 - 2360 MHz WCS and  
2400 - 2497 MHz ISM Bands



## PROJECTS

Low Noise Amplifier - 15 dB gain, 3 dB NF

Post Amplifier – 12 dB Gain, +20 dBm IP3

Down Converter – 160 MHz IF, +7 dBm LO

Up Converter – 160 MHz IF, +7 dBm LO

Driver Amplifier - 15 dB gain, +10 dBm output @ P1dB

Power Amplifier – 100 milliwatt, 13 dB gain, class F

Frequency Doubler – 3 dB Conversion Loss

Voltage Control'd Osc. - 1070 to 1170 MHz tuning range

DPDT Switch – 1 dB insertion loss, 20 dB isolation

## GENERAL CONDITIONS

### TriQuint:

TQTRx Process, with vias  
4 mil (100 micron) thick wafer  
60 x 60 mil die (ANACHIP)  
TOM3 FET model in ADS

### Testing:

Agilent 8510 VNA (45 MHz to 26 GHz)  
Cascade Model 43 wafer probe station with  
up to 4 RF probes & 4 DC needle probes  
Synthesized signal generators to 26 GHz  
Spectrum analyzer to 18 GHz

**SPECIFICATIONS FOR S BAND LOW NOISE AMPLIFIER**

*On chip high Q matching networks, source inductance  
and FET size tuned for low noise with good input VSWR*

FREQUENCY:	2300 to 2500 MHz
BANDWIDTH:	> 200 MHz
GAIN:	> 15 dB
GAIN RIPPLE:	$\pm 0.5$ dB max.
NOISE FIGURE:	< 5 dB;      3 dB, goal
INPUT IP3:	> +5 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	$\pm 5$ Volts;      + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

## **SPECIFICATIONS FOR S BAND POST AMPLIFIER**

*Two stage amplifier with on chip bias network and FET size tuned for efficient Class A power operation with good input & output VSWR*

FREQUENCY:	2300 to 2500 MHz
BANDWIDTH:	> 200 MHz
GAIN small signal:	> 12 dB; 15 dB, goal
GAIN RIPPLE:	$\pm 0.5$ dB goal
OUTPUT IP3:	> +20 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	$\pm 5$ Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

## **SPECIFICATIONS FOR S BAND DOWN CONVERTER**

*FET mixer with lumped element match for RF and LO,  
external bias for starved LO operation.*

FREQUENCY:            RF = 2300 to 2500 MHz; LO = 2140 to 2340 MHz;  
                              IF=160 MHz

ISOLATION:            LO/RF 10 dB min.; 16 dB goal

CONVERSION LOSS:    10 dB max.;     7 dB goal

LO POWER:            +7dBm max    0 dBm goal

VSWR, 50 Ohm:        2.5:1 max.;     1.5:1 goal

SUPPLY VOLTAGE:    Variable, 0 to 5 Volts

SIZE:                    60 x 60 mil ANACHIP

## **SPECIFICATIONS FOR S BAND UP CONVERTER**

*Lumped element hybrid for RF and LO,  
external bias for starved LO operation.*

FREQUENCY:            RF = 2300 to 2500 MHz; LO = 2140 to 2340 MHz;  
                              IF=160 MHz

ISOLATION:            LO/RF 10 dB min.; 16 dB goal

CONVERSION LOSS:    10 dB max.;     7 dB goal

LO POWER:            +7dBm max    0 dBm goal

VSWR, 50 Ohm:        2.5:1 max.;     1.5:1 goal

SUPPLY VOLTAGE:    Variable, 0 to 5 Volts

SIZE:                    60 x 60 mil ANACHIP

## **SPECIFICATIONS FOR S BAND DRIVER AMPLIFIER**

*Two stage amplifier with on chip bias network and FET size tuned for efficient Class A power operation with good input & output VSWR*

FREQUENCY:	2300 to 2500 MHz
BANDWIDTH:	> 200 MHz
GAIN small signal:	> 15 dB; 18 dB, goal
GAIN RIPPLE:	$\pm 0.5$ dB goal
OUTPUT POWER:	> +10 dBm @ 1 dB compression
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	$\pm 5$ Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

## **SPECIFICATIONS FOR S BAND POWER AMPLIFIER**

*On chip drain and gate bias network, output matching network,  
and FET size tuned for efficient Class F power operation with  
good input & output VSWR*

FREQUENCY:	2300 to 2500 MHz
BANDWIDTH:	> 200 MHz
GAIN, small signal:	> 13 dB;                      15 dB, goal
GAIN RIPPLE:	$\pm 0.5$ dB max.
OUTPUT POWER:	> +20 dBm @ 1 dB compression
EFFICIENCY:	> 20 % @ 1dB compression; 25 %, goal
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE:	+ 7 and -5 Volts
SIZE:	60 x 60 mil ANACHIP

**SPECIFICATIONS FOR L/S BAND FREQUENCY DOUBLER**

*FET doubler with on chip matching for fundamental  
and third harmonic rejection.*

FREQUENCY:            OUTPUT = 2140 to 2340 MHz;  
                              INPUT=1070 TO 1170 MHz

CONVERSION LOSS:    3 dB max.;      0 dB goal

INPUT POWER:        +10 dBm typ.

SPURIOUS:            FUNDAMENTAL = 16 dBc min.; 25 dBc goal  
                              THIRD = 20 dBc min.; 30 dBc goal

VSWR, 50 Ohm:        2.5:1 max.;      1.5:1 goal

SUPPLY VOLTAGE:     $\pm 5$  Volts;    + 5 Volts only, goal

SIZE:                    60 x 60 mil ANACHIP

**SPECIFICATIONS FOR L BAND VOLTAGE CONTROLLED OSCILLATOR**

*On chip high Q resonator and tuning varactor.*

FREQUENCY: 1070 to 1170 MHz  
OUTPUT POWER: > +10 dBm; +13 dBm goal  
CONTROL VOLTAGE: 0 TO -5 Volts  
SUPPLY VOLTAGE:  $\pm 5$  Volts; +5 Volts only goal  
OUTPUT IMPEDANCE: 50 Ohm, nominal  
SIZE: 60 x 60 mil ANACHIP

## **SPECIFICATIONS FOR S BAND DPDT SWITCH**

*FET switch with on chip TTL driver internally connected for low RF insertion loss operation as a bypass switch*

FREQUENCY:	2300 to 2500 MHz
BANDWIDTH:	> 200 MHz
INSERTION LOSS:	< 1 dB;      0.6 dB, goal
ISOLATION:	> 20 dB
POWER HANDLING:	> +20 dBm @ 1 dB compression
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	$\pm$ 5 Volts
CONTROL:	TTL
SIZE:	60 x 60 mil ANACHIP