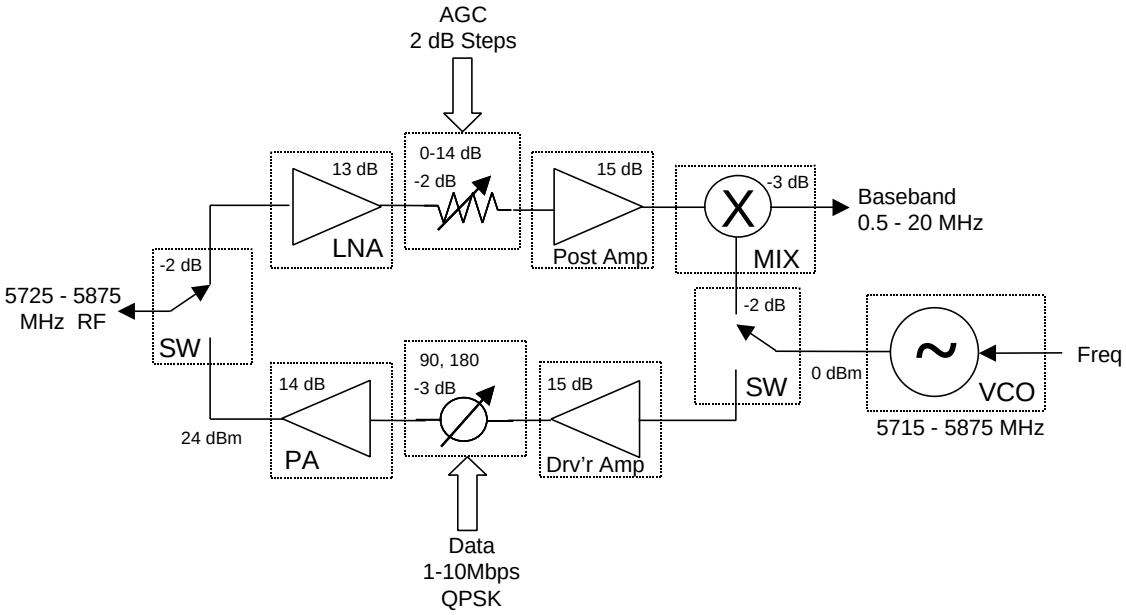
MMIC DESIGN EE 525.787 FALL 2003

STUDENT PROJECTS

This year's project for the MMIC Design class at The Johns Hopkins University is a simplex transceiver for the C-band industrial, scientific, and medical (ISM) band. The down conversion scheme uses a single FET frequency converter, which produces a baseband output at 0.5 to 20 MHz. The VCO serves as the receive LO as well as the C-band frequency source in the transmit mode. QPSK modulation is introduced by a 2 bit quadrature phase shifter, switching at up to 10 Mbps. C-band SPDT switches are employed to route receive and transmit signals and the VCO appropriately. The receive chain consists of an LNA, a 3 bit attenuator for AGC, and a post amplifier in cascade. The transmit path employs a driver amplifier and a 2 bit phase shifter feeding a ¼ watt power amplifier. Nine unique MMIC designs make up the ten chip C-band transceiver. Each design is to be contained on a 60 mil square die in the TQS TRx process. The proposed block diagram is shown below.



Chip Set for the 5725 - 5875 MHz ISM Band

PROJECTS

Low Noise Amplifier - 13 dB gain, 3 dB NF

Step Attenuator – 0 to 14 dB attenuation in 2 dB steps

Post Amplifier – 15 dB Gain, +15 dBm OIP3

Mixer – 3 dB conversion loss, -2 dBm LO power

Voltage Control'd Osc. - 5715 to 5875 MHz tuning range

Driver Amplifier - 15 dB gain, +13 dBm output @ P1dB

Digital Quad Modulator – 2 bit QPSK 1 to 10 Mbps

Power Amplifier - 1/4 watt, 15 dB gain, class F

SPDT Switch – 2 dB insertion loss, 20 dB isolation

GENERAL CONDITIONS

TriQuint:

TQTRx Process, with vias
4 mil (100 micron) thick wafer
60 x 60 mil die (ANACHIP)
TOM3 FET model in ADS

Testing:

Agilent 8510 VNA (45 MHz to 26 GHz)
Cascade Model 43 wafer probe station with
up to 4 RF probes & 4 DC needle probes
Synthesized signal generators to 26 GHz
Spectrum analyzer to 18 GHz

SPECIFICATIONS FOR C BAND LOW NOISE AMPLIFIER

On chip high Q matching networks, source inductance and FET size tuned for low noise with good input VSWR

FREQUENCY:	5725 to 5875 MHz
BANDWIDTH:	> 150 MHz
GAIN:	> 13 dB
GAIN RIPPLE:	$\pm$ 0.5 dB max.
NOISE FIGURE:	< 3 dB;
OUPUT IP3:	> +5 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	$\pm$ 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND POST AMPLIFIER

Two stage amplifier with on chip bias network and FET size tuned for efficient Class A power operation with good input & output VSWR

FREQUENCY:	5725 to 5875MHz
BANDWIDTH:	> 150 MHz
GAIN small signal:	> 15 dB
GAIN RIPPLE:	$\pm$ 0.5 dB goal
OUTPUT IP3:	> +15 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	$\pm$ 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND POWER AMPLIFIER

On chip drain and gate bias network, output matching network, and FET size tuned for efficient Class F power operation with good input & output VSWR

FREQUENCY:	5725 to 5875 MHz
BANDWIDTH:	> 150 MHz
GAIN, small signal:	> 15 dB
GAIN RIPPLE:	$\pm$ 0.5 dB max.
OUTPUT POWER:	> +24 dBm @ 1 dB compression
EFFICIENCY:	> 20 % @ 1dB compression; 30 %, goal
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE:	+ 7 and –5 Volts
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND DRIVER AMPLIFIER

Two stage amplifier with on chip bias network and FET size tuned for efficient Class A power operation with good input & output VSWR

FREQUENCY:	5725 to 5875MHz
BANDWIDTH:	> 150 MHz
GAIN small signal:	> 15 dB
GAIN RIPPLE:	$\pm$ 0.5 dB max.
OUTPUT POWER:	> +13 dBm @ 1 dB compression
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	$\pm$ 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND DOWN CONVERTER

Active FET mixer with on chip LO amplifier.

FREQUENCY: RF = 5725 to 5875 MHz
LO = 5715 to 5865 MHz;
IF= 0.5 to 20 MHz

ISOLATION: LO/RF 10 dB min.; 16 dB goal

CONVERSION LOSS: 3 dB max

LO POWER: -2 dBm max

VSWR, 50 Ohm: 2.5:1 max.; 1.5:1 goal

SUPPLY VOLTAGE: Variable, 0 to 5 Volts

SIZE: 60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND VOLTAGE CONTROLLED OSCILLATOR

On chip high Q resonator and tuning varactor.

FREQUENCY:	5715 to 5875 MHz
OUTPUT POWER:	> 0 dBm
CONTROL VOLTAGE:	0 TO 5 Volts
SUPPLY VOLTAGE:	±5 Volts; +5 Volts only goal
OUTPUT IMPEDANCE:	50 Ohm, nominal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND SPDT SWITCH

FET switch with on chip TTL driver and FET size tuned for ¼ watt power operation with good input & output VSWR

FREQUENCY:	5725 to 5875 MHz
BANDWIDTH:	> 150 MHz
INSERTION LOSS:	< 2 dB; 1.5 dB, goal
ISOLATION:	> 20 dB
POWER HANDLING:	> +24 dBm @ <2 dB loss
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	$\pm$ 5 Volts
CONTROL:	TTL
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND QUADRATURE MODULATOR

FET switched 2 bit 90^o an 180^o phase shift with on chip TTL driver

FREQUENCY:	5725 to 5875 MHz
BANDWIDTH:	20 MHz instantaneous
PASSBAND RIPPLE:	$\pm$ 0.5 dB max.
PHASE DIFFERENCE:	90 degrees $\pm$ 5 degrees between any state
AMPLITUDE BALANCE:	$\pm$ 1 dB between any state
INSERTION LOSS:	3 dB, goal
VSWR, 50 Ohm:	< 1.5:1, any state, goal
CONTROL VOLTAGE:	Two TTL lines
CONTROL RATE:	1 to 10 Mbps
SUPPLY VOLTAGE:	+5 and –5 Volts
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND DIGITAL ATTENUATOR

FET switched 3 bit 0 to 14 db in 2 dB steps with on chip TTL driver

FREQUENCY:	5725 to 5875 MHz
BANDWIDTH:	<150 MHz
PASSBAND RIPPLE:	$\pm$ 0.5 dB max.
AMPLITUDE DIFFERENCE:	2 dB $\pm$ 0.5 dB between any state
INSERTION LOSS:	2 dB, goal
VSWR, 50 Ohm:	< 1.5:1, any state, goal
CONTROL VOLTAGE:	Three TTL lines
SUPPLY VOLTAGE:	+5 and –5 Volts
SIZE:	60 x 60 mil ANACHIP