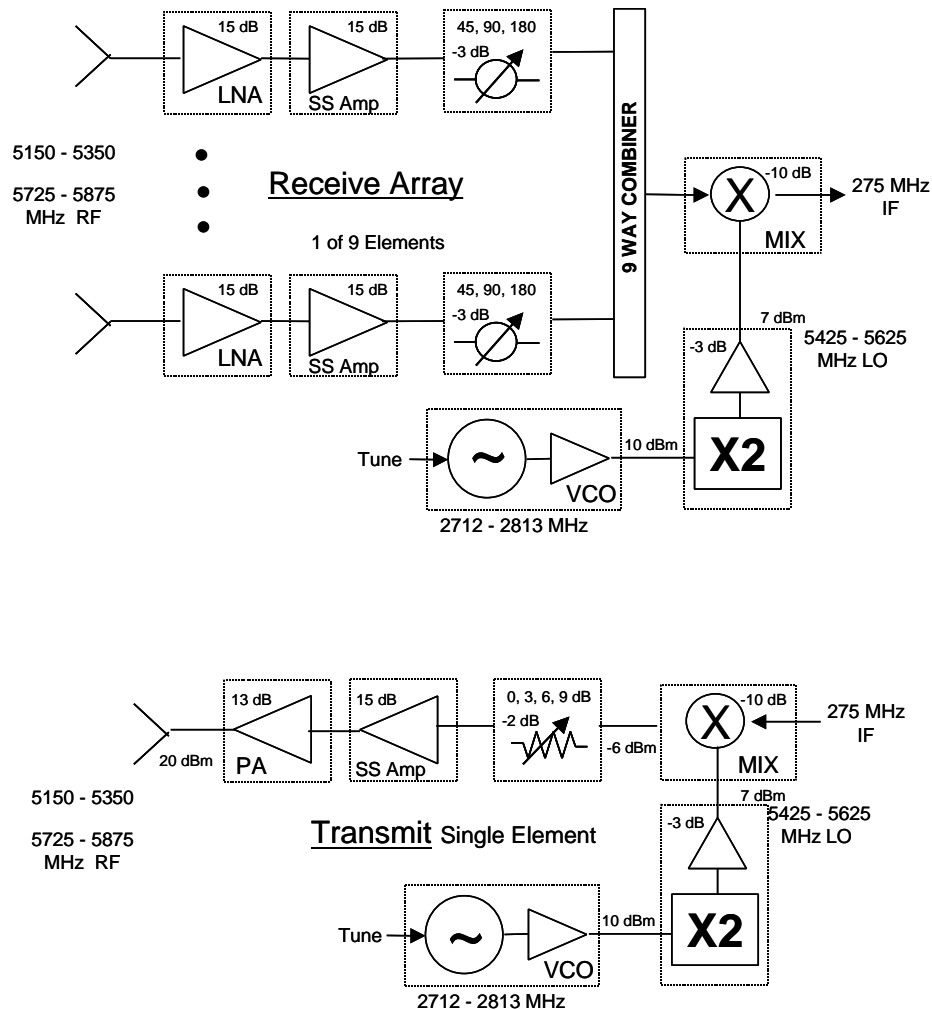


MMIC DESIGN EE 525.787 FALL 2004

STUDENT PROJECTS

This year's project for the MMIC Design class at The Johns Hopkins University is a duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies. The frequency conversion scheme uses a C-band frequency converter, which produces a 275 MHz IF signal that carries the modulation. The modulated 275 MHz IF is upconverted to C-band in the transmit mode. The frequency converter consists of a mixer, VCO, and frequency doubler. The VCO operates from 2712 to 2813 MHz, which when doubled is between the WLAN and ISM frequencies. A phase shifter chip implements a 3 bit phase for the receive array. Transmit level control is implemented with the MMIC attenuator chip. Each element of the receive chain array consists of an LNA and a driver amplifier in cascade, followed by a phase shifter. The transmit path employs a driver amplifier feeding a 100 milliwatt power amplifier. Nine unique MMIC designs make up the S-band transceiver. Each design is to be contained on a 60 mil square die in the TQS TRx process. The proposed block diagram is shown below.



**Chip Set for the 5150 - 5350 MHz WLAN and
5725 - 5875 MHz ISM Bands**

PROJECTS

Low Noise Amplifier - 15 dB gain, 3 dB NF

SS Amplifier – 15 dB Gain, +20 dBm IP3

Up/Down Converter – 275 MHz IF, +7 dBm LO

Attenuator – goal 2 dB IL, 3 dB steps, 2 bit control

Power Amplifier – 100 milliwatt, 13 dB gain, class F

Frequency Doubler – 3 dB Conversion Loss

Voltage Control'd Osc. - 2712 to 2813 MHz tuning range

3 bit Phase Shifter – goal 3 dB insertion loss, 1/2 LSbit accuracy

GENERAL CONDITIONS

TriQuint:

TQTRx Process, with vias
4 mil (100 micron) thick wafer
60 x 60 mil die (ANACHIP)
TOM3 FET model in ADS

Testing:

Agilent 8510 VNA (45 MHz to 26 GHz)
Cascade Model 43 wafer probe station with
up to 4 RF probes & 4 DC needle probes
Synthesized signal generators to 26 GHz
Spectrum analyzer to 18 GHz

SPECIFICATIONS FOR C BAND LOW NOISE AMPLIFIER

*On chip high Q matching networks, source inductance
and FET size tuned for low noise with good input VSWR*

FREQUENCY:	5150 to 5875 MHz
BANDWIDTH:	> 800 MHz
GAIN:	> 15 dB
GAIN RIPPLE:	± 0.5 dB goal.
NOISE FIGURE:	< 4 dB; 3 dB, goal
INPUT IP3:	> +5 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	± 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR SMALL SIGNAL AMPLIFIER

Two stage amplifier with on chip bias network and FET size tuned for efficient Class A power operation with good input & output VSWR

FREQUENCY:	5150 to 5875 MHz
BANDWIDTH:	> 800 MHz
GAIN small signal:	> 15 dB; 16 dB, goal
GAIN RIPPLE:	± 0.5 dB goal
OUTPUT IP3:	> +20 dBm
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	± 5 Volts; + 5 Volts only, goal
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND UP/DOWN CONVERTER

diode mixer with lumped element match for RF and LO..

FREQUENCY: RF = 5150 to 5875 MHz; LO = 5425 to 5625 MHz;
IF=275 MHz

ISOLATION: LO/RF 10 dB min.; 16 dB goal

CONVERSION LOSS: 10 dB max.; 7 dB goal

LO POWER: +7dBm max 0 dBm goal

VSWR, 50 Ohm: 2.5:1 max.; 1.5:1 goal

SUPPLY VOLTAGE: Variable, 0 to 5 Volts

SIZE: 60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND POWER AMPLIFIER

*On chip drain and gate bias network, output matching network,
and FET size tuned for efficient Class F power operation with
good input & output VSWR*

FREQUENCY:	5150 to 5875 MHz
BANDWIDTH:	> 800 MHz
GAIN, small signal:	> 13 dB; 15 dB, goal
GAIN RIPPLE:	± 0.5 dB max.
OUTPUT POWER:	> +20 dBm @ 1 dB compression
EFFICIENCY:	> 20 % @ 1dB compression; 25 %, goal
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE:	+ 5 and -5 Volts
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR S/C BAND FREQUENCY DOUBLER

*FET doubler with on chip matching for fundamental
and third harmonic rejection.*

FREQUENCY: OUTPUT = 5425 to 5625 MHz;
 INPUT=2712 TO 2813 MHz

CONVERSION LOSS: 3 dB max.; 0 dB goal

INPUT POWER: +10 dBm typ.

SPURIOUS: FUNDAMENTAL = 16 dBc min.; 25 dBc goal
 THIRD = 20 dBc min.; 30 dBc goal

VSWR, 50 Ohm: 2.5:1 max.; 1.5:1 goal

SUPPLY VOLTAGE: ± 5 Volts; + 5 Volts only, goal

SIZE: 60 x 60 mil ANACHIP

SPECIFICATIONS FOR S BAND VOLTAGE CONTROLLED OSCILLATOR

On chip high Q resonator and tuning varactor.

FREQUENCY: 2712 to 2813 MHz

OUTPUT POWER: > +10 dBm; +13 dBm goal

CONTROL VOLTAGE: 0 TO -5 Volts

SUPPLY VOLTAGE: ± 5 Volts; +5 Volts only goal

OUTPUT IMPEDANCE: 50 Ohm, nominal

SIZE: 60 x 60 mil ANACHIP

SPECIFICATIONS FOR C BAND ATTENUATOR

FET switches with on chip TTL driver

FREQUENCY:	5150 to 5875 MHz
BANDWIDTH:	> 800 MHz
INSERTION LOSS:	< 3 dB min IL (2 dB goal); steps 0, 3, 6, and 9 db
ISOLATION:	> 20 dB
POWER HANDLING:	> +20 dBm @ 1 dB compression
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	\pm 5 Volts
CONTROL:	TTL
SIZE:	60 x 60 mil ANACHIP

SPECIFICATIONS FOR 3 BIT PHASE SHIFTER

Goal: *FET switches with on chip TTL driver*

FREQUENCY: 5150 to 5875 MHz
BANDWIDTH: > 800 MHz
INSERTION LOSS: < 4 dB min IL (3 dB goal);
INSERTION BALANCE: +/- 1dB min IL;
PHASE SHIFT: steps 45 (goal), 90 and 180 degrees
VSWR, 50 Ohm: < 1.5:1 input & output
SUPPLY VOLTAGE : ± 5 Volts
CONTROL: TTL (goal); or 0, -5V switch inputs
SIZE: 60 x 60 mil ANACHIP