

C-Band General Purpose Amplifier



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Abstract - A single-supply 12dB MMIC C-band general-purpose amplifier for the HYPERLAN wireless local area network frequencies has been designed based on well-known small-signal s-parameter techniques and the Cripps method. The amplifier is packaged on a 60x60 mil ANACHIP realized using Triquint's foundry process. The design is capable of producing in excess of +13dBm of power with good input and output VSWR (50Ω). Also, the design features DC blocking capacitors at the input and output. The schematic and layout were simulated using Agilent's Advanced Design System (ADS). Simulated results show that all design specifications were met.

C-Band General Purpose Amplifier

1. Introduction

1.1. *Circuit Description*

The design is a two stage C-band general-purpose amplifier with on-chip bias network utilizing two 300um GFETs. The amplifier is intended to operate from 5150 to 5350 MHz on a single +5V supply. A simultaneously conjugate matched first stage is followed by a second power amplifier stage to provide 12 dB of gain across the band. The output power is typically 16 dBm at 1dB gain compression. The second stage is biased directly from the +5V supply. A resistive divider provides approximately 4V to the first stage. The resistive divider along with a 12 pF capacitor assists in isolating the two stages thereby suppressing instability. On-chip DC blocks allows *cascaability* with good input and output VSWR. The overall chip size is 60x60 mil.

1.2. *Design Philosophy*

The design is implemented using small-signal s-parameter techniques and the Cripp's method. The primary design strategy was to work with each stage separately. The secondary design strategy is to begin matching the 2nd stage output matching network (OMN) towards the 1st stage input matching network (IMN). Note that the stability of the individual and combined first and second stages was checked.

1.2.1. Selection of transistors and operating point

Two 300um GFETs were selected. The 2nd stage GFET is suitable for meeting the output power requirements. However, the 1st stage GFET is sized for ease of matching between the 1st and 2nd stages. A simple interstage matching network (CMN) is desired because it uses less chip space. The 1st stage is biased to provide ample linear gain prior to the 2nd stage. The 2nd stage was biased at approximately $\frac{1}{2} I_{DSS} = 50$ mA.

1.2.2. Transistor stabilization

The utilization of series and shunt resistors at the gates suppresses instabilities at the high and low end, respectively.

1.2.3. Design of second stage output matching network

The Cripps method was used to realize the 2nd stage OMN. The desired load line that the amplifier would like to see for maximum symmetrical swing is 80Ω . This then leads to a preliminary OMN that matches 80Ω to 50Ω . Also, a 300Ω shunt was added to provide improved output VSWR.

1.2.4. Design of second stage input matching network

The input of the 2nd stage was simply conjugately matched to 50Ω with the OMN in place.

1.2.5. Design of first stage input and output matching network

The 1st stage was simply simultaneously conjugate matched.

1.2.6. Design of interstage matching network

It is straightforward to realize the interstage matching network (CMN) based on the 1st stage output and 2nd stage input impedances found previously.

1.2.7. Overall amplifier optimization

The first and second stages were combined using the interstage matching network. The overall amplifier was then optimized. Further optimization was required after replacing the ideal elements with Triquint elements. The stability was checked.

1.2.8. Conversion to self-bias

The drain and source bias resistors were selected to provide the desired bias (Figure 5).

1.2.9. Realization of the on-chip layout

All elements contained in the self-bias schematic were placed strategically within the required area of the 60x60 mil ANACHIP. Next, interconnects were routed and the elements positioned as appropriate. Then, schematics of the first, interstage, and second stage matching networks were recreated from the layout. Subsequent optimization of each stage was used to recover the performance seen in the prelayout schematic (Figure 4).

Also, the RC shunt networks were affixed on both sides of the FET artwork to preserve electrical symmetry (Figure 1).

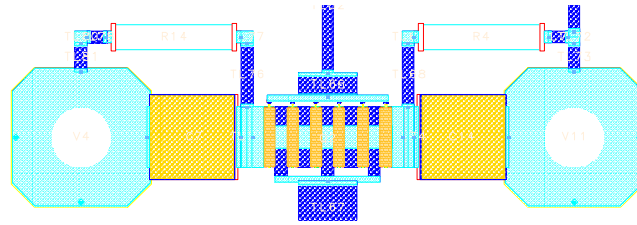


Figure 1: Layout - FET Symmetry

1.3. Trade-offs

In realizing a design that meet ALL specifications, the following were the trade-offs that were made.

- ◆ Gain & Power for output VSWR – the OMN network was readjusted slightly to improve VSWR.
- ◆ First stage transistor size for ease of developing interstage match - a smaller transistor makes matching difficult.
- ◆ Gain for stability – the stabilizing resistors taxed the gain
- ◆ Power for self-bias – the self-bias network pinched the output signal swing at high voltages and the operating point shifted from 5 to 4.3V.

2. Modeled Performance

2.1. Specification Compliance Matrix

Table 1: Specification Compliance Matrix

Requirements	Specification	Goal	Simulated	
			Pre-layout	Post-layout
Frequency	5150 to 5350 MHz	-	ACHIEVED	ACHIEVED
Bandwidth	> 200MHz	-	ACHIEVED	ACHIEVED
Gain (small-signal)	> 12dB	15dB	15	14
Gain ripple	± 0.5 dB	-	ACHIEVED	ACHIEVED
Output Power @ 1dB compression	> +13dBm	-	18	16
VSWR, 50 Ω				
Input	< 1.5:1	-	1.46	1.46
Output	< 1.5:1	-	1.22	1.22
Supply Voltage	± 5 Volts	+5 Volts	ACHIEVED	ACHIEVED
Size	60x60mil ANACHIP	-	ACHIEVED	ACHIEVED

2.2. Predicted Performance

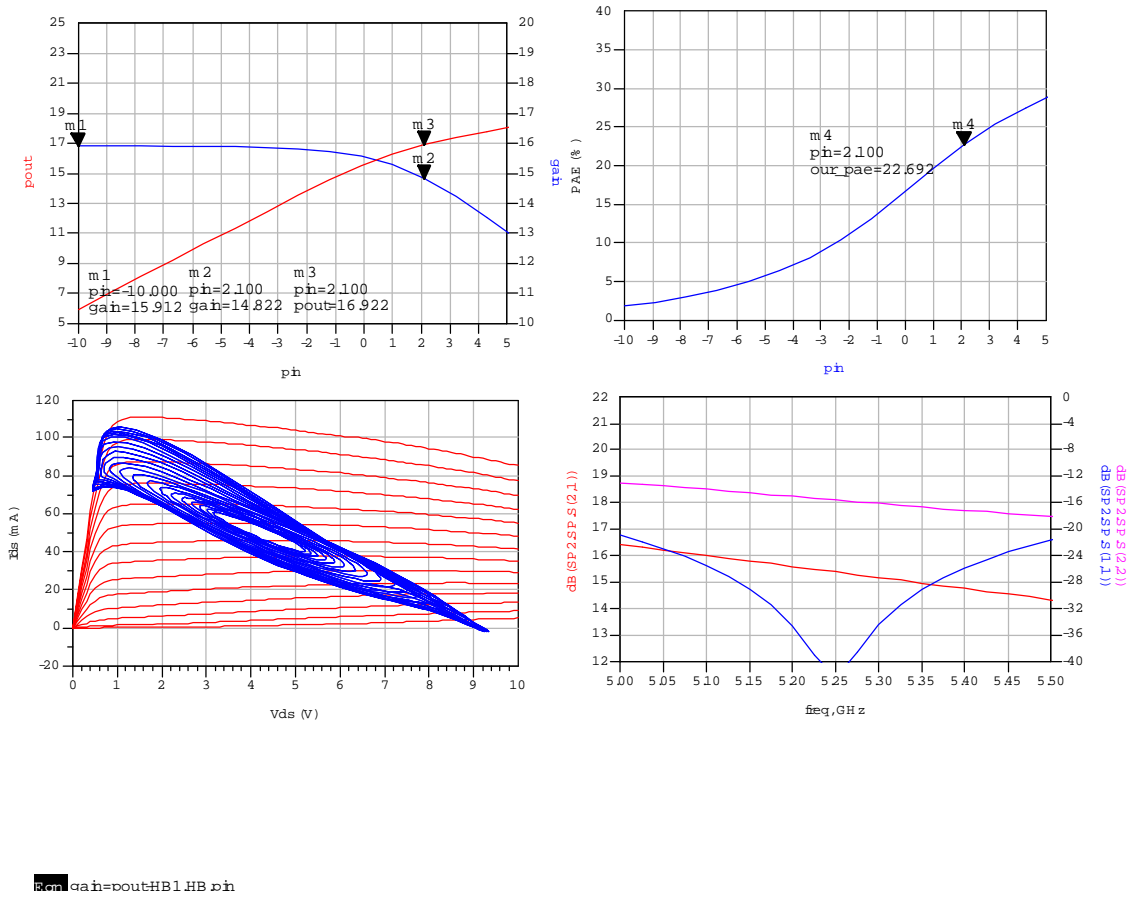
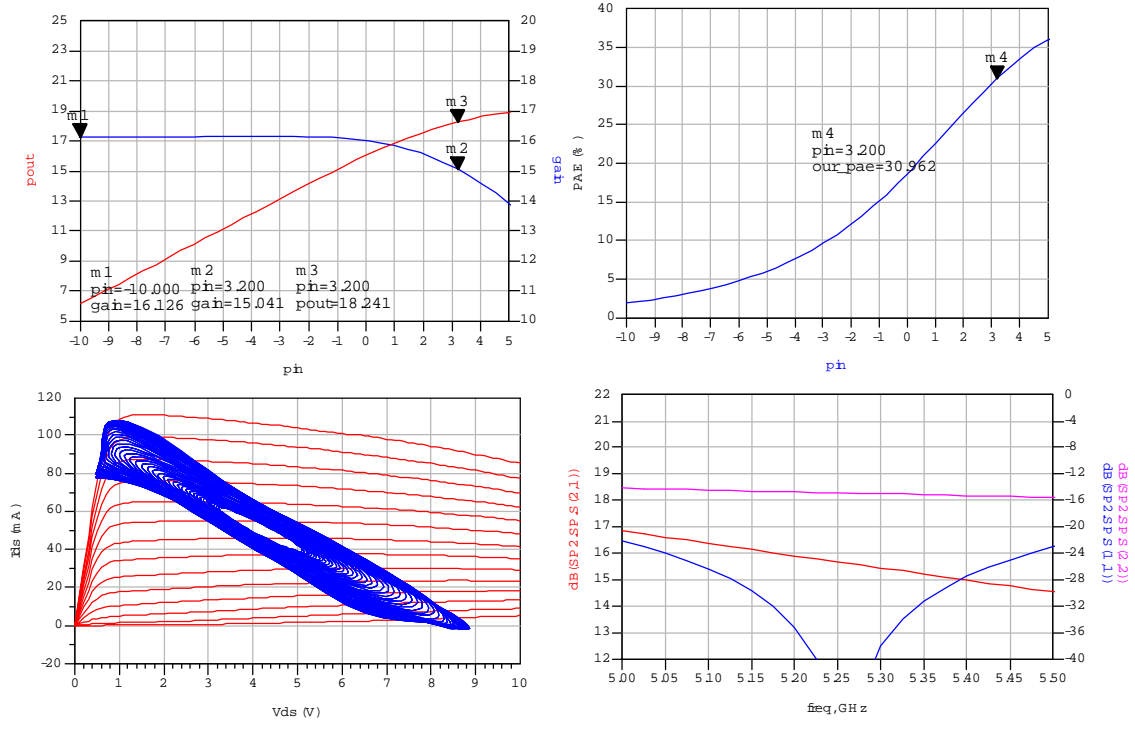


Figure 2: Overall Performance (Post-layout)



Sim: gain=pout-HR1_HR.ph

Figure 3: Overall performance (Pre-layout)

Schematic Diagrams

R1	24
R2	445
R3	114
R4	34
R5	300
R6	10
R7	14
R8	300
Vdd	5V
C1	0.46 pF
C2	12 pF
C3	12 pF
C4	0.13 pF
C5	0.66 pF
C6	12 pF
C7	12 pF
C8	0.71 pF
C9	1.64pF
L1	1840 pH
L2	5000 pH
L3	3000 pH
L4	3000 pH
L5	3500 pH
Q1	GFET 300um
Q2	GFET 300um

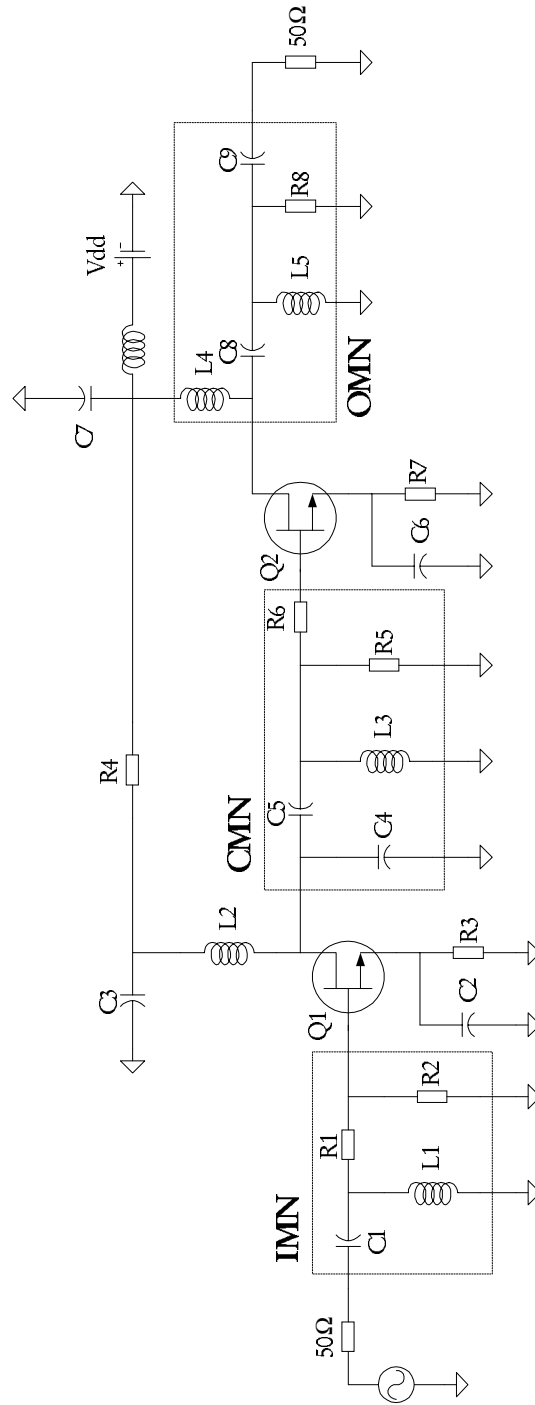


Figure 4: Self-bias Schematic (Pre-layout)

3. DC Analysis

3.1. Simplified DC Schematic

R1	24
R2	445
R3	114
R4	34
R6	10
R7	14
Vdd	5V
Q1	GFET 300um
Q2	GFET 300um

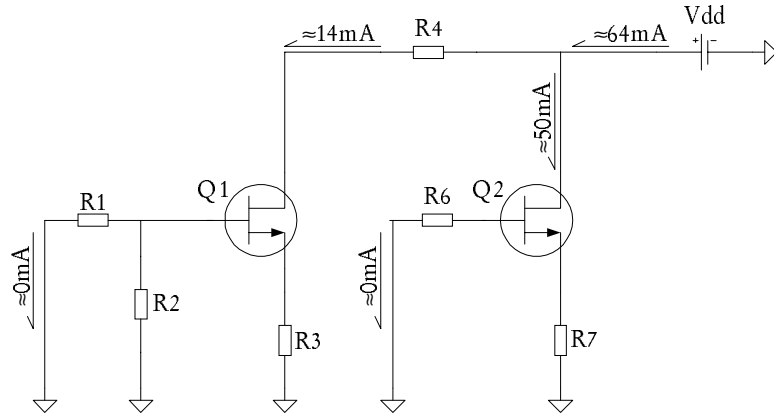


Figure 5: Simplified DC Schematic

3.2. Bias Check

Both stages are biased from a single drain supply of +5V. This feature was achieved via a self-bias topology (Figure 5).

Table 2: Modeled DC Analysis (Pre-layout)

Stage	Vgs (V)	Vds (V)	Ids (mA)
1	-1.54	3	14
2	-0.7	4.3	50

3.3. Interconnect and Component DC Current Stress

The NiCr resistors and all other interconnects used in the layout meets the current stress requirement. The resistors and the interconnects are specified to handle 1 and 18 mA per micron, respectively. A break-down of the current handling capability of the ‘high-risk’ resistors is summarized in Table 3. The maximum specified DC current stress rating is obtained by the following expression: $I_{max} = (\text{Width} \times \text{Rating in mA per micron}) \times 150\%$.

Table 3: Resistor Current Stress Rating

Resistor	Width (um)	Current (mA)		
		Max. spec.	Nominal	Worst-case
R3	50	50	14	21
R4	25	25	14	21
R7	76	76	50	75

4. Test Plan

- Setup test bench (Figure 6) to measure total current and s-parameters
- Apply bias – the total current should be approximately 64mA based on DC analysis.
- Measure s-parameters – chip level probe testing with the Wiltron VNA; the chip has one RF input and one RF output, and one DC input.
- Setup test bench (Figure 6) to measure 1dB gain compression
- Apply bias
- Measure power vs. pin at 5150, 5250, and 5350 MHz – increase the input incrementally while recording the output power.

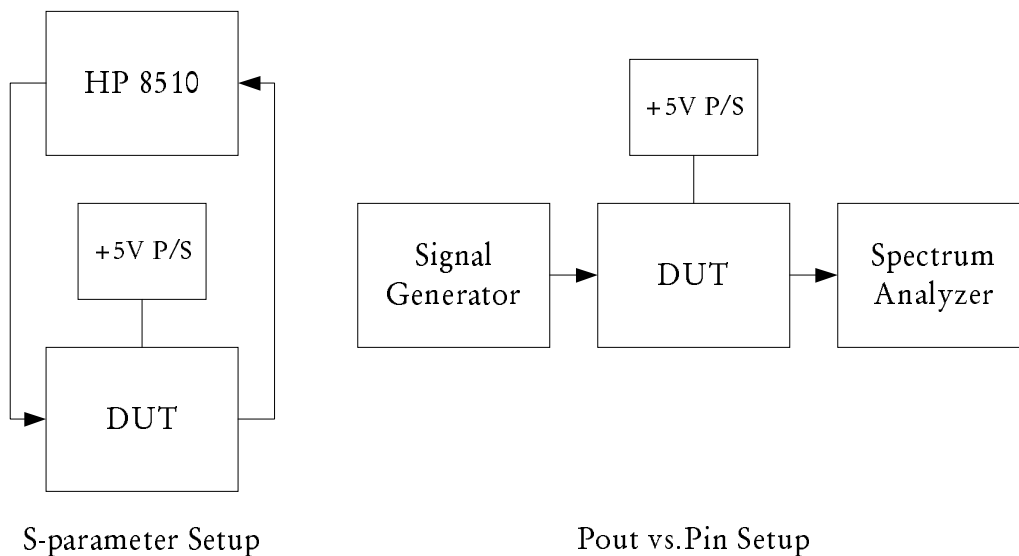


Figure 6: Test set-up

5. Conclusions & Recommendations

The two-stage general-purpose amplifier met all of its design specifications. I recommend tuning the output matching network if more margin on the output VSWR is desired. Also, I recommend checking performance based process variations. The process variations can be minimize by adding a resistor ladder.