

## *C-Band MESFET Low Noise Amplifier*

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*Abstract* – This paper details a C-Band,  $0.6\mu\text{m}$  MESFET low noise amplifier MMIC, designed for use in a duplex transceiver employing a HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies. The LNA design was simulated using Agilent's Advanced Design Systems (ADS 2003C). TriQuint Semiconductor, Oregon, provided small-signal and large-signal FET models resulting in the LNA having more than 17dB of gain, with a NF of less than 1.6dB, and an ITOI of +7dBm. Finally, the C-Band LNA was realized in a 60x60 mil ANACHIP footprint.

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# 1. Introduction

## 1.1 Circuit Description

The LNA design utilizes a two-stage cascaded topology operating at C-Band frequencies (5150MHz – 5875MHz). The first stage of the LNA is a noise matched 300 $\mu$ m DFET feeding a 600 $\mu$ m DFET. The second stage is conjugate matched to provide the 17dB of gain and nominal 1.5dB NF across the 0.8GHz operating bandwidth. The LNA employs a self-biased configuration on both stages to eliminate needless gate bias complexity while allowing the MMIC to operate using a single +3V power supply. Stability for the LNA is addressed using source feedback on the first stage and gate-to-drain feedback on the larger second stage. Similarly, a small resistance is added in the drain bias path on the first stage to further increase stability at low frequencies. Finally, this C-Band LNA is designed with to fit into a 60x60 mil ANACHIP layout.

## 1.2. Design Philosophy

The LNA design was realized using large signal MESFET models from TriQuint Semiconductor, Oregon. The basic low noise amplifier design consisted of noise matching the 300 $\mu$ m input stage and conjugately matching the following 600 $\mu$ m stage. Once a noise match was determined for the 1<sup>st</sup> stage, and a basic gain match satisfied for the 2<sup>nd</sup> stage, the LNA was then optimized to meet the design requirements and compact the layout.

### 1.2.1. Transistor selection

The bias configuration for the two stages of the LNA was set to approximately 50% Idss for both stages. The 300 $\mu$ m DFET produced a reasonable noise match when biased at ~2V Vds with 11mA of drain current. The 600 $\mu$ m second stage was bias at ~3V Vds and 22mA of drain current. The second stage bias was selected in part to help improve the LNA's linearity, as it drew more drain current.

### 1.2.2. Transistor Stability

Both stages of the LNA employed stability enhancing techniques. Source feedback was implemented on the 300 $\mu$ m DFET to lower gain and increase its stability. Similarly, drain-to-gate feedback was designed on the 600 $\mu$ m DFET to help flatten the overall gain of the LNA adding to the stability margin of the MMIC. Finally, by using a self-biasing configuration for both stages, the instabilities associated with off chip gate biasing was eliminated, further increasing stability.

### 1.2.3. First stage input matching network

The design of the input-matching network (IMN) was determined solely by noise matching the 300 $\mu$ m DFET with its added source inductance. The simple three-element matching network allowed for a reasonable input match while limiting the amount of loss presented to the 1<sup>st</sup> stage DFET.

#### **1.2.4. Interstage matching network**

Once the IMN was determined, the interstage network was chosen to provide the bandwidth for the LNA. Increasing the series capacitance on the gate of the 2<sup>nd</sup> stage extended the low-end frequency response. The drain-to-gate feedback on the 2<sup>nd</sup> stage was incorporated into the design of the interstage. This feedback allowed the gain of 600 $\mu$ m DFET to be reduced and flattened.

#### **1.2.5. Second stage output matching network**

As with the interstage, the design of the output matching network (OMN) also involved tweaking the feedback around the 2<sup>nd</sup> stage DFET. As with the IMN, a similar three-element network was chosen providing an excellent output match while reducing the size of the layout.

#### **1.2.6. Design optimization**

Once the basic design topology was determined, the simplified LNA model was then optimized. It is important to select appropriate ranges for the design elements during the optimization process so that the simulator does not blindly optimize. This process quickly yielded a LNA model that satisfied the majority of the design requirements.

#### **1.2.7. Design layout**

After the LNA was initially tuned to meet the design requirements, it was then brought into layout and tweaked to fit into the 60x60 mil ANANCHIP footprint. This iterative process finally yielded the layout shown in Figure 12.

### ***1.3. Trade-offs***

Many trade-offs are implemented in designing low noise amplifiers, including trades on gain, stability, noise figure, match, and IP3. While all of these parameters are important to successful circuit design, this C-Band LNA had only one major trade-off, NF vs. input VSWR.

As with most LNA designs, input match is often traded to improve noise figure. While the spec for this C-Band LNA required a noise figure of 4dB, the design was optimized to minimize noise figure. In the effort to reduce the NF to ~1.6dB, the input VSWR specification was relaxed from 1.5:1 to a 2.1:1 ratio, resulting in a -9dB input match. Giving up 5dB of input match for a 2.4dB improvement in NF seemed to be a reasonable trade.

## 2. Modeled Performance

### 2.1. Specification Compliance Matrix

Table 1: Specification Compliance Matrix

Parameter	Units	Requirement	Design	Compliance	Comments	
Size	mils	60 x 60	60 x 60	Yes		
Rx	Frequency	GHz	5.15-5.875	5.15-5.875	Yes	
	Bandwidth	GHz	0.8	0.8	Yes	
	Receive Gain	dB	>15	>17	Yes	
	Gain Ripple	dB	$\pm 0.5$	0.1	Yes	
	Noise Figure	dB	4	<1.6	Yes	2.4dB improvement
	TOI	dBm	>5	7.2	Yes	
	Input VSWR		1.5:1	2.1:1	No	Traded VSWR Spec for improve noise figure
	Output VSWR		1.5:1	<1.2:1	Yes	
	Rx Current	mA	<del>27</del>	27	Yes	
	Rx Voltage	V	5	3	No	Need to add a TAN resistor to layout, w=30um, l=38um
Stability		unconditional	unconditional	Yes		

### 2.2. Predicted Performance

#### 2.2.1. Large Signal DFET DC Simulations

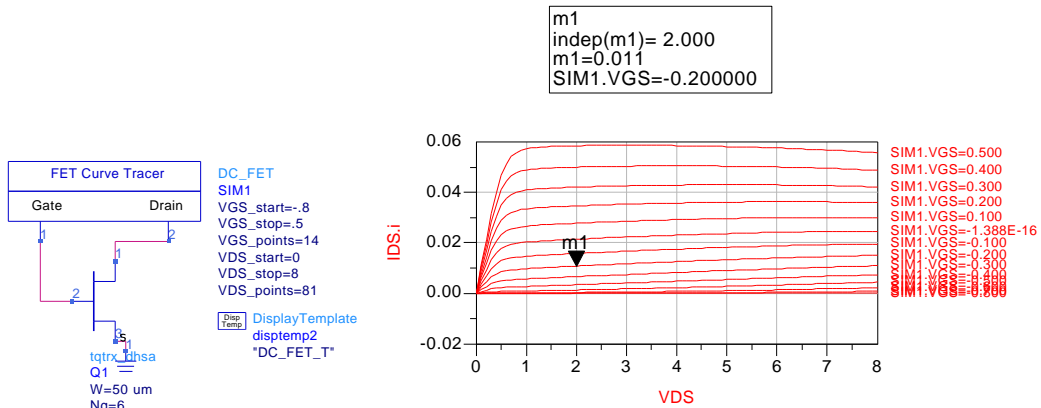


Figure 1. Stage 1 – 300um DFET (6 fingers x 50um wide)

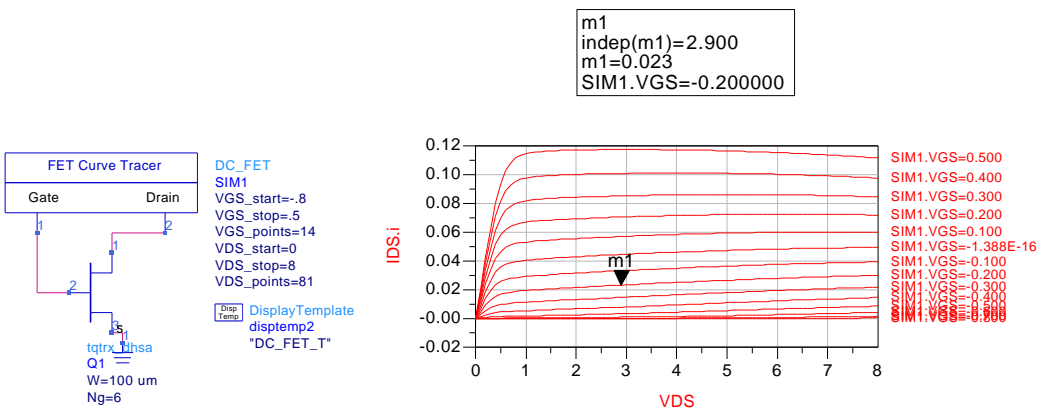


Figure 2. Stage 2 – 600um DFET (6 fingers x 100um wide)

## 2.2.2. Large Signal DFET RF Simulations

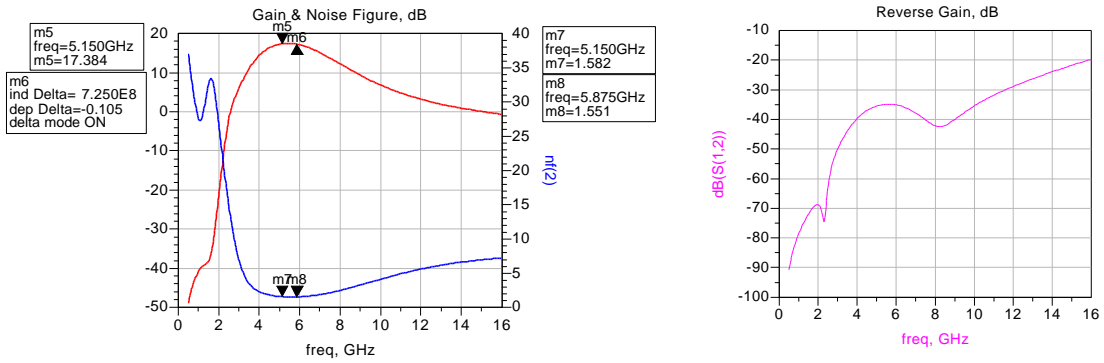


Figure 3. Complete Design – Wideband Gain, NF, and Reverse Gain Response

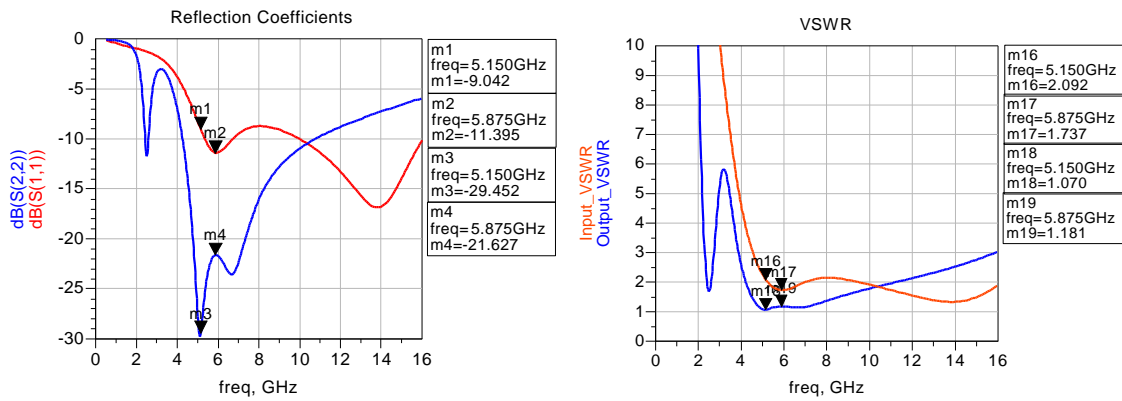


Figure 4. Complete Design – Wideband Match & VSWR Response

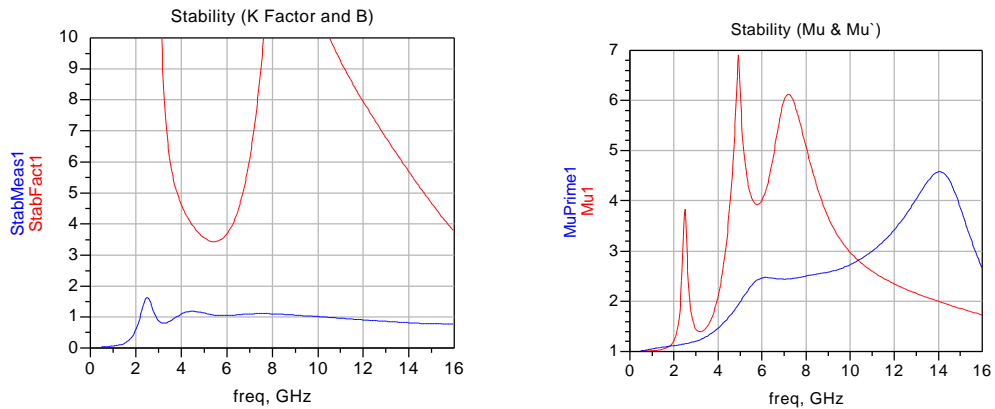


Figure 5. Complete Design – Wideband Stability Response

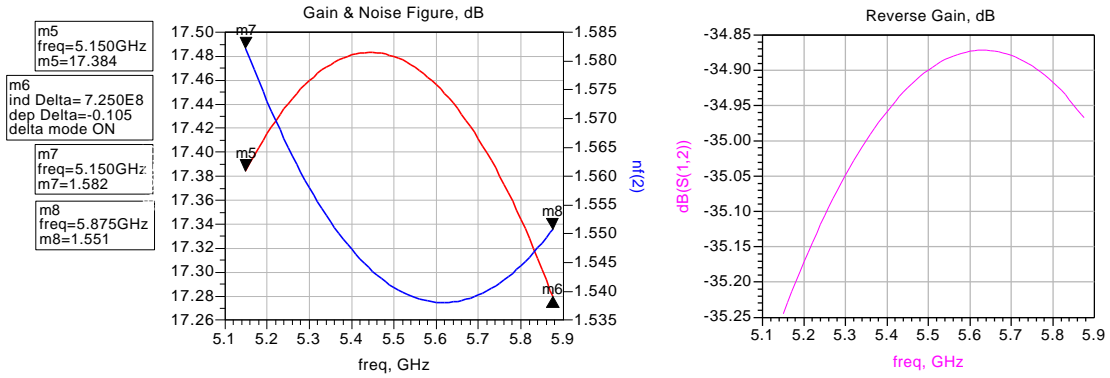


Figure 6. Complete Design – Narrow Band Gain, NF, and Reverse Gain Response

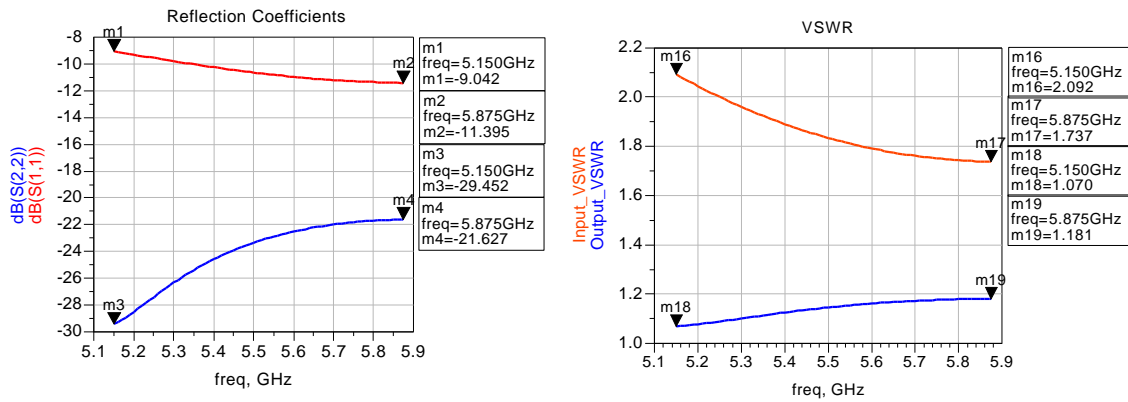


Figure 7. Complete Design – Narrow Band Match & VSWR Response

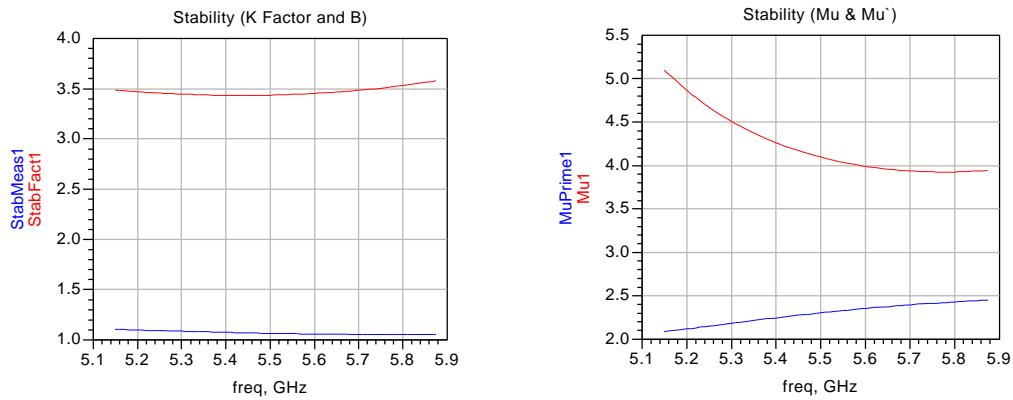


Figure 8. Complete Design – Narrow Band Stability Response

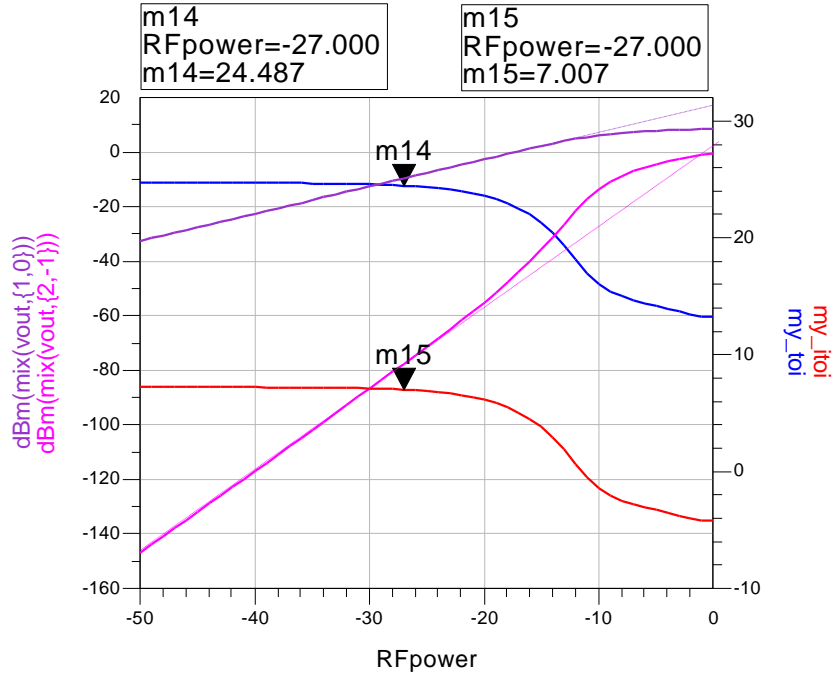


Figure 9. Complete Design – ITOI Response

RFpower	my_toi	my_itoi
-50.000	24.702	7.222
-49.000	24.702	7.222
-48.000	24.702	7.222
-47.000	24.701	7.221
-46.000	24.701	7.221
-45.000	24.700	7.220
-44.000	24.699	7.219
-43.000	24.698	7.218
-42.000	24.696	7.217
-41.000	24.695	7.215
-40.000	24.692	7.213
-39.000	24.690	7.210
-38.000	24.686	7.206
-37.000	24.682	7.202
-36.000	24.676	7.196
-35.000	24.669	7.189
-34.000	24.660	7.180
-33.000	24.649	7.169
-32.000	24.635	7.155
-31.000	24.617	7.137
-30.000	24.595	7.115
-29.000	24.567	7.087
-28.000	24.534	7.052
-27.000	24.487	7.007
-26.000	24.431	6.951
-25.000	24.361	6.881
-24.000	24.272	6.792
-23.000	24.161	6.681
-22.000	24.021	6.541
-21.000	23.845	6.365
-20.000	23.624	6.144
-19.000	23.346	5.866
-18.000	22.996	5.516
-17.000	22.556	5.076
-16.000	22.002	4.523
-15.000	21.305	3.826
-14.000	20.431	2.951
-13.000	19.357	1.877
-12.000	18.130	0.650
-11.000	16.950	-0.529
-10.000	16.050	-1.430

Figure 10. Complete Design – Tabulated ITOI Response, +7dBm @ -27dBm input Power

### 3. Schematic

#### 3.1. RF Schematic

#### 3.2. Simplified DC Schematic

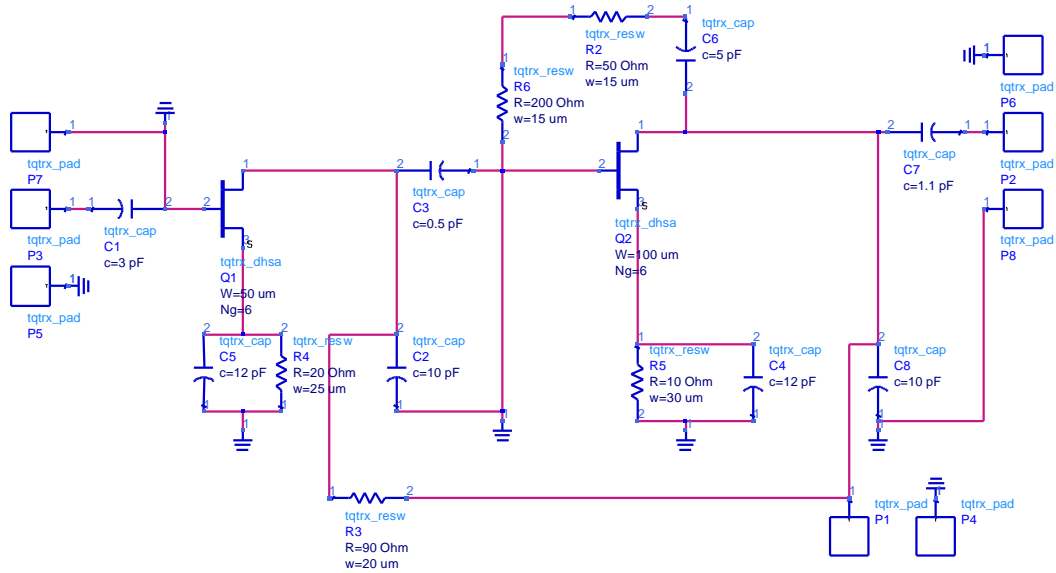


Figure 11. Simplified DC schematic of C-Band LNA

#### 3.3. Bias Check

This C-Band LNA uses a single drain bias to supply voltage to both DFET stages. Table 2 summarizes the biasing scheme for each stage. Figures 1 & 2 show the DC test bench for each DFET stage. The first stage was chosen to operate around  $2V_{ds}$ , however, after implementing the self-bias network, it reduced to 1.85V. Similarly, after the self bias network was added to the second stage,  $V_{ds}$  reduced to 2.73.

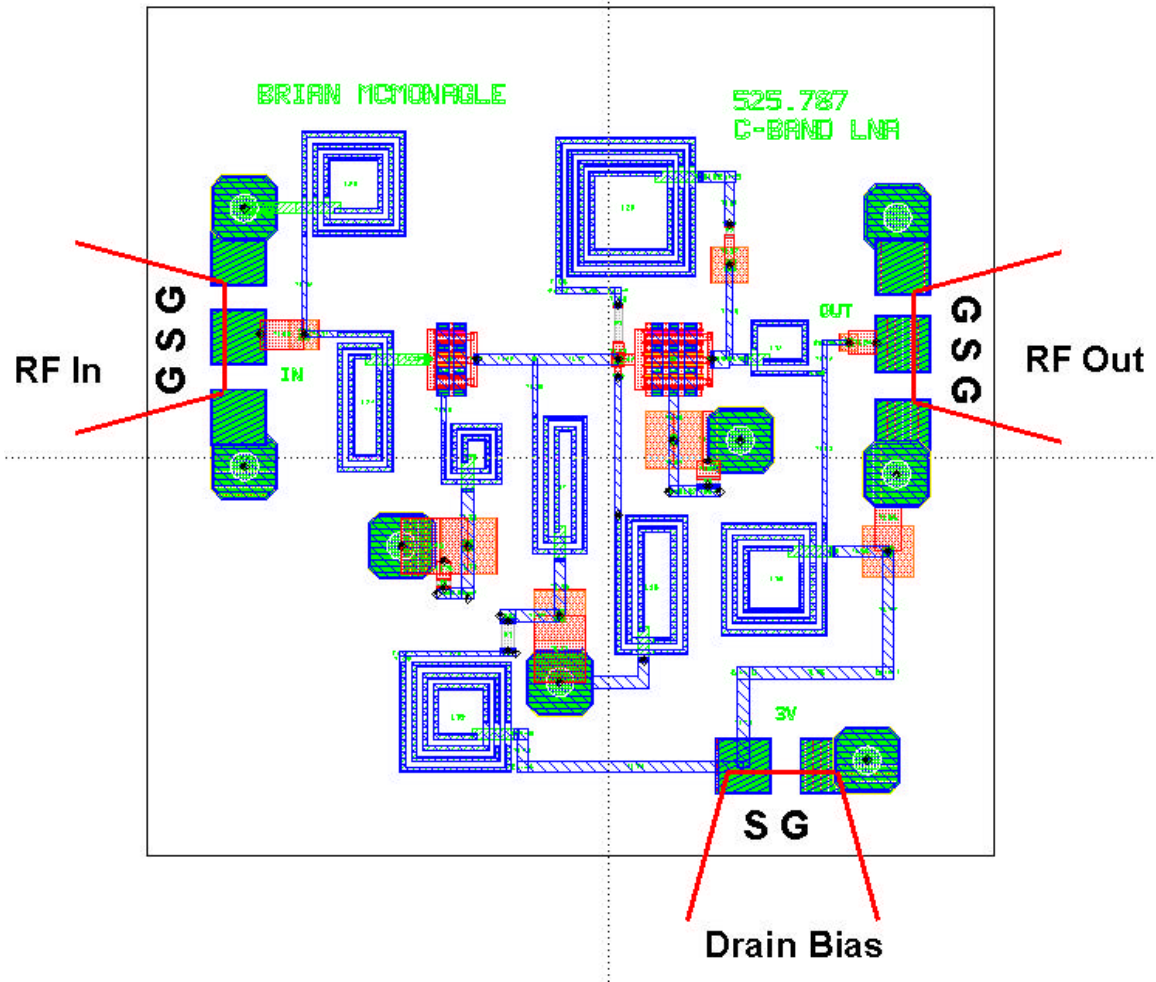
Table 2: Modeled DFET DC Parameters

Stage	Size	V <sub>gs</sub>	V <sub>ds</sub>	I <sub>ds</sub>
1	300 μm	-0.211V	1.85V	10.1mA
2	600 μm	-0.215V	2.73V	21.5mA

## 4. Layout

### 4.1. Final C-Band LNA Layout

Figure 12. C-Band LNA layout showing bond pad configuration



## 5. Test Plans

Design verification for the C-Band LNA will involve measuring small signal s-parameters, noise figure, IP3, and DC parameters. The LNA design uses two 125 $\mu$ m pitch GSG probes for both of its RF contacts (East and West sides of the MMIC). The DC supply will make contact from the south side of the MMIC using a common 125 $\mu$ m SG probe.

### 5.1. Test Equipment

The following test equipment will be needed to fully characterize the LNA design.

- Agilent 8510 Network Analyzer (or comparable 2-port VNA)
- Agilent C-Band Noise Figure Meter with C-Band Noise Diode
- Simple DC Power Supply
- Spectrum Analyzer
- Two (2) Signal Generators
- Agilent Power Meter

### 5.2. Turn On Procedure

When testing the LNA, care should be taken that the LNA does not get overstressed with drain voltage. Also, to help protect the design from excessive current draw due to possible layout errors or defects, set the current limit of the supply to twice the nominal current pull. Since this LNA is designed to operate at 32mA, the current limit on the DC supply to approximately 65mA. With the LNA correctly probed, as shown in Figure 12, ramp the drain voltage of the DC supply slowly up to the required +3V operating voltage.

### 5.3. RF Measurements

Calibration needs to perform on all test equipment prior to test. Since the LNA will be probed, the VNA should be calibrated from 1–10GHz, 201 points, using a SOLT calibration standard. The noise figure test set and IP3 test set should also be calibrated. When calibrating the noise figure meter, reducing the amount of connector loss in the system this will increase the accuracy of the noise figure measurement.

#### 5.3.1. S-Parameter Measurements

After calibrating the VNA, connect the RF and DC probes up to the LNA as shown in Figure 12. Following the “*Turn On Procedure*” for the MMIC, record the current draw off the power supply and make S11, S21, S12, and S22 measurements.

### 5.3.1. Noise Figure Measurements

After calibrating the noise figure test set such that the amount of calibrated loss is minimized, record the NF from 1–10GHz. Make note of the current and gain while recording the data.

### 5.3.1. IP3 Measurements

After calibrating the IP3 test bench, set the tone frequency separation to 10MHz, i.e.  $f_1=5.5\text{GHz}$ ,  $f_2=5.51\text{GHz}$ . This will ensure that the gain at each tone frequency will be exactly equal. Next, set the power levels of the two tones equal to one another. Start with the power levels set to a low level, i.e.  $-15\text{dBm}$ . Using a spectrum analyzer, increase the power levels of the two tones and look for the third order products to be at least 5 to 10dB above the noise floor. Record the delta between the third order products and the fundamental tones – these are the third order intercept (TOI) values. To get the input TOI (ITOI) values subtract off the gain at the fundamental tone frequency. Record these ITOI values at various in-band frequencies.

## 6. Summary & Conclusion

The design of a C-Band,  $0.6\text{mm}$  MESFET low noise amplifier MMIC was described. The LNA design was simulated using ADS with TriQuint Semiconductor's large signal DFET models. These models produced an LNA with simulated gain greater than 17dB, noise figure less than 1.6dB, and an ITOI of +7dBm. Optimizing and compacting the various matching networks realized the C-Band LNA into a 60x60 mil ANACHIP footprint.