C-Band Low Noise Amplifier
Final Report
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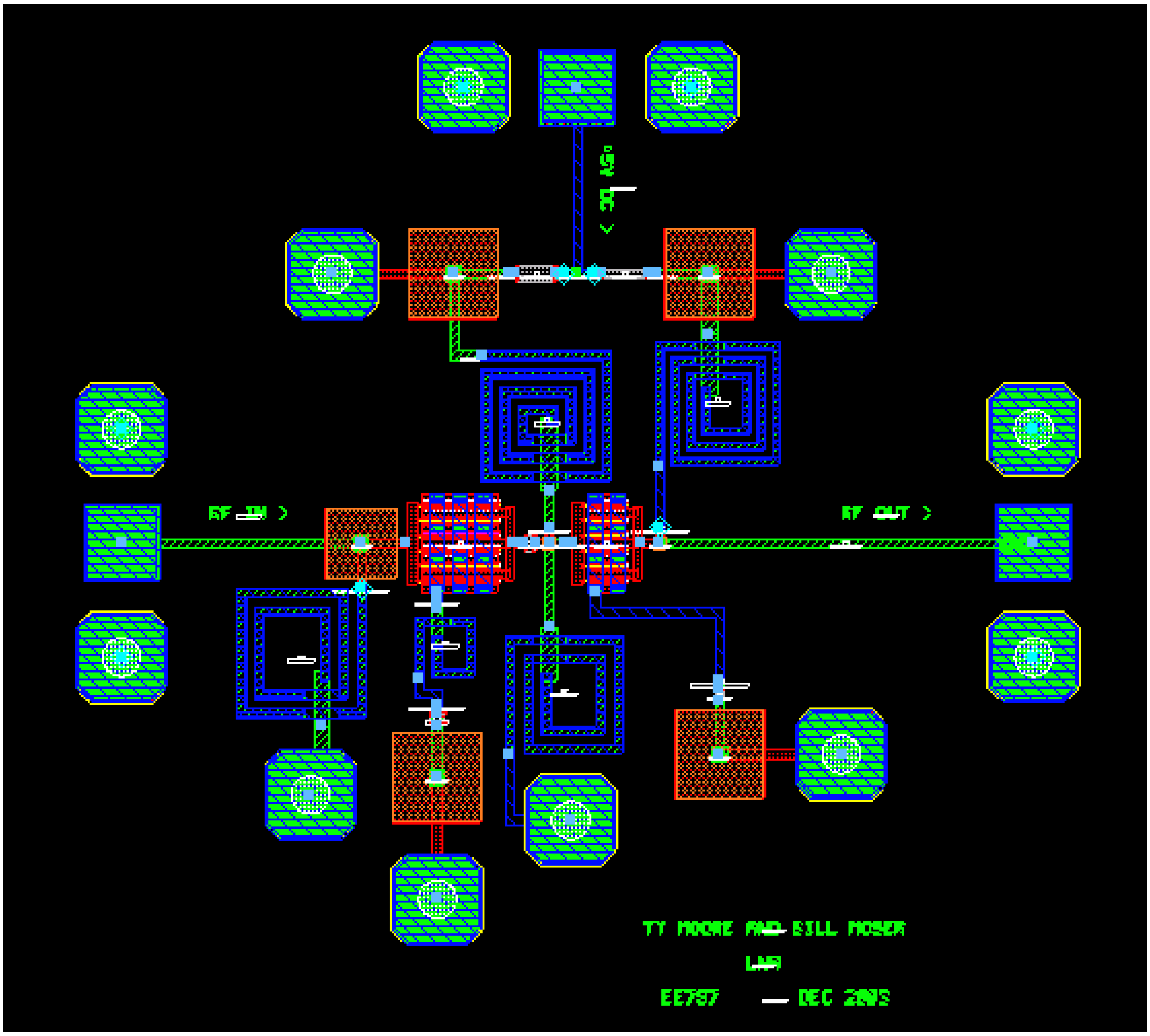

Bill Moser bill.moser@ngc.com
Ty Moore glenn.moore@jhuapl.edu

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Abstract

A GaAs Monolithic Microwave Integrated Circuit (MMIC) Low Noise Amplifier (LNA), operating at C-band has been designed using Agilent Advanced Design System (ADS 2003a) with TriQuint Semiconductor linear and non-linear models. The LNA is an integral part of a Simplex Transceiver chipset being developed by Professors and Students of the Johns Hopkins University, Whiting School of Engineering MMIC Design course. This paper details the design, design philosophy, design trade-offs and simulated performance of the LNA.

Introduction

The Simplex Transceiver operates in the Industrial, Scientific, and Medical (ISM) band with an RF center frequency of 5800 MHz, a 3 dB bandwidth of 150 MHz and a transmit power of ¼ Watt. The transceiver IF is 0.5 to 20 MHz and the modulation format is QPSK. The LNA is one of nine unique designs that make up the Transceiver system. Figure 1 is a block diagram of the Transceiver system.

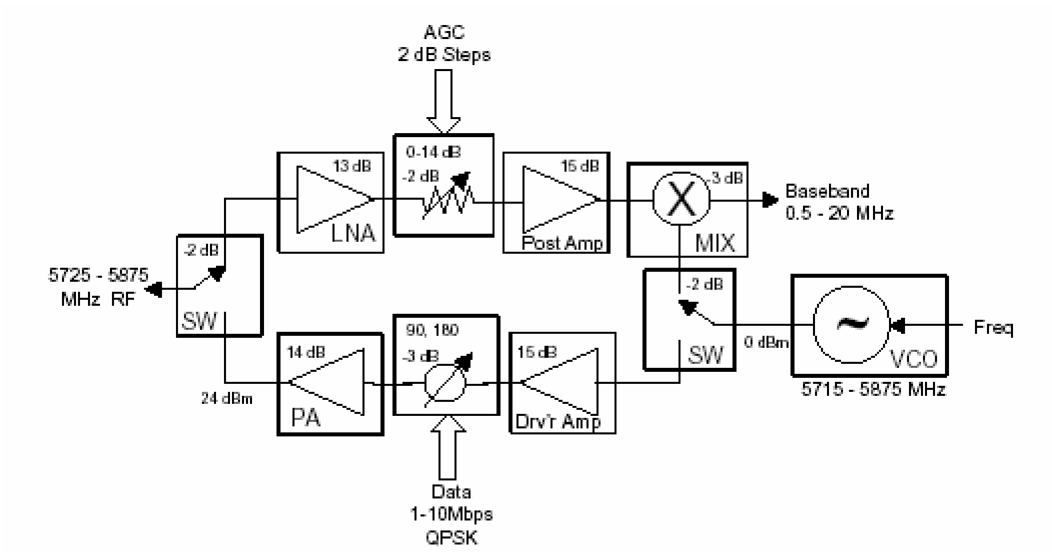

Figure 1 Simplex Transceiver Block Diagram

The RF downconverter chain noise figure is set by the noise figure of the LNA and the insertion loss of the Transmit / Receive Switch. The required LNA noise figure is 3 dB and the insertion loss of the T/R switch is 2 dB for a system noise figure of 5 dB. The required LNA gain is 13 dB, with a gain ripple of ± 0.5 dB. Input and output Voltage Standing Wave Ratio (VSWR) is specified at 1.5:1.

Circuit Description

To meet the gain specification of 13 dB a two stage design is required. The first stage is a 600 μM DJFET (6 fingers, each 100 μM wide), with Ids ≈ 15 mA. The 600 μM DJFET was chosen to provide significant gain in the first stage while providing a reasonable noise figure. The second stage is a 300 µM DJFET (6 fingers, each 50 µM wide) with Ids ≈ 7.5 mA. A self bias configuration was chosen so that a single +5.0 Volt power supply could be used. Both FETs were biased with Vds = 2.7 V and Vgs = -0.3V. Source inductances were included on both stages for stability as well as a series stabilizing resistor on the drain of the first stage. All matching networks are included on chip.

Design Philosophy

Design of the LNA began by selecting the proper bias points for both FETs. Simulation of the FET dynamic load lines was performed using the TriQuint DJFET non-linear model. Next stability of both amplifier stages was verified as individual stages. To stabilize the first stage a source inductance of 250 pH was required along with a 20Ω series drain resistor. The second stage required a 500 pH source inductance. With the bias points and stabilizing components determined the input match of the first stage was designed for a 2.5 dB noise figure and VSWR < 1.5:1 using ideal lumped elements and the 300 µM DJFET linear S2P file. This provided a 0.5 dB noise figure margin for losses induced by the TriQuint lumped elements and microstrip traces. The 600 µM DJFET was simulated by using two 300 µM S2P files in parallel. With the input match determined the output match of the second stage was then designed to provide an output VSWR < 1.5:1. With the input and output matches determined, the interstage match was designed so that a conjugate match was presented to each amplifier. Fortunately, a simple highpass Π network provided a good match and convenient bias injection points. With the LNA now designed, stability, noise figure, gain, input and output VSWR were checked and component values adjusted as required to meet the specifications. After all specifications were met with margin the FET non-linear models were installed and the amplifier configured for self bias operation with a single power supply. Again the ideal components were adjusted so that the specifications were met with margin then replaced with TriQuint lumped elements and substrate vias. The TriQuint elements were adjusted so that the specifications were met with margin and then layout of the LNA on a 60 mil x 60 mil die (ANACHIP) began. As microstrip traces were inserted in the design the lumped elements were tuned to compensate for the degradation in performance. As the layout was performed care was taken to separate components by at least 24 µM (two trace widths) and to keep trace lengths to a minimum. Input and output pads were added to the design in a Ground – Signal – Ground orientation so that the probing station probes could be used for testing the die.

Trade-offs

Designing an LNA consists of trading gain, stability, N.F., input and output match. As the input match is altered to provide the best noise figure the gain is reduced and the input VSWR becomes larger. Stability can also be affected by the input and output match. During the design process unconditional stability over all frequencies was treated as the most important parameter. After unconditional stability was achieved the design was altered to achieve a noise figure with 0.5 dB margin. The 600 µM DJFET chosen for the first stage provided ample gain, so trading gain was not an issue. Obtaining a 1.5:1 input VSWR while maintaining a 2.5 dB noise figure was the most challenging part of the design.

Modeled Performance

Simulations of the design indicate that all specifications have been met. The following sections detail the simulation results.

Specification Compliance

Table 1 is a Specification Compliance Matrix which details the design specifications, simulated results of the simplified design, simulated results of the final design / layout and the design margin. All specifications have been met or exceeded.

Parameter	Specification	Simplified Design w/ TriQuint Components	Final Design and Layout	Margin
Operating Frequency	5725 to 5875 MHz	5725 to 5875 MHz	5725 to 5875 MHz	N/A
Bandwidth (3dB)	> 150 MHz	> 1 GHz	> 1 GHz	> 850 MHz
Gain	> 13 dB	17.6 dB	17.0 dB	4.0 dB
Gain Ripple	± 0.5 dB max	- 0.3 dB	± 0.3 dB	± 0.2 dB
Noise Figure	< 3dB	2.75 dB	1.9 dB	1.1 dB
Output IP3	> +5 dBm	+25 dBm	+24 dBm	19 dBm
Input VSWR	< 1.5:1	1.34:1	1.275:1	4 dB
Output VSWR	< 1.5:1	1.09:1	1.21:1	5.5 dB
Supply Voltage	± 5 Volts; +5 Volt, goal	+5 Volt	+5 Volt	N/A

Table 1
Specification Compliance Matrix

Predicted Performance

The LNA gain is required to be at least 13 dB with a maximum gain ripple of ± 0.5 dB and a 3 dB bandwidth of > 150 MHz. The following figures illustrate the simulated performance of the simplified design.

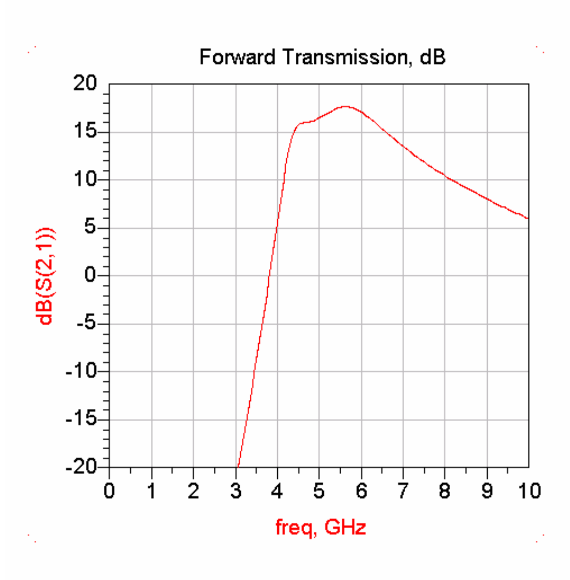

Figure 2 Gain - Simplified Schematic

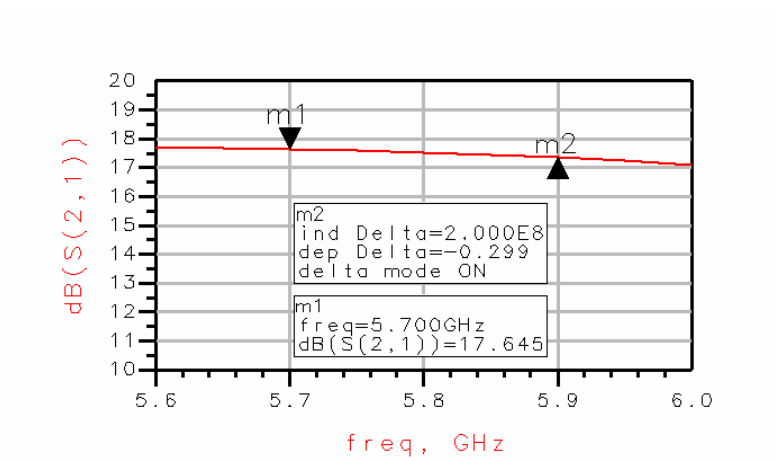

Figure 3 Gain Ripple – Simplified Schematic

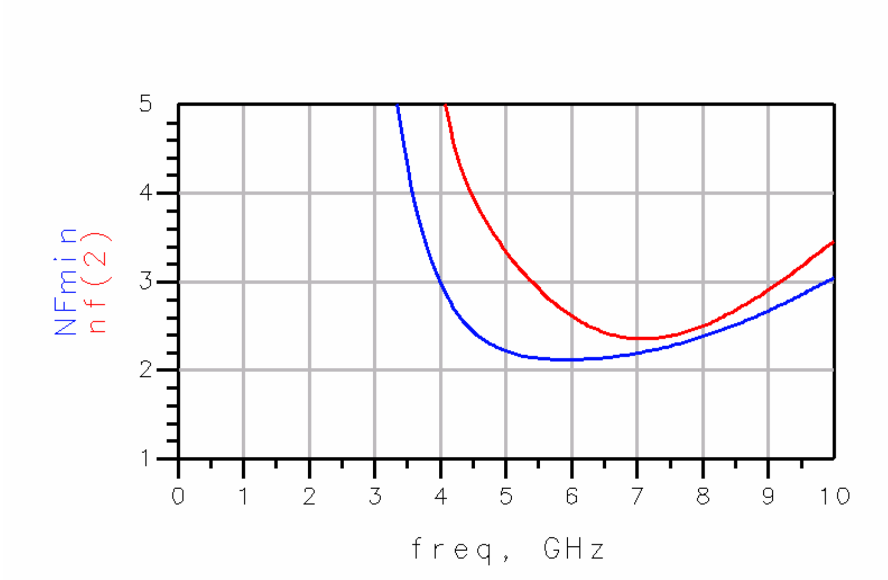

Figure 4 Noise Figure – Simplified Schematic

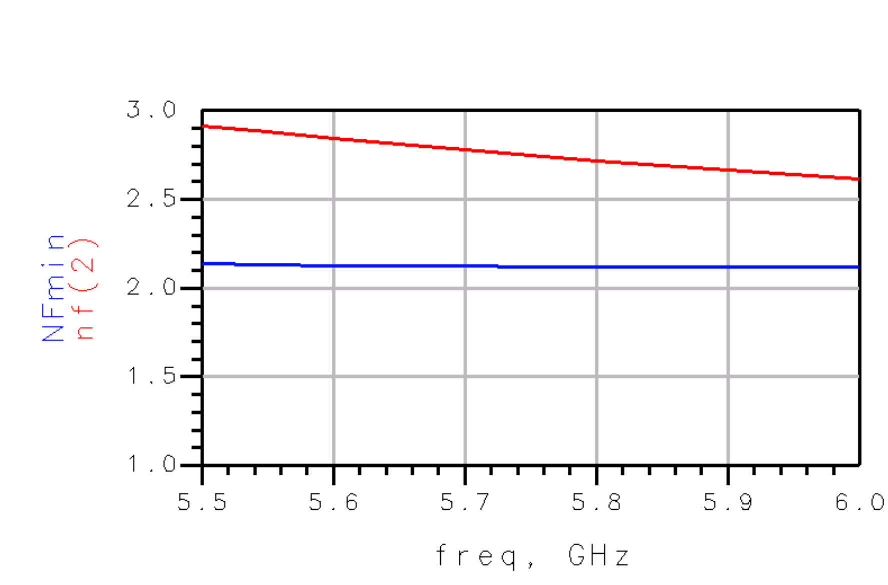

Figure 5 Noise Figure over 3 dB Bandwidth– Simplified Schematic

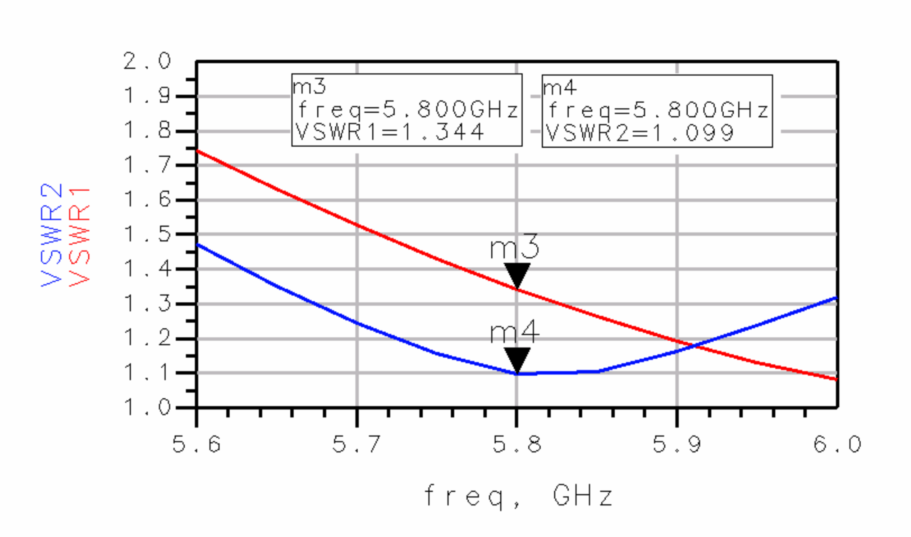

Figure 6 Input and Output VSWR – Simplified Schematic

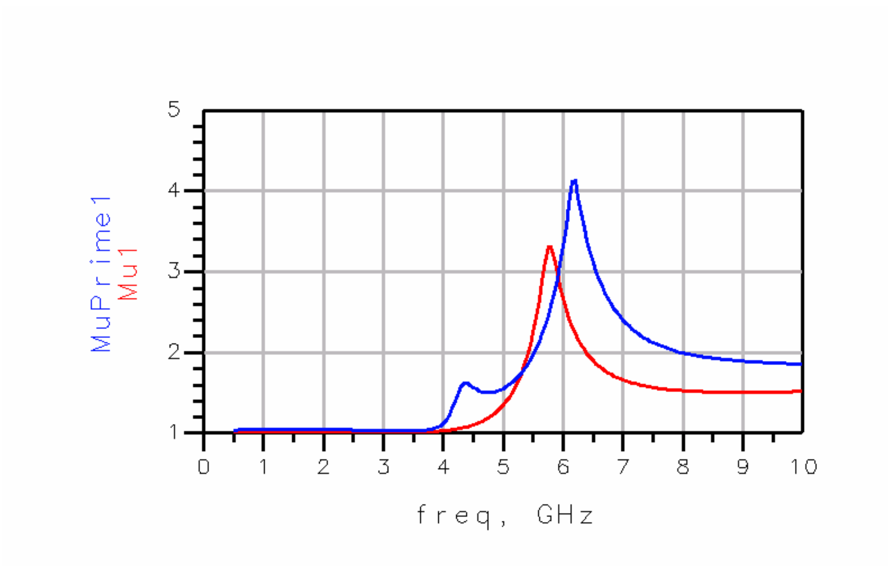

Figure 7 Stability – Simplified Schematic

The following figures illustrate the performance of the completed LNA including all microstrip connections.

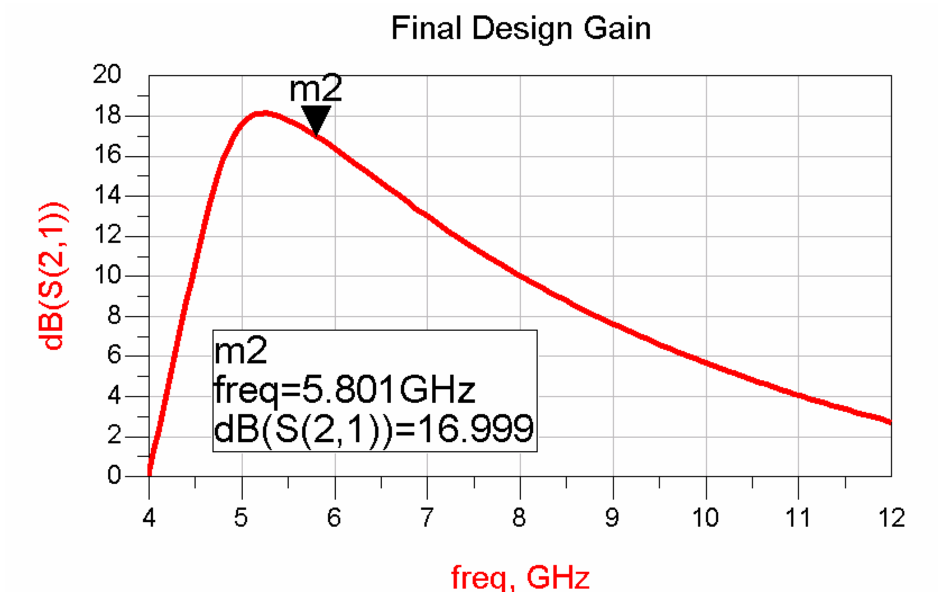

Figure 8 Gain – Complete Design

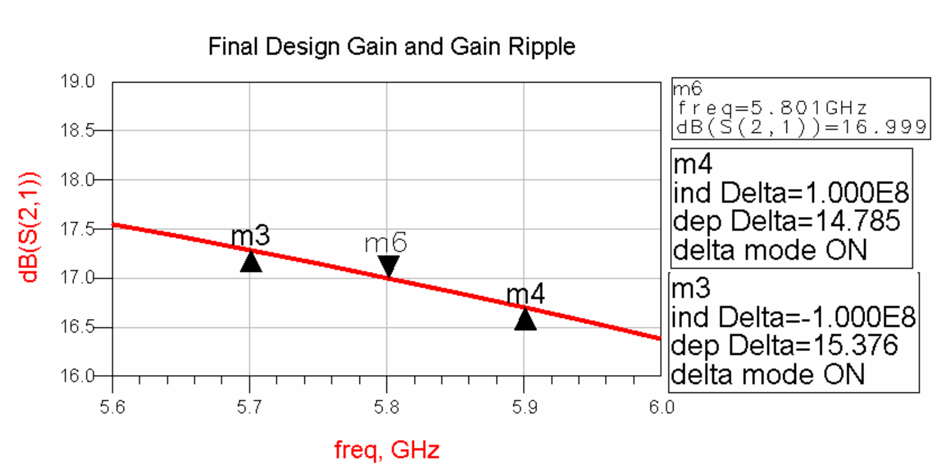

Figure 9 Gain Ripple – Complete Design

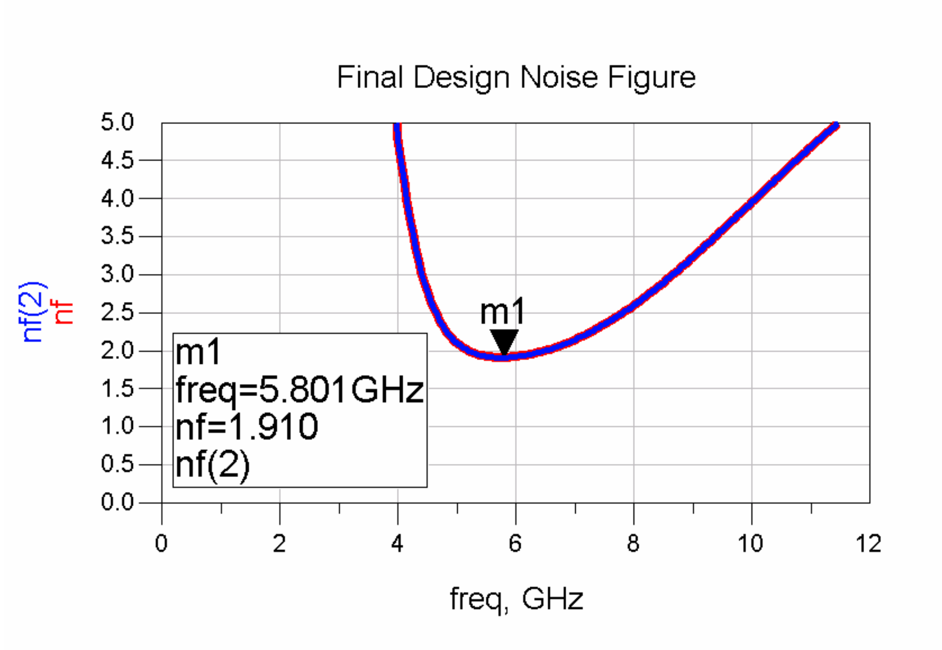

Figure 10 Noise Figure – Complete Design

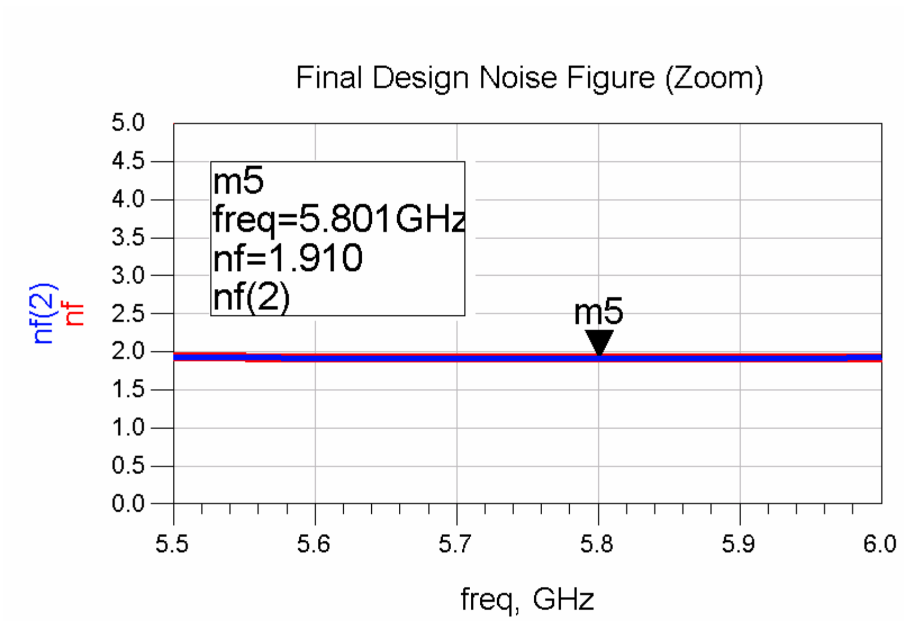

Figure 11 Noise Figure Over 3 dB Bandwidth – Complete Design

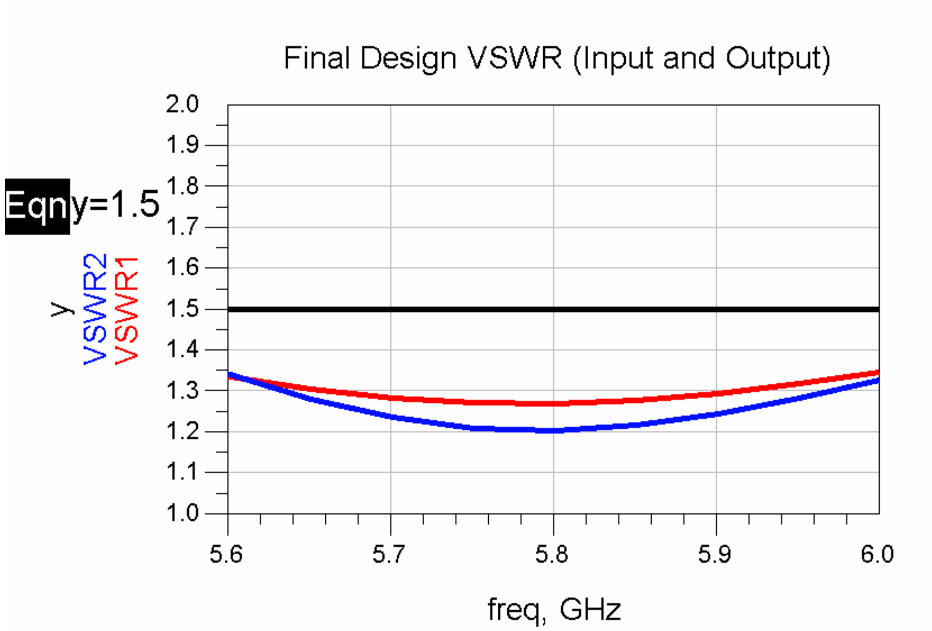

Figure 12 Input and Output VSWR– Complete Design

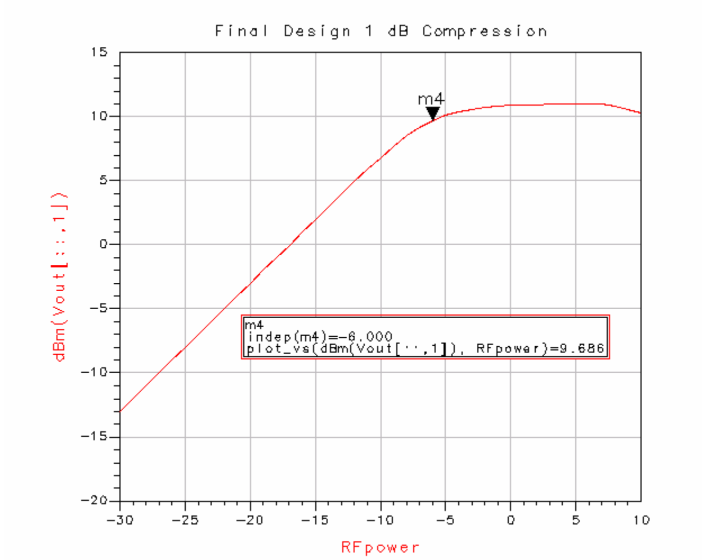

Figure 13 1 dB Compression – Complete Design

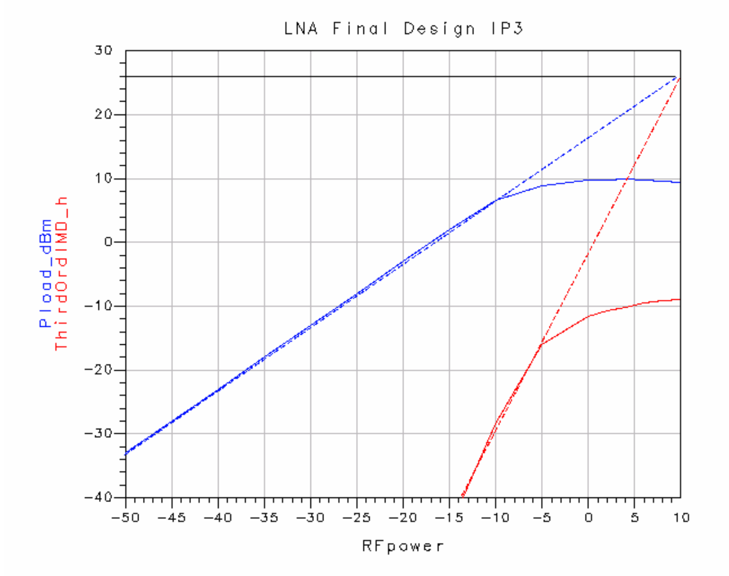

Figure 14 IP3 – Complete Design

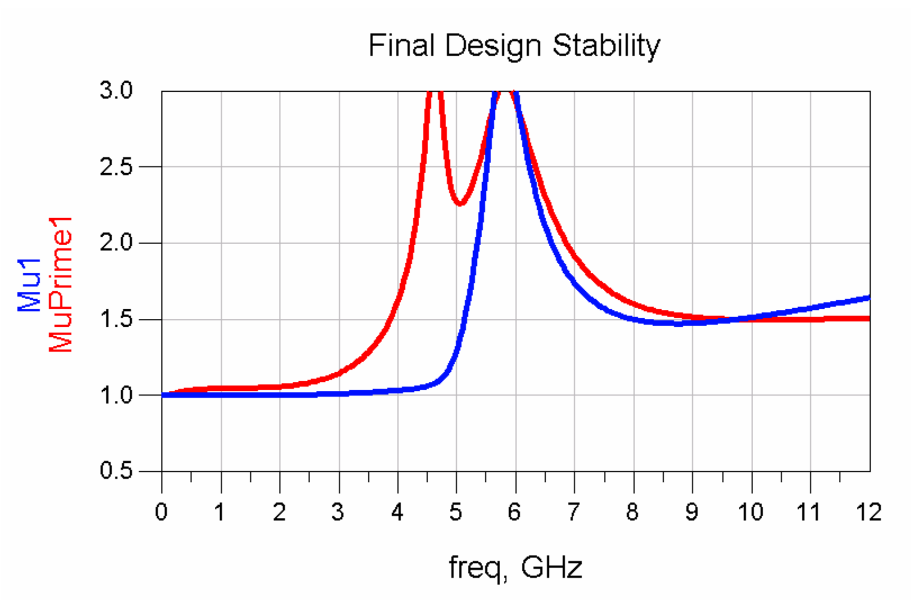

Figure 15 Stability – Complete Design

Schematic Diagrams

Simplified Schematic

Figure 16 is a schematic diagram of the design with TriQuint components, prior to layout.

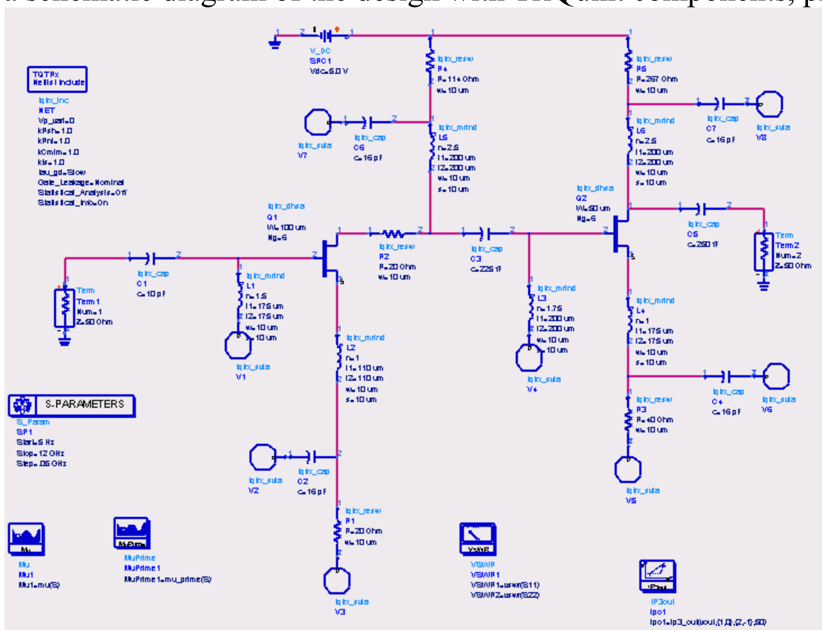

Figure 16 Simplified Design Schematic

Complete Design

Figures 17 and 18 are schematic diagrams of the final design with TriQuint components and microstrip traces. Two figures were used for clarity.

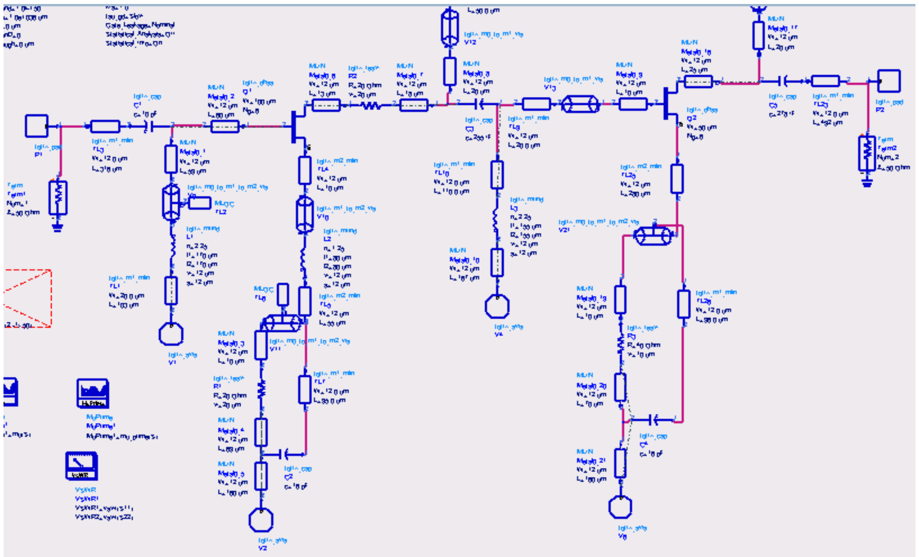

Figure 17 Final Design Schematic

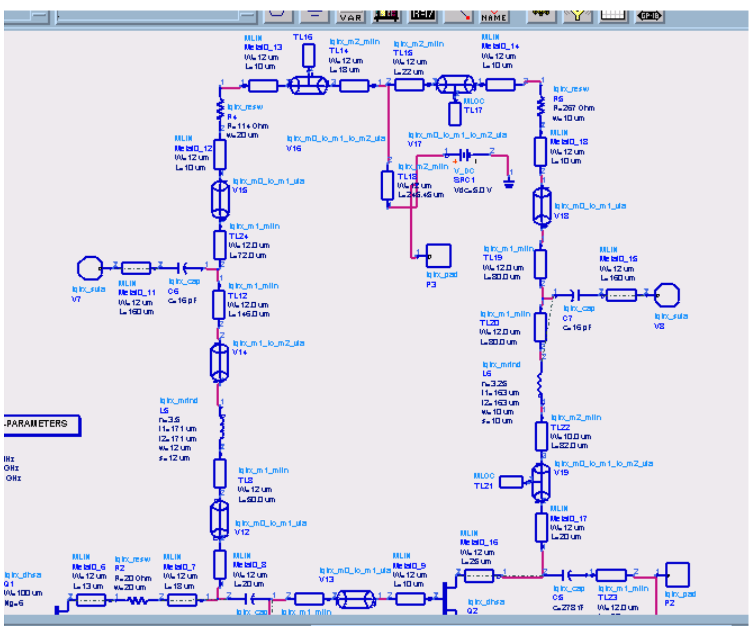

Figure 18 Final Design Schematic Continued

Final Layout

Layout of the LNA was performed with TriQuint components and microstrip traces. Interconnects were routed on Metal 1 and Metal 2 wherever possible. Those interconnects routed on Metal 0 were kept as short as possible and are 12 µM wide to provide ample current carrying capability (1.5 mA/µM = 18 mA). As microstrip traces were inserted in the design the lumped elements were tuned to compensate for the degradation in performance. This required the replacement of the second stage shunt source stabilizing inductor with a microstrip trace. As the layout was performed care was taken to separate components by at least 24 µM (two trace widths). Input and output pads were added to the design in a Ground – Signal – Ground orientation so that the probing station probes could be used for testing the die.

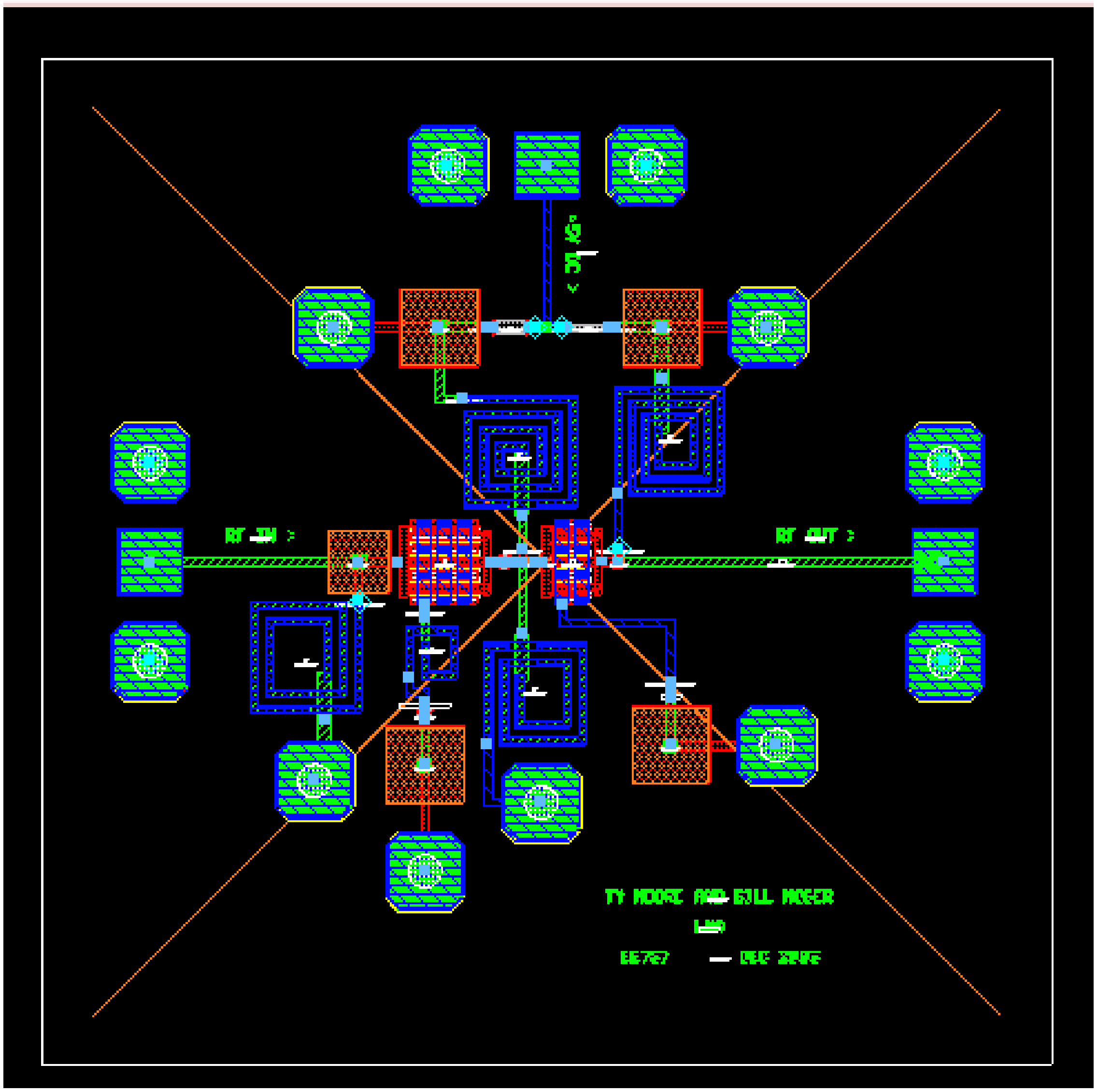

Figure 19 Final Design Layout

DC Analysis

Simplified Schematic

The input stage was designed to provide ample gain for the amplifier so that the noise figure would not be compromised by the output stage. As such, the input FET was scaled to twice the output FET (600 µM vs 300 µM) and biased so that Ids was also two times that of the output stage. Table 2 details the DC operating points of the LNA simplified design and Figure 20 is a DC annotated schematic.

Stage 1	Stage 2
Vds = 2.721 V	Vds = 2.737 V
Vgs = 0.299 V	Vgs = 0.293 V
Ids = 14.6 mA	Ids = 7.32 mA

Table 2 Simplified Schematic DC Operating Points

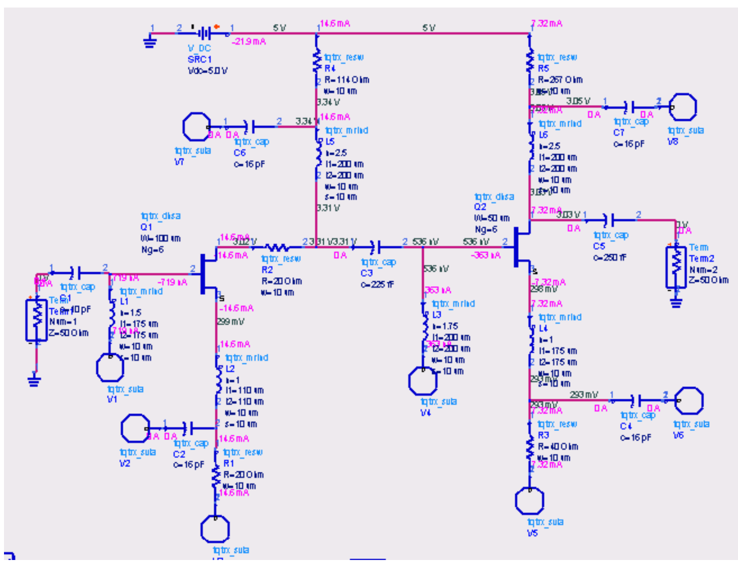

Figure 20 Simplified Design DC Operating Points

Complete Design

Table 3 details the DC operating points of the LNA complete design and Figure 21 is a DC annotated schematic.

Stage 1	Stage 2
Vds = 2.727 V	Vds = 2.714 V
Vgs = 0.293 V	Vgs = 0.296 V
Ids = 14.7 mA	Ids = 7.4 mA

Table 3 Complete Design DC Operating Points

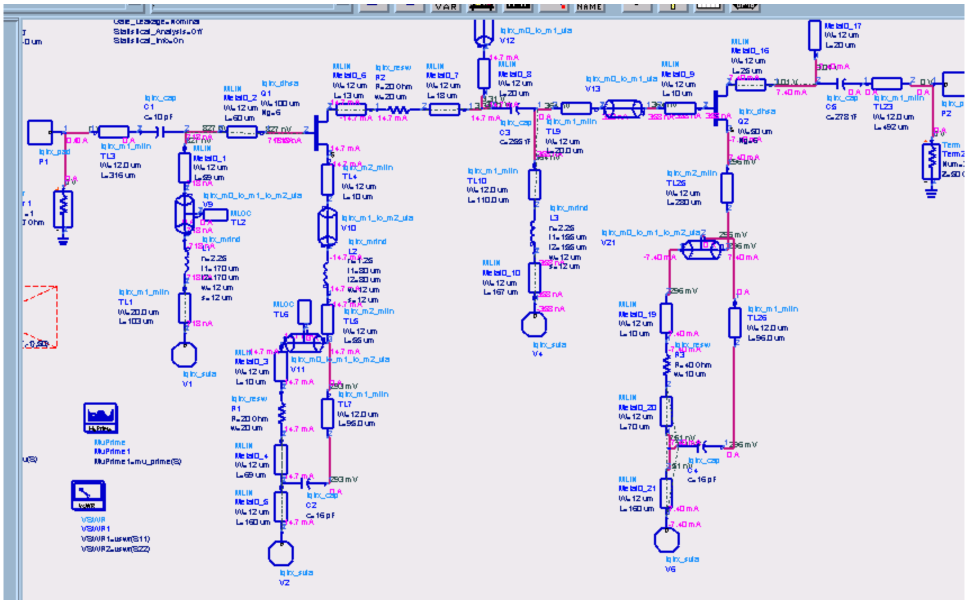

Figure 21 Final Design DC Operating Points

Component Stress

A maximum current of 15 mA is drawn by the first stage, so the resistors in this stage were sized to handle 20 mA by setting the width to 20 µM (1mA/µM). The second stage resistors carry 7.5 mA and are 10 µM wide. The overall power consumption for the die is approximately 110 mW (5 Volts @ 22 mA).

Test Plan

Verification of the LNA will require tests for noise figure, gain, VSWR (input and output), 3 dB bandwidth and power consumption. Noise figure shall be verified with a Noise Figure Meter capable of operating at 5.8 GHz while the remaining RF tests shall be performed with a Network Analyzer such as an Agilent 8510. Power consumption shall be verified by monitoring the current and voltage supplied to the die.

Test Configuration

A probing station with a Ground – Signal – Ground probe orientation is required to inject the RF signal and monitor the LNA output. An additional probe is required to provide bias to the LNA.

Turn On Procedure

Set the dc power supply for 5.0 Volts.
Set the current limit for 30 mA.
Apply power to the die.

S-Parameter Measurement

Perform a full calibration on the network analyzer from 1 to 10 GHz.

Connect the bias probe to the +5V IN pad.
Connect the input probe to the RF IN pad.
Connect the output probe to the RF OUT pad.
Perform the Turn On Procedure.
Measure S21 of the LNA and store the measurement data.
Measure S11 of the LNA and store the measurement data.
Measure S22 of the LNA and store the measurement data.
Turn off power supply.

Noise Figure Measurement

Perform a calibration on the noise figure meter at 5.8 GHz.
Connect the bias probe to the +5V IN pad.
Connect the input probe to the RF IN pad.
Connect the output probe to the RF OUT pad.
Perform the Turn On Procedure.
Measure the noise figure of the LNA and store the measurement data.
Turn off power supply.

Conclusion and Recommendations

The design of a GaAs Low Noise Amplifier operating at C-band has been completed. The LNA design meets or exceeds all design criteria in simulation and it is expected the TriQuint fabricated die shall as well. Measurements of the manufactured die will be performed, compared to the simulated results and published at a later date.