

S-BAND LOW NOISE AMPLIFIER (LNA)

FINAL PROJECT REPORT

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1.0 Summary

A Low Noise Amplifier (LNA) operation at S-Band (2.3GHz to 2.5GHz) has been design as part of a project for the MMIC course at the John Hopkins University. The project is a duplex transceiver employing a receive array for the S-Band wireless communications service(WCS) and industrial, scientific, and medical (ISM) frequencies. The LNA is one of the nine unique designs. Each design is contained on a 60 mil square ANACHIP die using the TriQuint TQTRX design process, with vias, 4 mil (100 um) thick wafer and TOM3 FET model in ADS. Agilent Advanced Design Systems (ADS 2002) is used for the design software. The predicted LNA design achieved all design goals including gain greater than 15 dB, noise figure less than 3 dB (1.12dB MAX), input IP3 great than +5dBm (+7dBm), and input/output VSWR 1.5:1. The LNA will be fabricated by TriQuint and tested with in year 2003.

2.0 Introduction

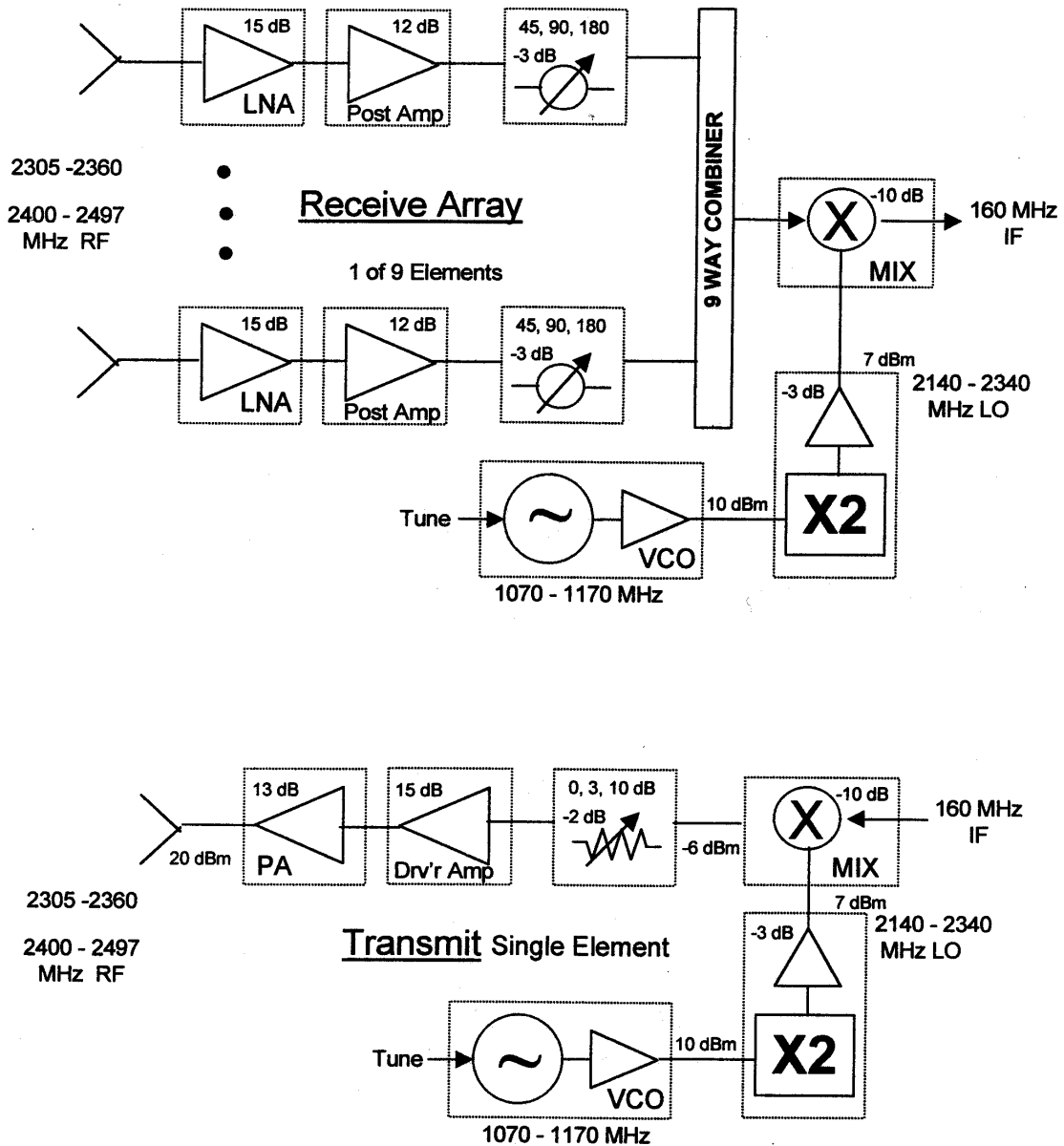
A Low Noise Amplifier (LNA) operation at S-Band (2.3GHz to 2.5GHz) has been design as part of a project for the MMIC course at the John Hopkins University. The project is a duplex transceiver employing a receive array for the S-Band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies. The LNA is one of the nine unique designs. Each design is contained on a 60 mil square ANACHIP die using the TriQuint TQTRX design process, with via, 4 mil (100 um) thick wafer and TOM3 FET model in ADS. Figure 1 is a chip set diagram for the 2305 – 2360 MHz WCS and 2400 – 2497 ISM Bands.

2.1 Circuit Description

The LNA circuit design was a cascaded two-stage amplifier. 600um DFET (12 fingers X 50um) is used for both stages. In order to achieve a single +5Volt power supply, self-biasing was used for both stages. A series inductor at each source of DFET was used for stabilization. High pass matching networks for input/output ports and inter-stage matching were used for reducing the number of entire chip elements. An active load (300um DFET) for each stage amplifier, which generated 20mA constant bias current, was used for saving chip area. A feedback RC circuit for each stage was added to achieve the better performance of gain, gain ripple and stabilization.

2.2 Design Philosophy

Based on its low noise figure and gain characteristics, we choose TriQuint DFET for the LNA design. According to the S-Parameter information of 300um DFET (standard S-parameter file at bias condition $I_{ds}=10mA$, $V_{ds}=2V$), two 300um DFETs paralleled together must be used for each stage because of LNA gain and IIP3 issues. From DC curve of 300um DFET, one can see that if $V_{gs}=0V$, $I_{DSS}=20mA @ V_{ds}=2.5V$. See figure 2. 300um DFET active load can be used base on the 300um DFET DC curve for



**Chip Set for the 2305 - 2360 MHz WCS and
2400 - 2497 MHz ISM Bands**

Figure 1: Chip set for the 2305 – 2360 MHz WCS and 2400 – 2497 MHz ISM Bands

each stage DC bias. The bias point we chosen for each stage of 600um DFET is same, listed as following Table 1:

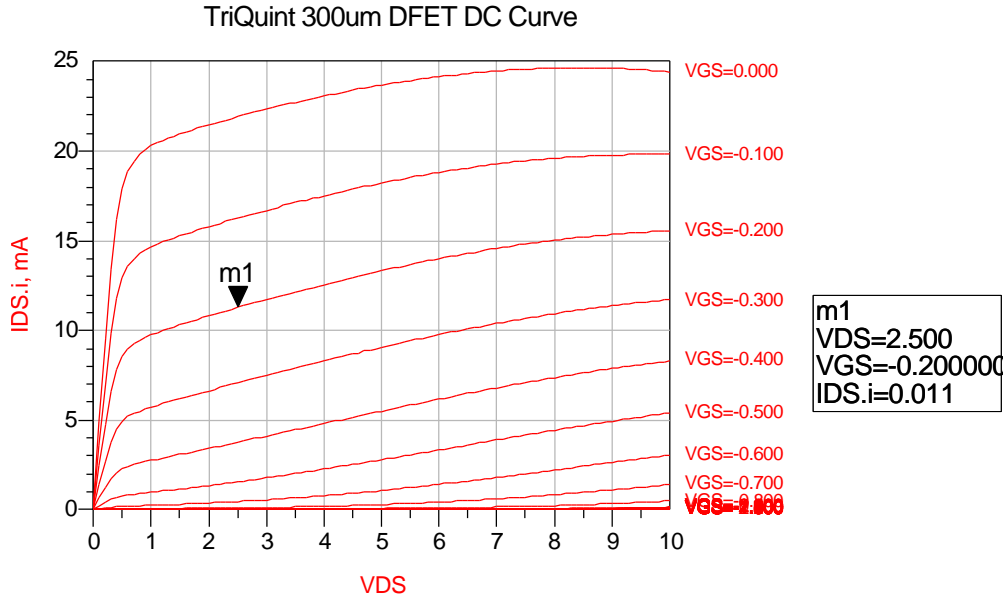


Figure 2: 300um DFET DC Curve

First stage	Second stage
Vds=2.5V	Vds=2.5V
Vgs=-0.17V	Vgs=-0.17V
Ids=20mA	Ids=20mA

Table 1: 600um DFET DC bias point

The design process was focused on achieving a stable design, the goals of high gain, low noise figure, high input IP3, lower gain ripple and good input/output port matching across a desired frequency band (2.3GHz to 2.4GHz). First, we need add an inductor to the source pin of DFET to stabilize it. The value, which we found is 2500 p μ H. Figure 3 shows the input and output stability circles at frequency 2.4GHz in Smith chart. Table 2 shows the stable factor K and Δ over the frequency range from 500MHz to 5GHz. $K > 1$ and $\Delta > 0$, that means the transistor is unconditional stable.

Gain, Noise, Input/Output stability circles

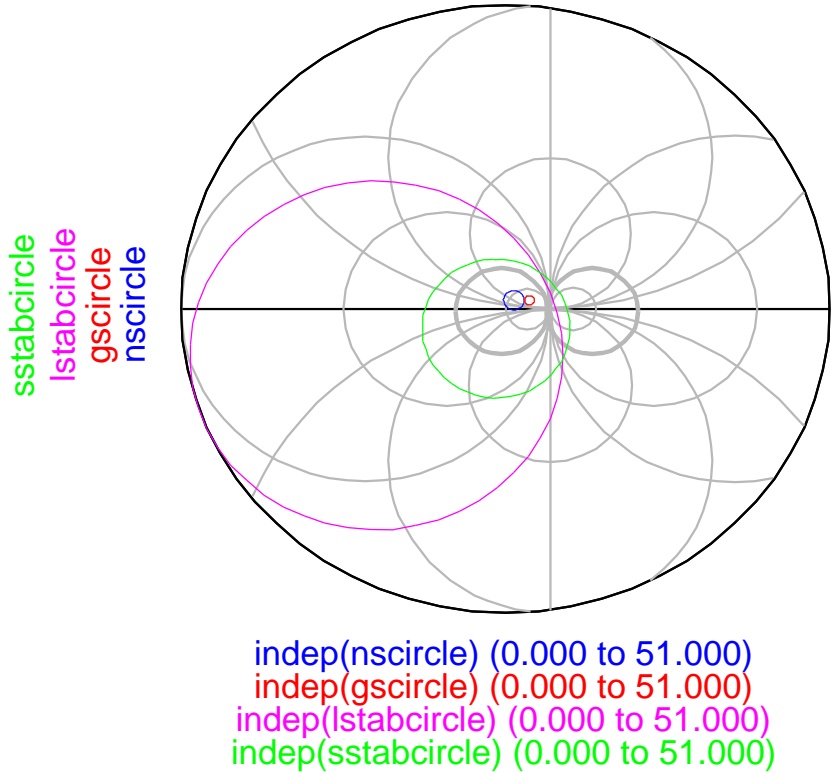


Figure 3: Input and Output stability circles with Gain and Noise Circles

freq	k	Δ
500.0MHz	1.113	1.018
1.000GHz	1.086	0.651
1.500GHz	1.071	0.463
2.000GHz	1.058	0.363
2.500GHz	1.045	0.297
3.000GHz	1.032	0.246
3.500GHz	1.020	0.200
4.000GHz	1.010	0.155

Table 2: Stable factor K and Delta

Second, in order to achieve as greater gain and lower noise figure as possible, a G_s gain circle and noise circle were drawn on one smith chart. See figure 4. An intersection point between G_s gain circle and noise circle is Γ_s . $\Gamma_s = 2.1+j1.15$. After Γ_s was found, an input matching network was calculated using high pass network. The reason using high pass network is to have few chip elements, so that chip area can be saved. The shunt inductor can be used as a part of matching network as well as self-bias inductor.

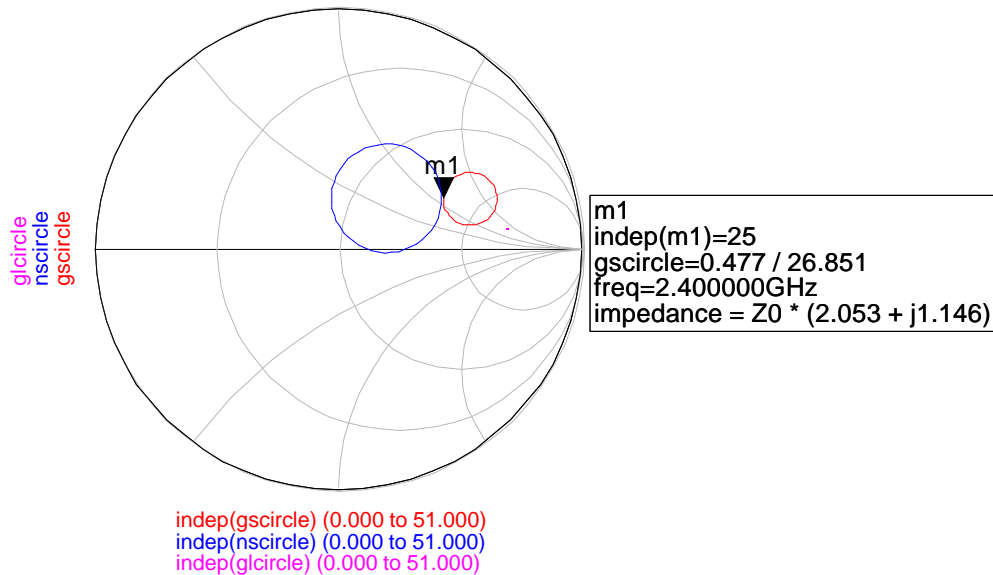


Figure 4: G_s gain circle and noise circle at $f=2.4$ GHz

Third, after input matching network was calculated, output matching network need to be calculated as well. In order to provide maximum power transfer to the load, Γ_L should equal to S_{22} conjugate. We found out S_{22} then the output matching network was calculated. Therefore single stage Low Noise amplifier was designed using 300um DFET S-parameter file. Because we only have 300um DFET S-parameter file, to get 600um DFET, two 300um DFET S-Parameter file need to be paralleled.

Now two single 600um DFET low noise amplifiers cascaded together to become one Low Noise Amplifier. The real TriQuint elements that would be required for the layout of final design replaced the ideal elements of the initial LNA design. We call this new one is a simplified schematic since there are no bends, tees MLINs which the final layout need them to finish the chip layout.

Do S-Parameter simulation of the simplified low noise amplifier, the simulation result (such as Gain, noise figure, VSWR and DC bias points) will be shown later at Section 3.2 Predicted Performance. This is the linear simulation using S-Parameter file. We need do a linear simulation with non-linear DFET model and harmonic balance non-linear simulation with non-linear DFET model for the non-linear performances of LNA such as P1dB and input IP3. Simply, replaced S-Parameter file by the non-linear model of 600um

DFET. Do simulation, the result will be shown later at Section 3.2 Predicted Performance.

Regarding layout, the layout process involves interconnection appropriate bends, tees, and MLINs to the optimized LNA design with TriQuint elements. General design guidelines include: keeping the separation as much more as possible between components, sharing vias as many as possible, making sure that a maximum allowable current through a resistor is 1 mA per 1um resistor's width. After finishing the layout, we need re-simulate the layout schematic (simplified amplifier plus bends, tees and MLINs) , if the simulation result is too much off that of the simplified amplifier schematic, we need re-tune the layout elements until the two simulation results are close enough.

2.3 Trade-offs

The major trade-off for designing low noise amplifier is the gain and the noise figure. It is not possible to get maximum gain and minimum noise figure at same time. Therefore, we need trade off the gain and noise figure to get more gain and less noise figure.

3.0 Modeled Performance

3.1 Specification Compliance Matrix

Table 2 shows the design specifications and the predicted performance for this LNA.

Table 3: Design Spec and Predicted Performance

Characteristic	Spec Goal	Simplified Schematic LNA performance	Final LNA predicted Performance
Frequency	2300 to 2500 MHz	2300 to 2500 MHz	2300 to 2500 MHz
Band width	> 200 MHz	> 200 MHz	> 200 MHz
Gain	> 15 dB	15.5 @ 2.4 GHz	16.5 @ 2.4 GHz
Gain ripple	±0.5 dB max	< ±0.5 dB	< ±0.5 dB
Noise figure	< 3 dB	1.2 dB	1.2 dB
Input IP3	>+5 dBm	+7 dBm	+7 dBm
VSWR, 50 Ohm	<1.5:1 input & output	1.4:1 max	1.6:1 max
Power supply voltage	+5 Volts only	+5 Volts only	+5 Volts only
Chip size	60 x 60 mil ANACHIP		60 x 60 mil ANACHIP

3.2 Predicted Performance

The following simulation results show the performances of this low noise amplifier.

Figure 5: S-Parameter performances of simplified schematic LNA (linear simulation using 300um DFET S-Parameter file)

Figure 6: Noise figure performance of simplified schematic LNA (linear simulation using 300um DFET S-Parameter file)

Figure 7: S-Parameter performances of simplified schematic LNA (linear simulation using 600um DFET non-linear TOM3 model)

Figure 8: P1dB performance of simplified schematic LNA (harmonic balance simulation using 600um DFET non-linear TOM3 model)

Figure 9: S-Parameter performances of final layout schematic LNA (linear simulation using 300um DFET S-Parameter file)

Figure 10: Noise figure performance of final layout schematic LNA (linear simulation using 300um DFET S-Parameter file)

Figure 11: S-Parameter performances of final layout schematic LNA (linear simulation using 600um DFET non-linear TOM3 model)

Figure 12: P1dB performance of final layout schematic LNA (harmonic balance simulation using 600um DFET non-linear TOM3 model)

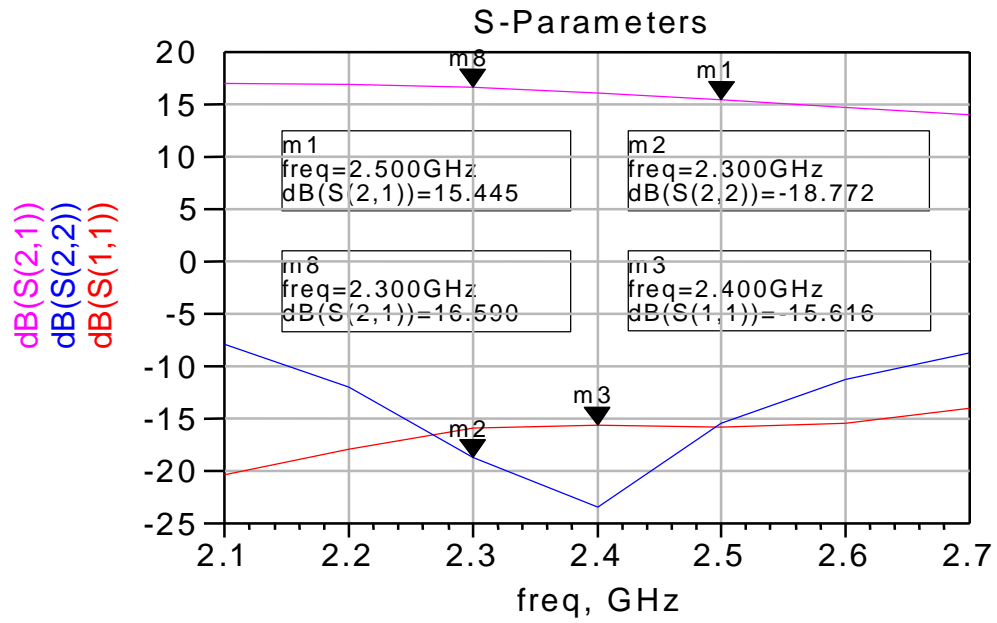


Figure 5: S-Parameter performances of simplified schematic LNA (linear simulation using 300um DFET S-Parameter file)

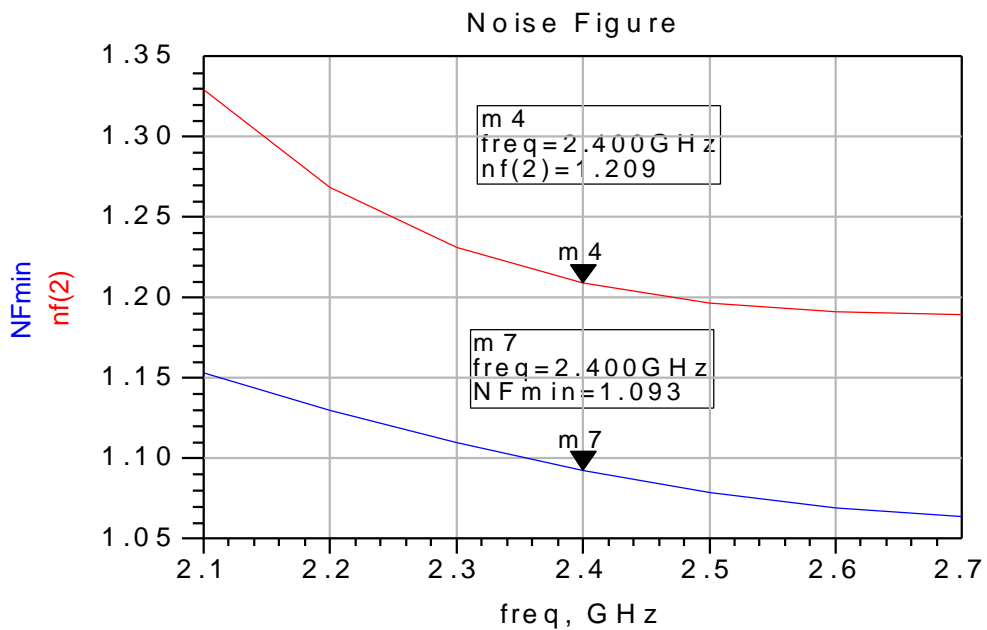


Figure 6: Noise figure performance of simplified schematic LNA (linear simulation using 300um DFET S-Parameter file)

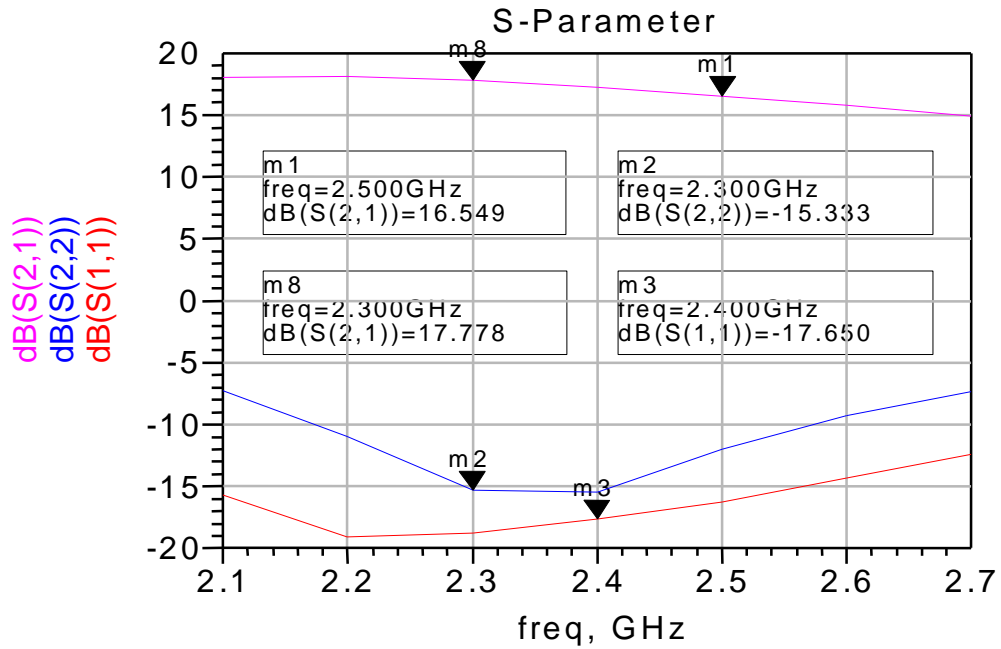


Figure 7: S-Parameter performances of simplified schematic LNA (linear simulation using 600um DFET non-linear TOM3 model)

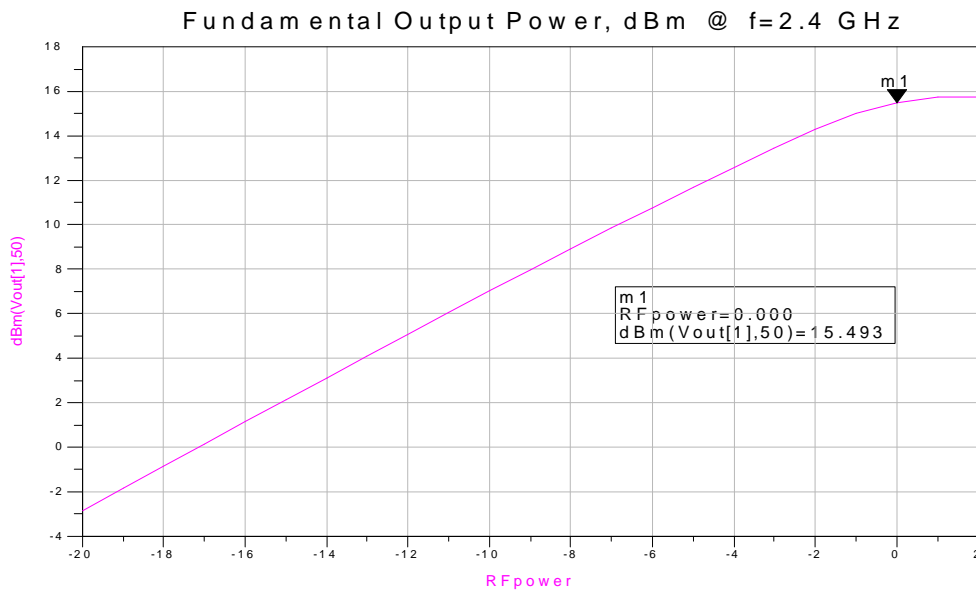


Figure 8: P1dB performance of simplified schematic LNA (harmonic balance simulation using 600um DFET non-linear TOM3 model)

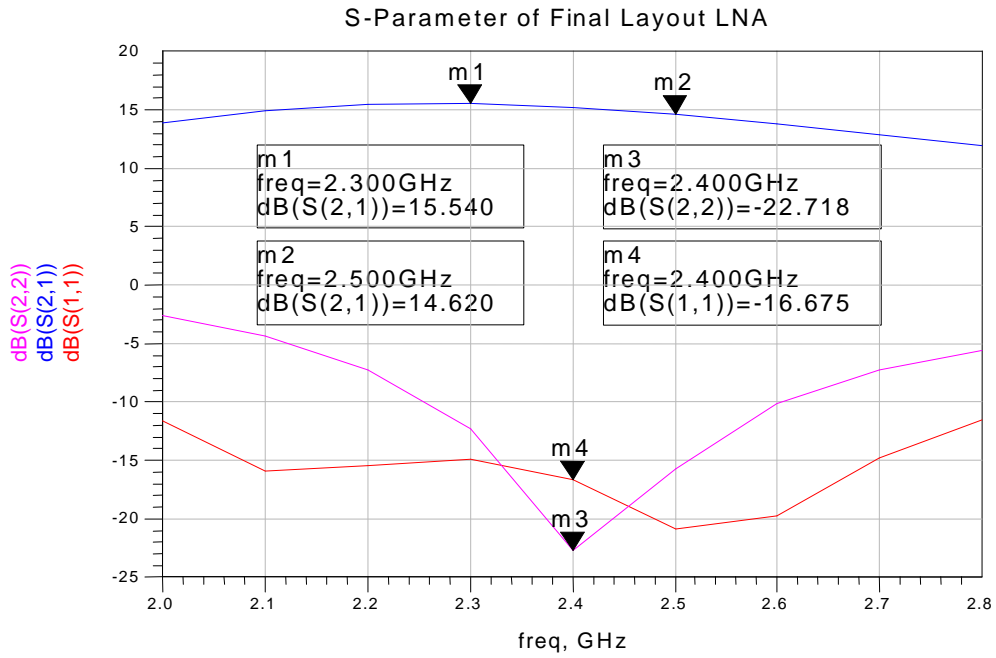


Figure 9: S-Parameter performances of final layout schematic LNA (linear simulation using 300um DFET S-Parameter file)

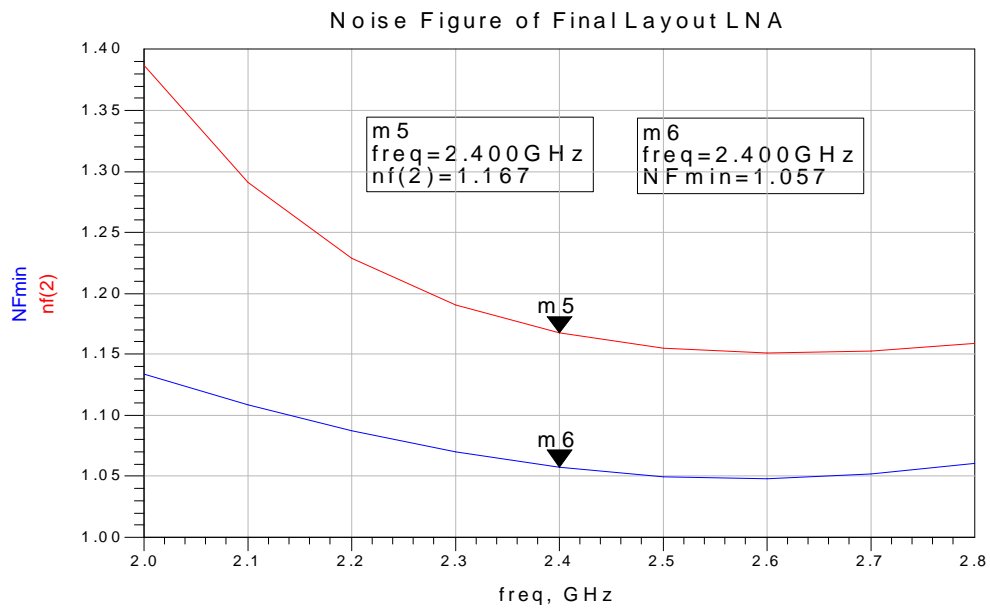


Figure 10: Noise figure performance of final layout schematic LNA (linear simulation using 300um DFET S-Parameter file)

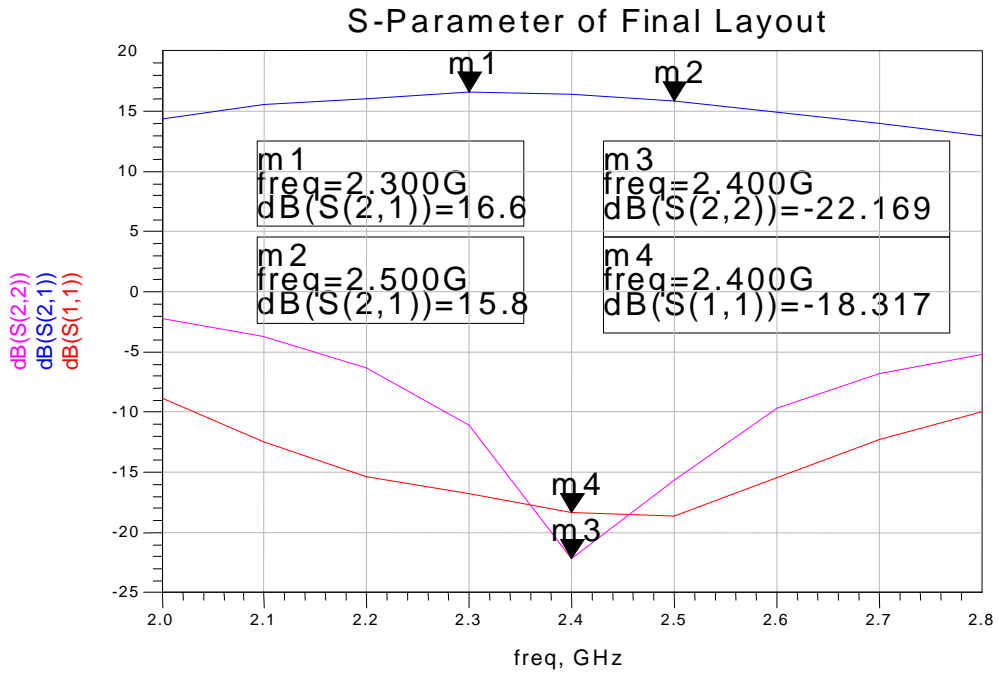


Figure 11: S-Parameter performances of final layout schematic LNA (linear simulation using 600um DFET non-linear TOM3 model)

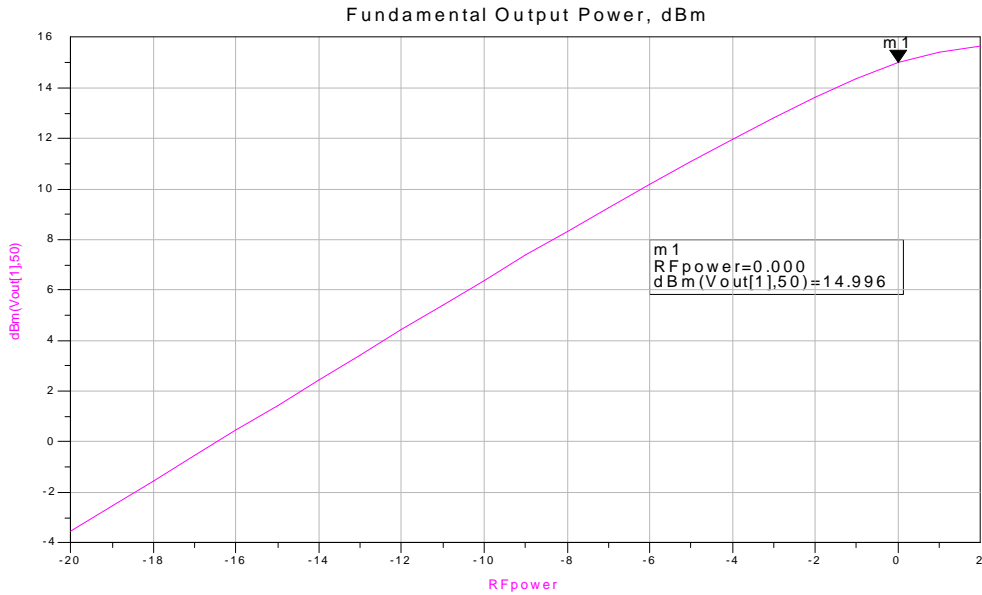


Figure 12: P1dB performance of final layout schematic LNA (harmonic balance simulation using 600um DFET non-linear TOM3 model)

4.0 Schematic diagrams and Layout

The following schematics are including in this report.

Figure 14: LNA simplified Schematic with S-Parameter file

Figure 15: LNA final layout schematic with DFET non-linear model

Figure 16: LNA final layout in ANACHIP

5.0 DC Analysis

Table 4 shows the DC bias simulation results for both stages DFET of LNA.

First stage DFET	Second stage DFET
Vds=2.38 V	Vds=2.38 V
Vgs=-0.17 V	Vgs=-0.17 V
Ids=21.7 mA	Ids=21.7 mA

Table 4: DC bias simulation results for both stages DFET of LNA

Figure 13 shows DC bias simulation results on simplified LNA schematic using 'Annotate DC simulation' function

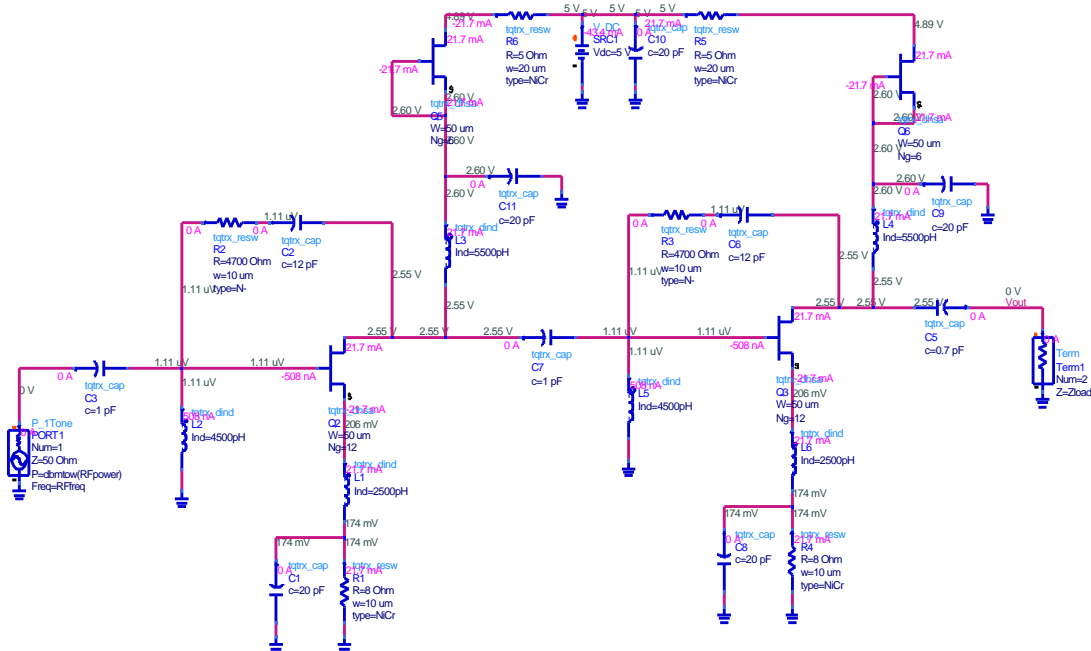


Figure 13: DC bias simulation results on simplified LNA schematic using 'Annotate DC simulation' function

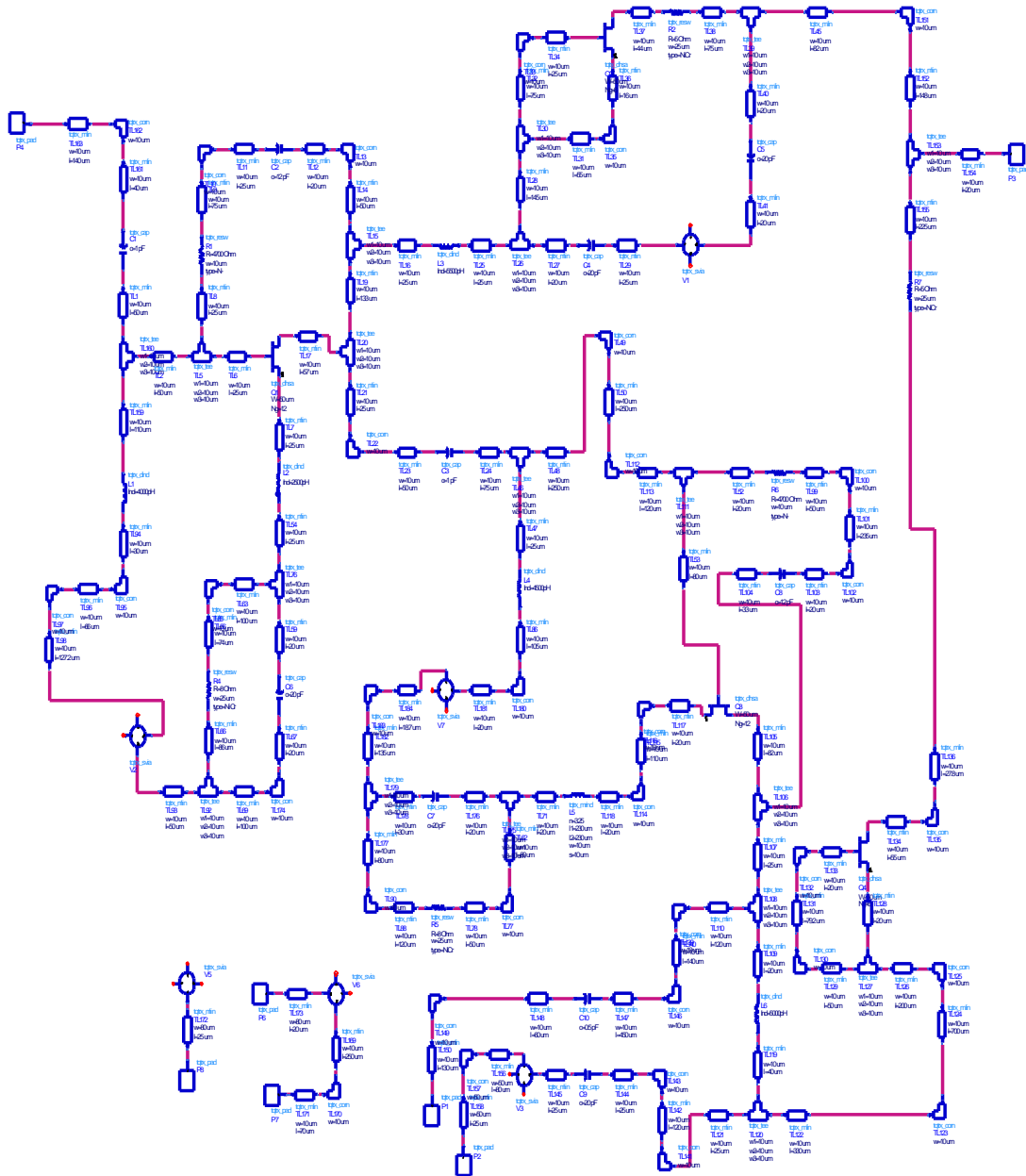


Figure 15: LNA final layout schematic with DFET non-linear model

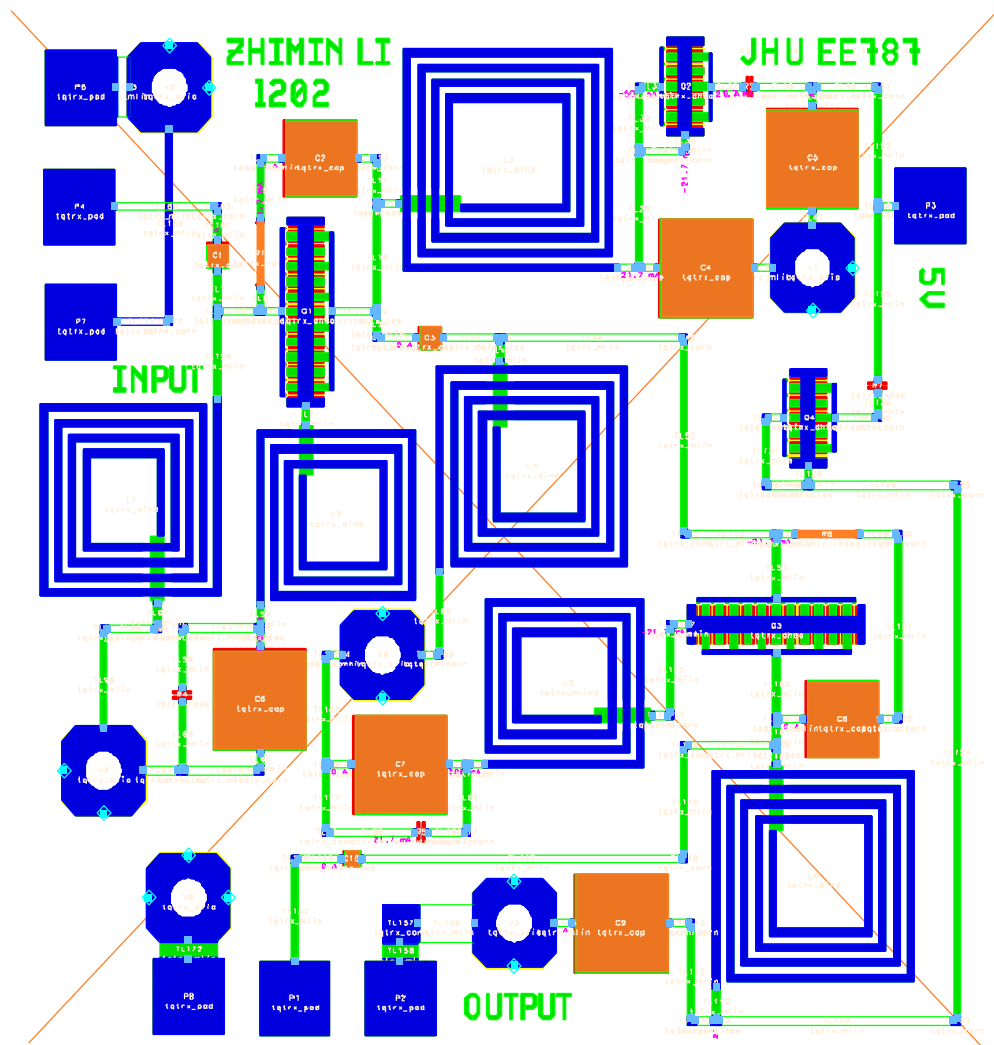


Figure 16: LNA final layout in ANACHIP

6.0 Test Plan

6.1 Test Equipment

The following test equipments or equivalent are necessary to measure the LNA performance:

- Agilent 8510 Network Analyzer
- Agilent xxxx Noise figure meter
- 5 V DC Power Supply
- Synthesized Signal generators to 26 GHz
- Power combiner
- Spectrum analyzer to 18 GHz
- Cascade Model 43 wafer probe station with up to 4 RF probes & 4 DC needle probes

6.2 Turn On Procedure

Extreme caution should be taken when turning on the +5 Volt DC power supply. Make sure the Ground wire is firmly connected on ground PAD before the +5 Volt DC power supply is connected. The required DC voltage and DC current are listed as following:

- The required voltage for the LNA is +5 V DC
- The DC current is around 42 mA

6.3 S-Parameter Measurement

- Calibrate the network analyzer from 2 to 2.8 GHz
- Position the bias probe on the 5V pad
- Position the input probes on the “INPUT” pads
- Position the output probes on the “OUTPUT” pads
- Make S11, S21, S12, S22 measurements, plot the data and store all data on disk

6.4 Noise figure Measurement

- Calibrate the noise figure meter
- Position the bias probe on the 5V pad
- Position the input probes on the “INPUT” pads
- Position the output probes on the “OUTPUT” pads
- Make noise figure measurements and record the data

6.5 Input IP3 testing

- Set $f_1=2.4$ GHz, $f_2=2.45$ GHz

- Set each tone power level of output port of power combiner to -10 dBm
- Use the spectrum analyzer to measure the delta of power level between fundamental frequency and third order frequency
- The input IP3 should equal to $-10+\Delta/2$ dBm

7.0 Conclusion and Recommendations

The LNA design and layout were very successful. It met all the goals. The gain is great than 15 dB over the desired frequency, noise figure is less than 1.3dB much less the spec of 3 dB, and input IP3 is great than +5 dBm. The layout of LNA is so nice and well organized. There is no recommendation.

8.0 Project file

The project file has been submitted on 3.5 inch HD diskette

9.0 GDSII (CALMA) Layout file

The GDSII layout file has been submitted to instructors