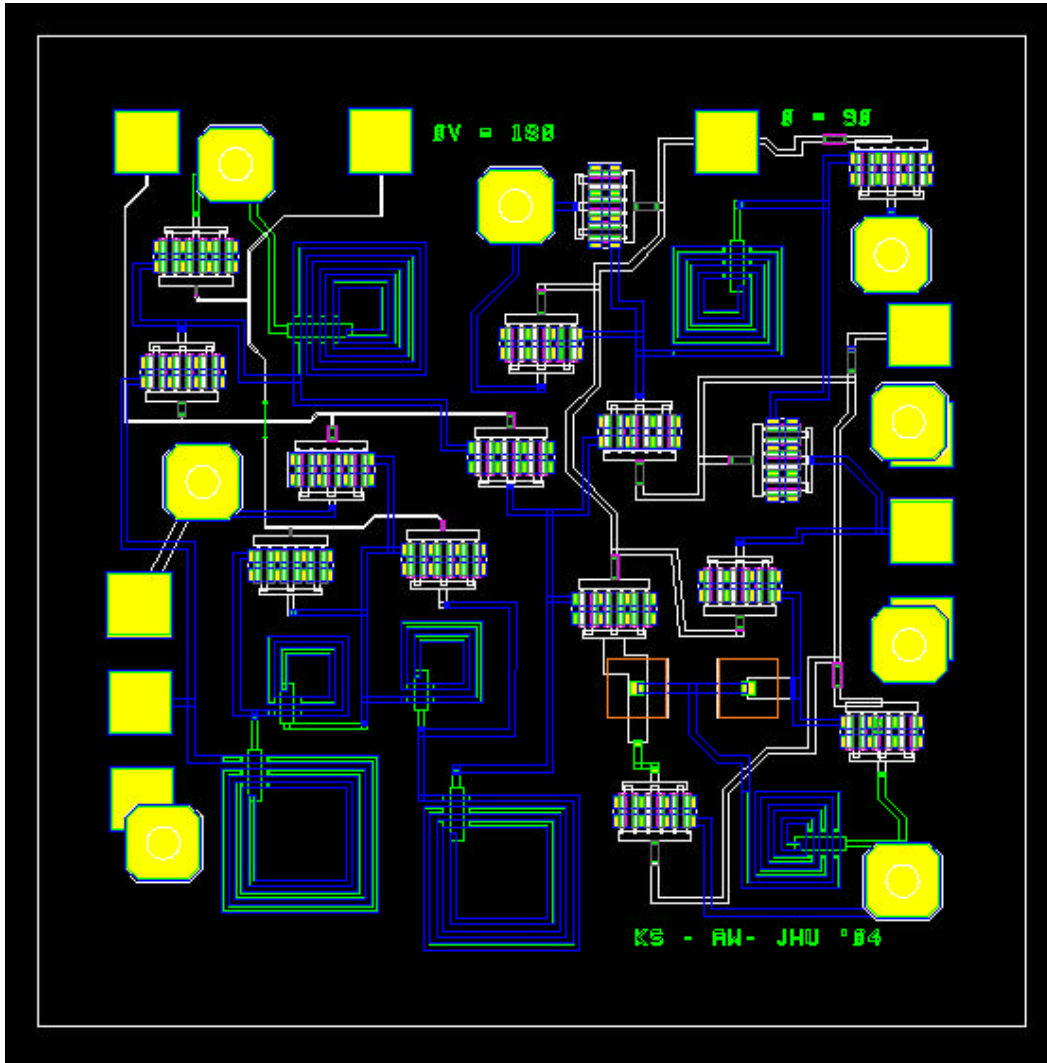


C-BAND 2-Bit Phase Shifter
JHU EE787
Fall 2004



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ABSTRACT

This report documents the design of a phase shifter for use as part of a C-band transceiver. The phase shifter is designed to work over the 5.2 to 5.9 GHz frequency band.

The phase shifter was designed using Agilent's Advanced design System (ADS) using the Triquint provided library. The layout was completed on a 60 x 60 mil AnaChip using ADS. The chip will be manufactured using the Triquint Trx process.

INTRODUCTION

Circuit Description

The circuit topology selected for the design was two high pass / low pass switched networks in series to create phase shifts of 90 and 180 degrees. The circuit was designed to use control voltages of 0 V and -5 V. Each bit requires two complimentary voltages to switch between the reference and phase shifted states.

Design Philosophy

The phase shifter design was required to have two phase bits of 90 and 180 degrees, with a loss of less than 8 dB. We chose topology from a documented switched phase Ku design. This design uses the internal characteristics of switched fets, resistive in the on state and capacitive in the off state, to create the high pass / low pass networks. The architecture has only one fet in the through path of the phase bit and should reduce the loss over a design with a switch before and after the high pass and low pass networks.

We began the design with the Ku band basic architecture and then scaled the RF components to C band. This provided a design that was close to desired. The ADS optimizer was then used to tweak the values to provide optimal results.

The next step was to add Triquint elements for simulation and layout. The ideal inductors and capacitors were replaced with Triquint MRIND and MIM capacitors and re-simulated. The result was then tweaked for performance using the Triquint elements. Layout was then completed using ADS and Triquint provided library elements.

Tradeoffs

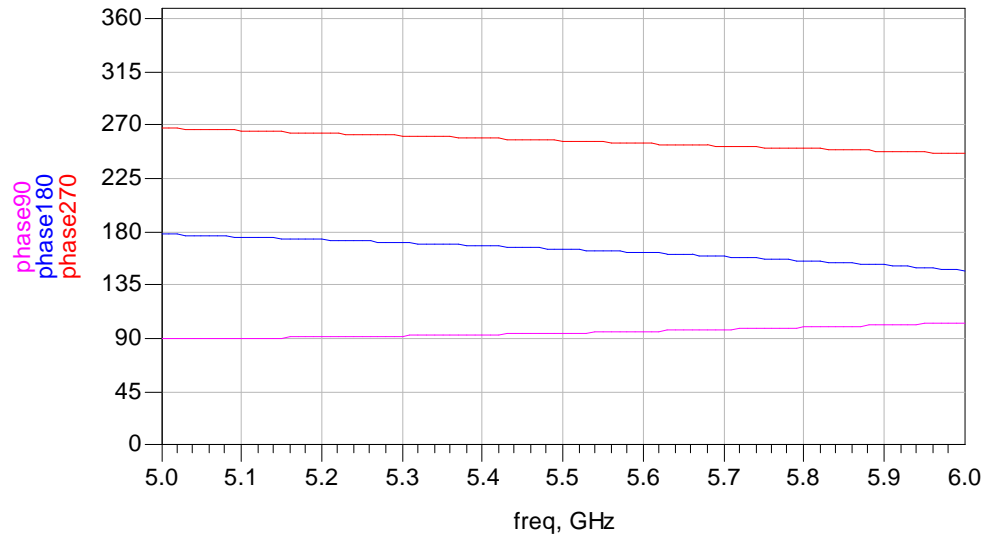
As in any design we had to make performance tradeoffs. We had to make a decision between phase error and loss. By allowing our phase to deviate from its ideal value we were able to achieve a better match over all states and less overall insertion loss.

Specifications and Compliance

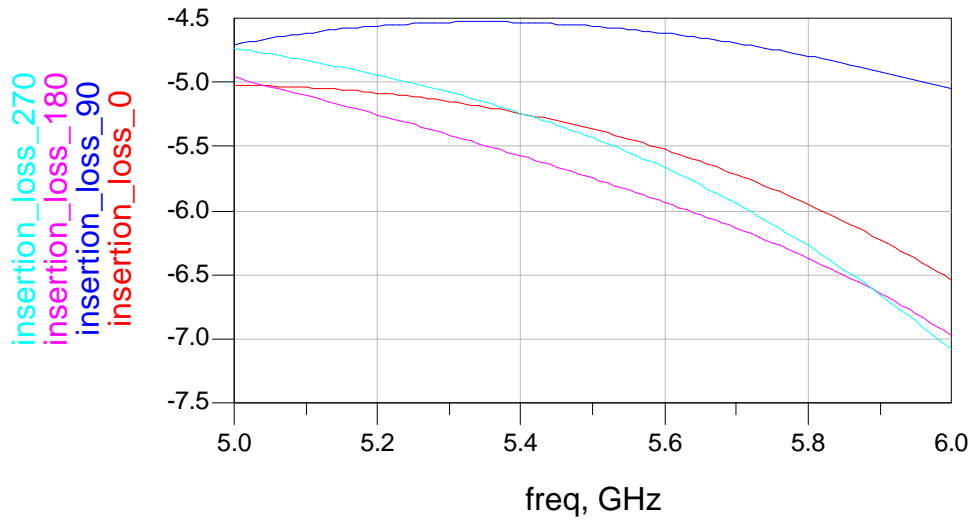
	Specification	Compliance
Frequency	5150 – 5875 MHz	Yes
Bandwidth	> 800MHz	Yes
Insertion Loss	< 4dB (3dB goal)	No
Insertion Balance	+/- 1dB min IL	No
Phase Shift	Steps: 45,90,180	Yes
VSWR, 50 ohms	< 1.5:1 input & output	No
Supply Voltage	+/- 5V	Yes
Control	TTL(goal); or 0,-5V switch inputs	Yes
Size	60 x 60 mil ANACHIP	Yes

Simulated Results

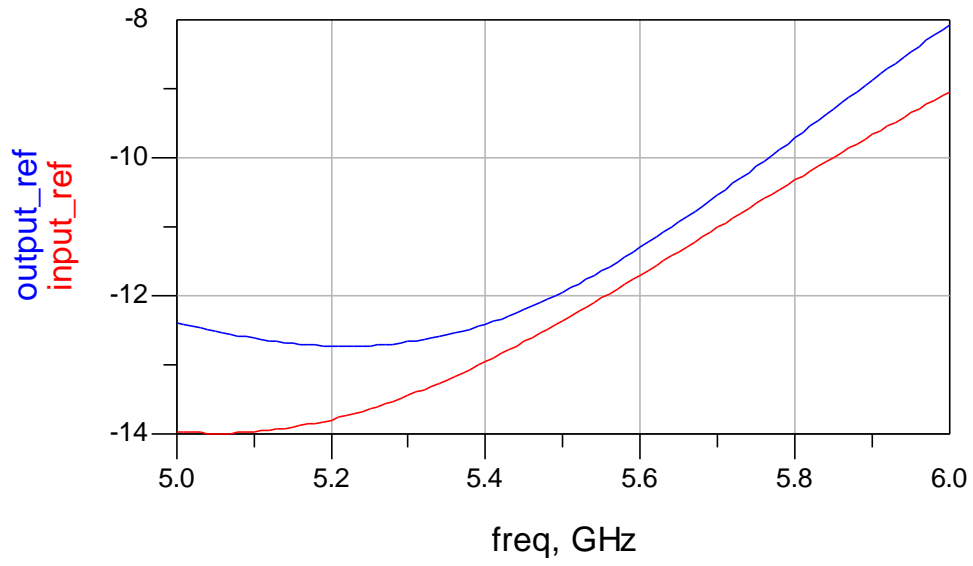
Phase of the different states references to the reference (zero phase shift) state



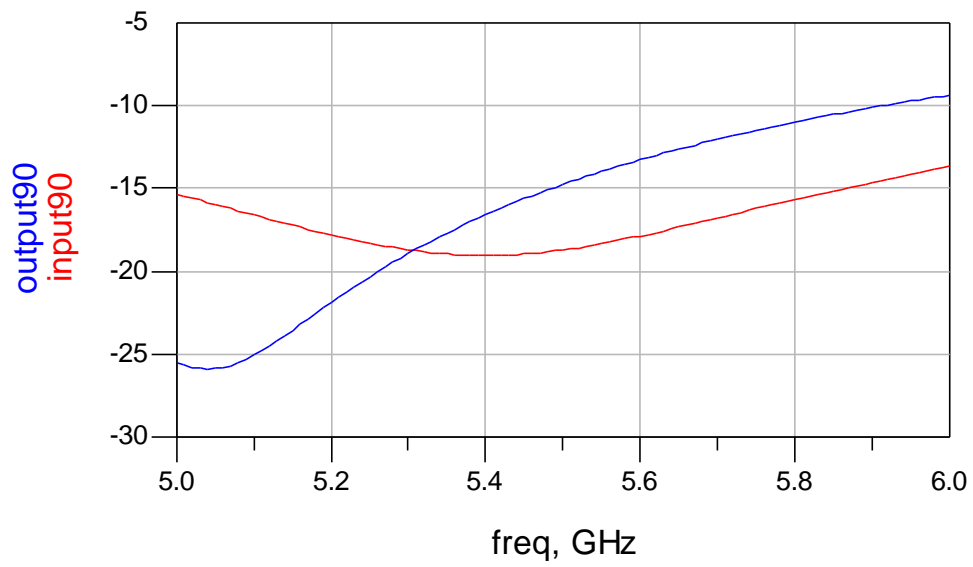
Insertion loss of the four phase states



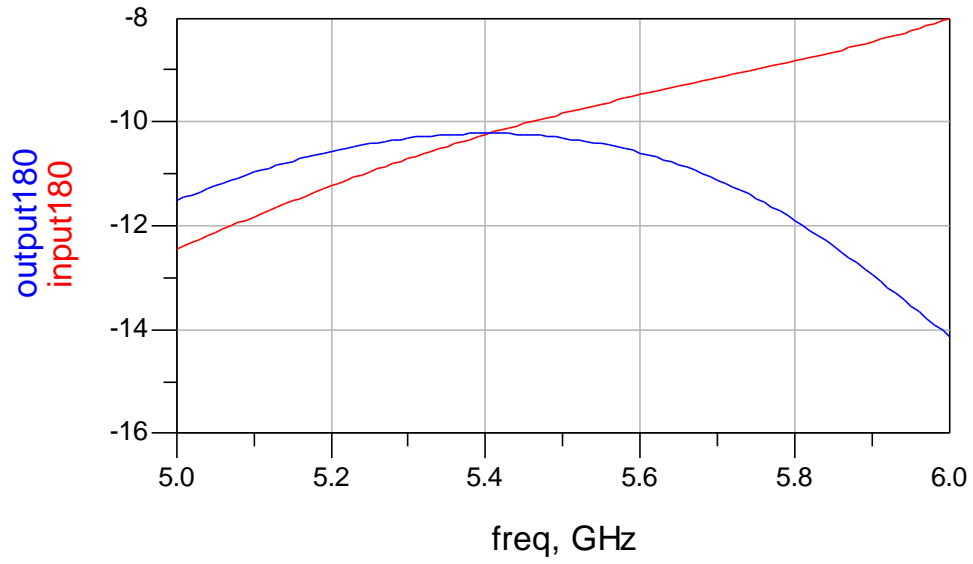
Return Loss for the zero phase state



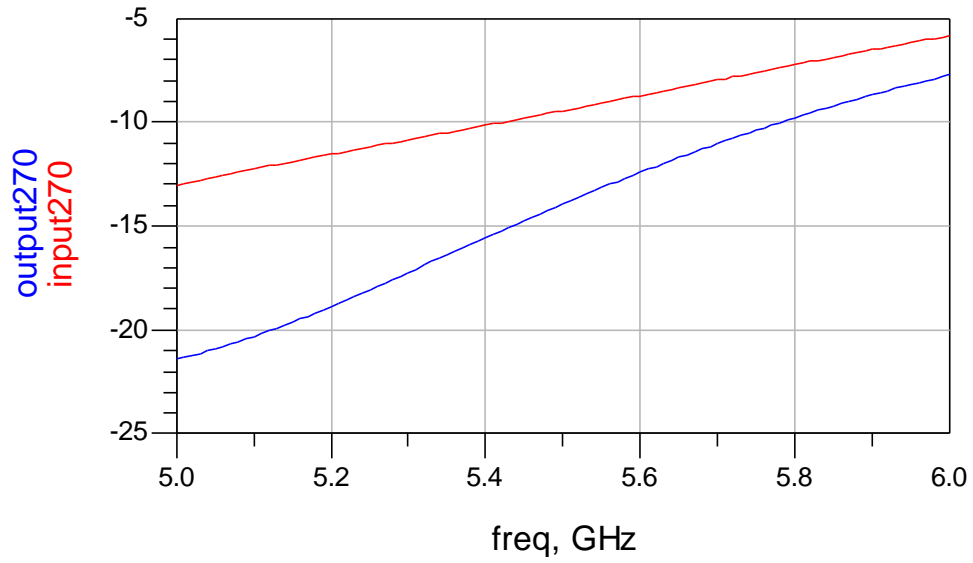
Return Loss of the 90° state



Return Loss of the 180° state

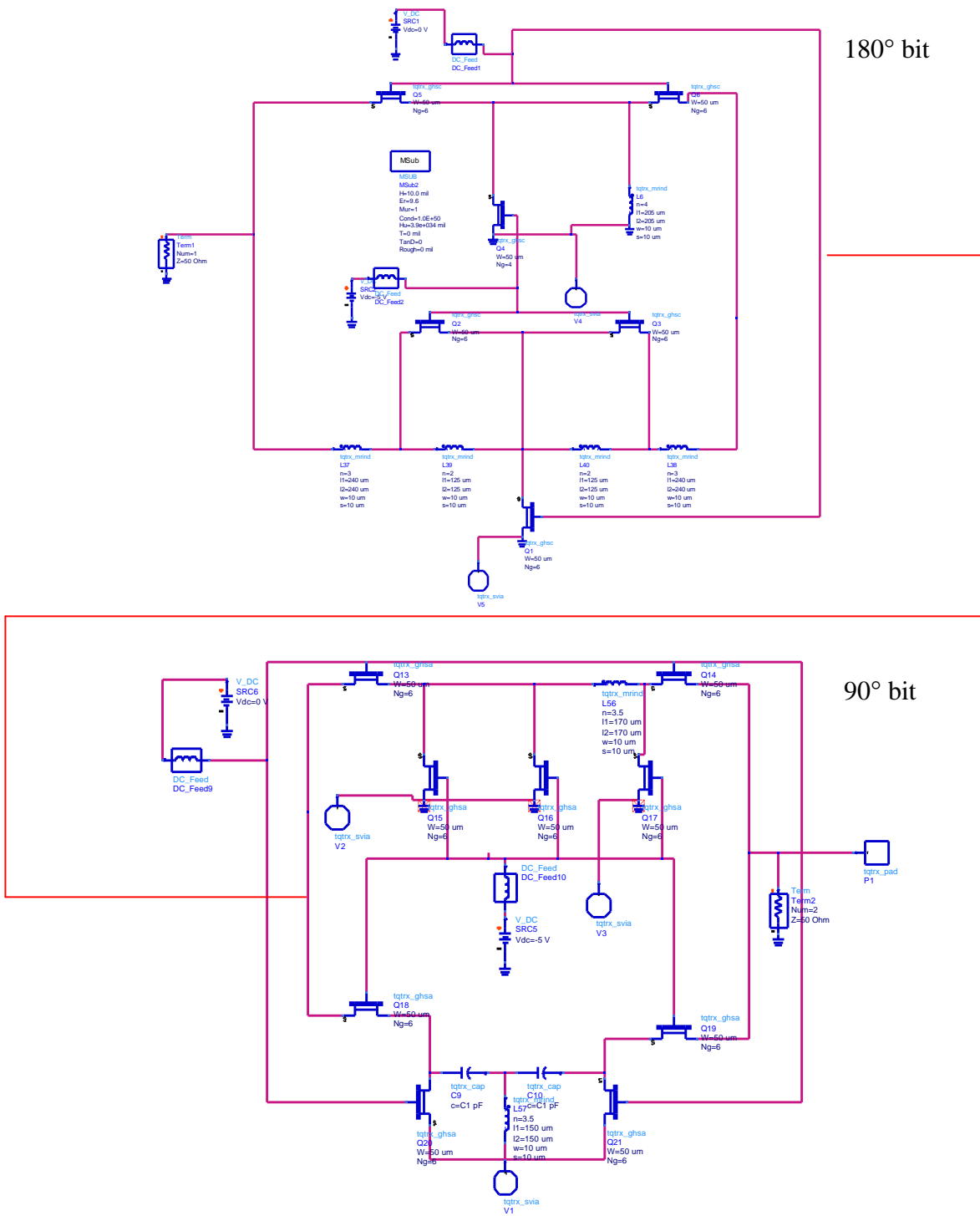


Return Loss of the 270° state



Schematic

This is the completed schematic using TriQuint parts.

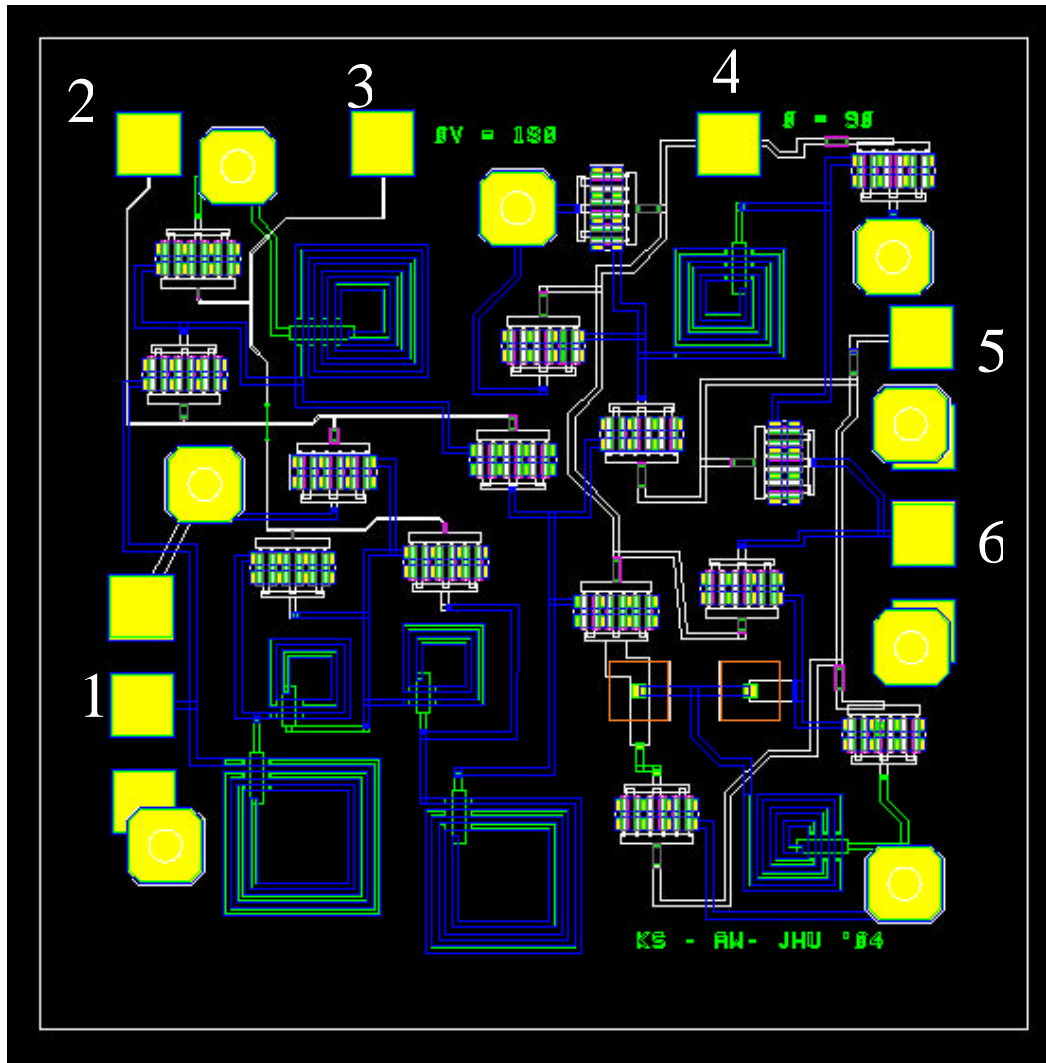


The DC voltages were toggles between 0V and -5V to change phase states.

Layout

The layout is designed to be fabricated on the TriQuint Oregon process. The RF is routed on metal layer two to reduce loss. The inductors are on metal layer 1 and 2 to reduce loss even further. The gate lines are the only signals routed on metal layer 0 since there is no current on these lines. These lines are also narrower than the other since the gate draws no current. G-implant resistors are used because of their high resistance per square allowed the resistors to be small. This type of resistor can not handle much current, but it is acceptable to use them on gate lines where there will be no current.

Pin Number	Pin Name
1	RF In
2	180 -
3	180 +
4	90 +
5	90-
6	RF Out



Test Plan

The phase shifter is designed to be tested using a probe station. For the RF connections (Pins 1 and 6), gnd-signal-gnd probes should be connected to a network analyzer to measure return loss, insertion loss, and phase. This type of probe is used to provide the most accurate measurements. A DC voltage (0V/-5V) must be applied to the other 4 pins using the chart below to dictate what phase state the phase shifter is in. Pins 2 and 5 are compliments and pins 4 and 5 are compliments. The design does not include any DC blocking capacitors on the MMIC, so external ones must be used if they are required.

Phase state	Pin 2	Pin 3	Pin 4	Pin 5
0°	0V	-5V	-5V	0V
90°	0V	-5V	0V	-5V
180°	-5V	0V	-5V	0V
270°	-5V	0V	0V	-5V

Conclusions

The phase shifter MMIC designed should meet the needs of the transceiver system that it is intended to be used in. When designing a phase shifter, a lot of trade-offs must be looked. We found that improving one of the parameters, such as phase accuracy, often meant sacrificing one of the other parameters, such as loss. In general we found it import to use the least amount of series components as possible- in the RF path to help keep the insertion loss to a minimal.

The design was only simulated using the schematic part of ADS. If time allowed, it would be recommended to simulate some of the RF structures in a EM simulator to enough there is no unwanted coupling or interaction between parts.

Once the design has been fabricated, comparing the measured data to the predicted performance will allow the design to be verified. If more space were available, it would be advantage to provide a break out for each of the bits so they could be characterized separately and this would provide more opportunity for troubleshooting.