

MMIC Design Project  
S Band Post Amplifier  
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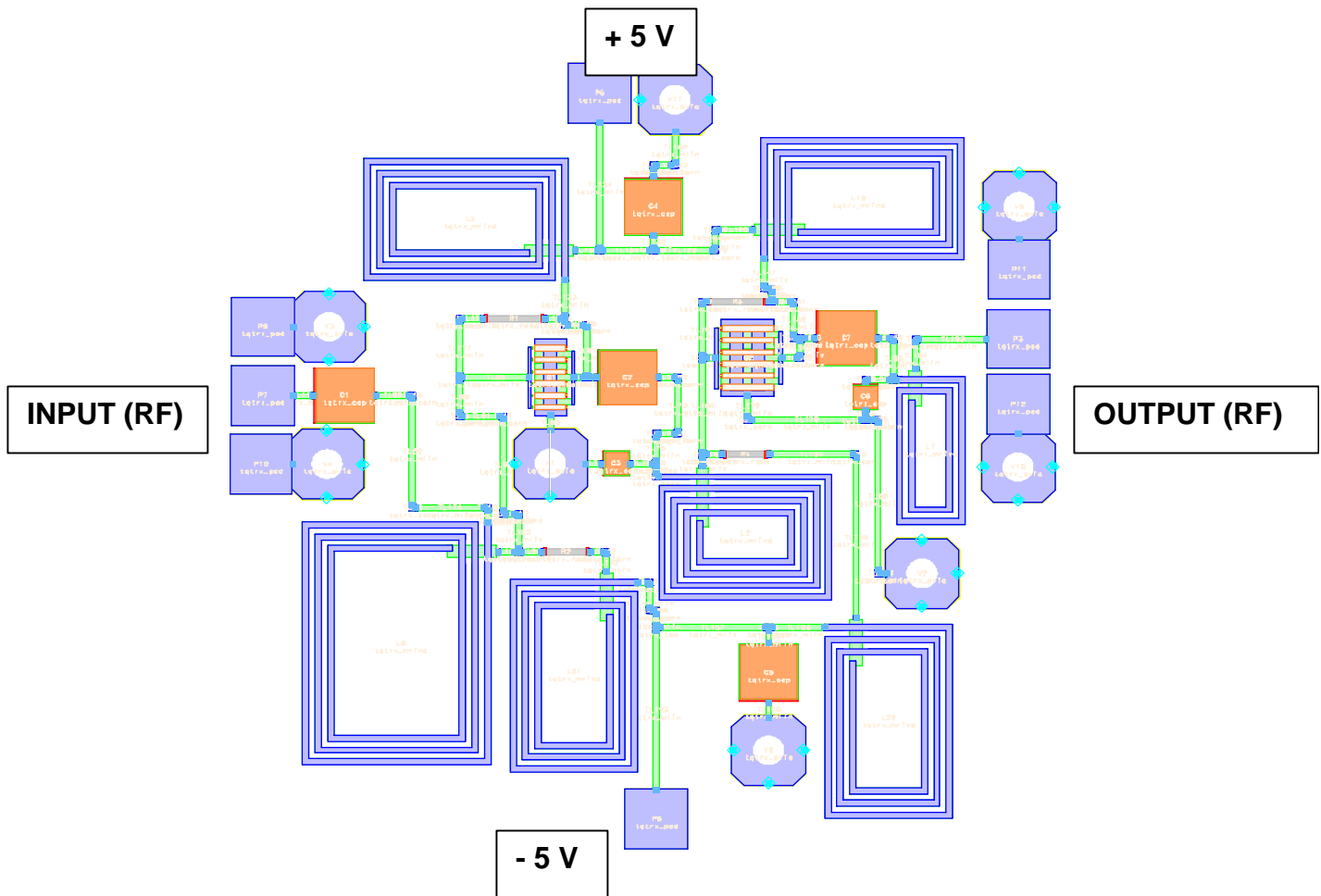
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## Abstract

This report documents the design of a post amplifier for primary use at 2.4GHz and using the Triquint TRx process. The design was produced as part of the MMIC Design Course taught at Johns Hopkins University during the Fall 2002 semester.

The post amplifier was designed for use in an S-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies.

The design software used to design the post amplifier was Agilent's Advanced Design System 2002C (ADS). The elements used were custom model elements based on Triquint process. The design was laid out on a 60 x 60 mil Anachip.



## **Introduction**

### **Circuit Description**

The circuit topology selected for the design was a cascaded two-stage amplifier layout, which requires two power supplies (of opposite polarity). The matching networks were designed using lumped element topology.

### **Design Philosophy**

The design specifications of the post amplifier called for an emphasis to be placed on gain and IP3. In the early stages of this design, a series of ideal case design using both the GFET and DFET transistor models sized at 300 and 500 um. It was determined that the 500 um GFET was the optimal choice device for this sort of application. Due to the gain requirement of 12 dB or more, we decided to use 300 um for the first stage and a 500 um for the second stage.

The first step in designing the post amplifier was to determine where the device should be biased. This stage was made fairly simple by utilizing ADS's Amplifier=> DC and Bias Point Simulations => and FET IV Curves template. For maximum gain, we already had in mind that we wanted to bias the device at IDSS 1/2. By correctly using the template, we determined that we wanted to bias the first stage at:

$$I_{ds} = I_{dss}/2 = 83\text{mA}/2 = 41.5\text{mA} @ 5 \text{ V} = V_{ds}, 900 \text{ mV} = V_{gs}$$

And the second stage at:

$$I_{ds} = I_{dss}/2 = 138\text{mA}/2 = 69\text{mA} @ 5 \text{ V} = V_{ds}, 900 \text{ mV} = V_{gs}$$

The next step in the design was to determine the input and output matching circuitry for the first and second stages separately. With the Cripps method in mind, this was process was accomplished through the use of ADS's Amplifier=>S-parameter Simulations=> S-parameters, noise figure...etc template. Ideal elements were used for the first iteration of designs for each stage.

Upon completing the matching networks for each stage, both stages were optimized for optimal gain, output power, and return loss. The results were analyzed using both linear and nonlinear simulated data. The two separate stages were than combined and the overall performance of the amplifier is optimized. After satisfactory performance is obtained using the ideal elements in the combined two-stage design, the ideal elements are replaced by Triquint elements. Special attention was given to the Triquint inductors as have been shown to be lossier than ideal inductors.

The final stage of the design process was to shift the design from schematic in layout. The circuit was tweaked and placed element by element into the given 60 x 60 mil anachip frame. Microstrip lines, tees, and vias were substituted for there ideal counterparts.

## **Trade-offs**

Two trade-offs considered in the design stemmed from the fact that the design was implemented using a dual-supply bias network. One trade-off considered in the design was that the correct sequencing of turning on/off power supplies was critical to avoid device burnout. Another trade-off encountered in the design was that of space, since by utilizing two power supplies, we also had to add extra bias inductors.

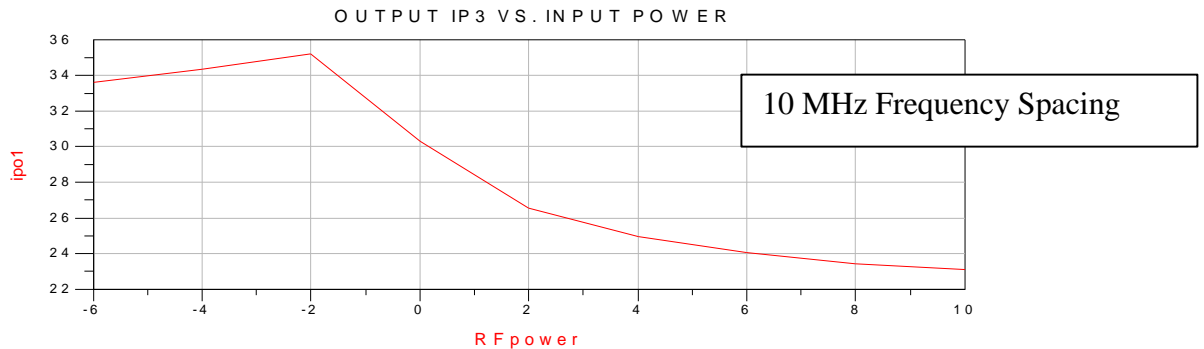
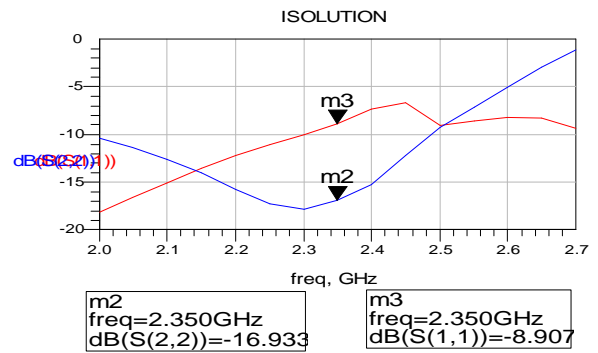
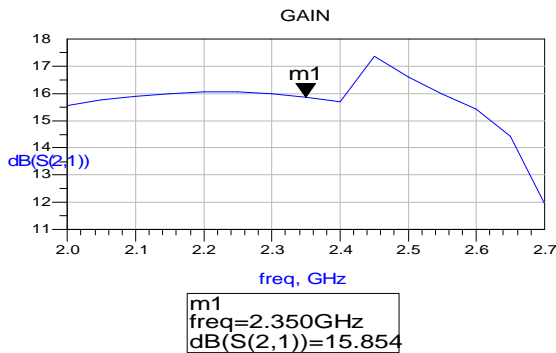
# Modeled Performance

## Specification Compliance Matrix

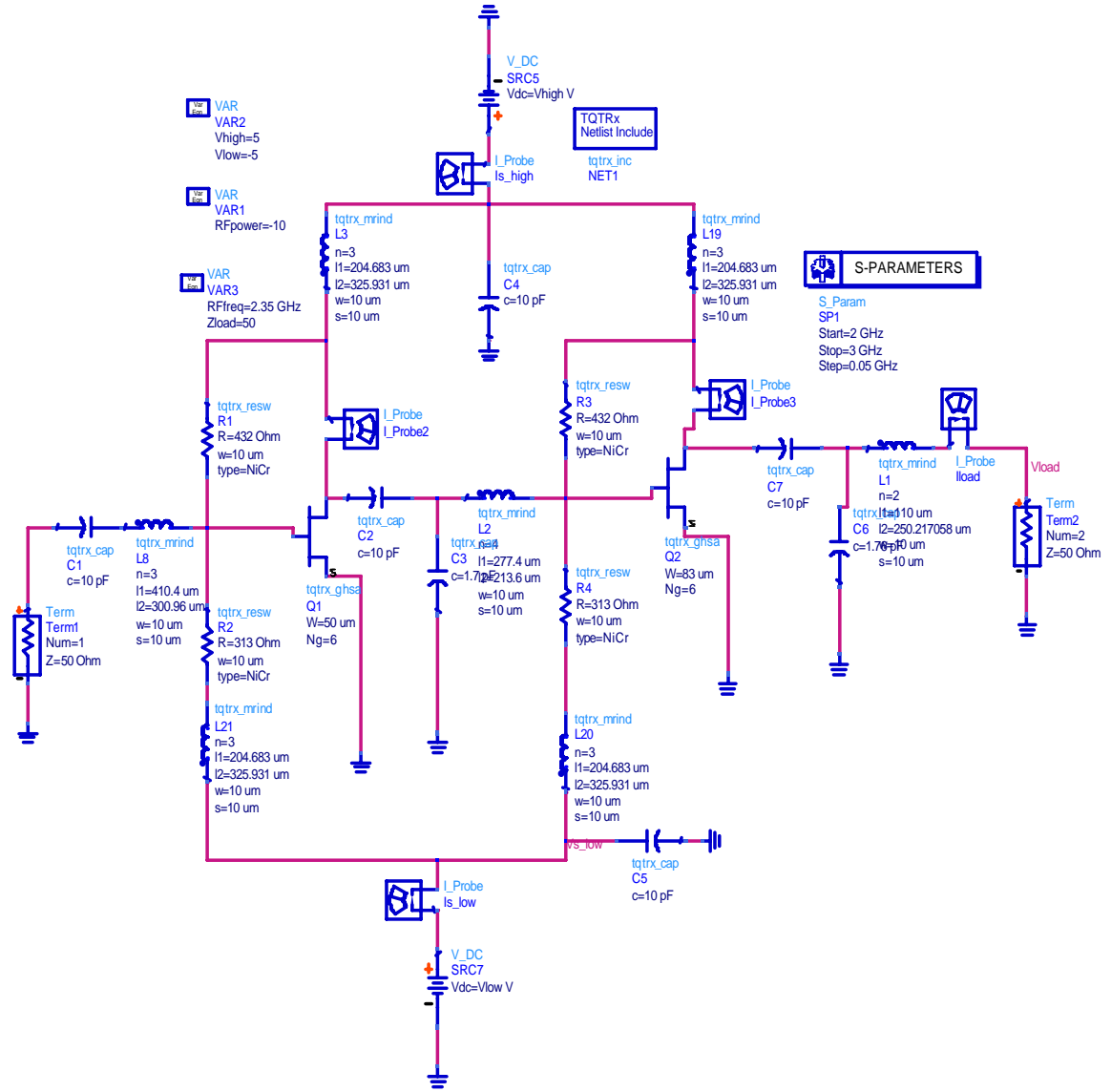
	Specification Goal	Triquint Elements Pre Layout	Final Layout Schematic
Frequency	2300 to 2500 MHz	2300 to 2500 MHz	2300 to 2500 MHz
Bandwidth	>200 MHz	> 700 MHz	> 700 MHz
Gain	>12 dB 15dB, Goal	> 15dB	> 15dB
Output IP3	> +20 dBm	> +22 dBm	> +22 dBm
VSWR, 50 Ohm	<1.5:1 input & output	1.51:input 1.8:1 output	2.1:1:input 1.3:1 output
Supply Voltage	+/- 5 Volts; +5 Volts Goal	+/- 5 Volts	+/- 5 Volts

## Predicted Performance

### SMALL SIGNAL CHARACTERISTICS LAYOUT TRIQUINT ELEMENTS



# Schematic Diagrams





## **Test Plan**

The following items and test procedures are recommended to test the S-band post amplifier

### **Linear Parameters**

Equipment: Vector network analyzer (Agilent 8510)  
Probe Station  
Bias Supplies

Procedure:

- Calibrate the network analyzer from 0.45 to 10 GHz
- Place the bias probe on the pad of the chip labeled “5V” and “NEG5V”.
- Place probe tips on the designated pads. The input port is labeled “IN” and the output port is labeled “OUT”.
- Turn on the two power supplies.
- Record data.

### **Power measurements**

Equipment: Signal Generator  
Spectrum Analyzer

Procedure:

- Connect the signal generator probe to the input pad of the amplifier chip, which is the port marked “IN”.
- Connect the spectrum analyzer probe to the output pad of the amplifier chip which is the port marked “OUT”.
- Place the bias probe on the pad of the chip labeled “5V” and “NEG5V”.
- Power supplies.
- For Pin vs. Pout set the generator to the frequency of interest and sweep the power up to, but not exceeding, 10 dBm.
- Record measurements from spectrum analyzer after each interval.

## **Conclusion & Recommendations**

In conclusion, we noted that we could have optimized one stage for VSWR and weighted this goal a little more than the others possibly. However, it would have involved a trade-off in gain (or noise figure). Finally, a more thorough Monte Carlo analysis could have been done in order to make the design more robust and less dependent on device variation.