The Design of an S-band Single Balanced Mixer for Starved Diode Operation

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1. Abstract

This paper presents the design strategy, simulation results, and final layout of a MMIC S-band single balanced mixer optimized for starved diode operation. The design fits on a 60 mils square die and is to be fabricated using the Triquint Semiconductor TRx process for GaAs. Agilent's Advanced Design System (ADS) in conjunction with Triquint's proprietary library was the software tool used for simulation and layout.

The RF band of the mixer is 2300-2500MHz; the LO band is 2140-2340MHz; and the IF center frequency is 160MHz. The mixer can be used for both upconversion and downconversion. With a 5V DC bias applied to the diodes and with a 0dBm LO power level, the mixer achieved the following performance:

- Conversion Loss < 10dB
- LO VSWR <= 1.6 : 1
- RF VSWR <=2.2 : 1
- IF VSWR < 2.1 : 1
- LO/RF Isolation > 27dB
- IF/RF Isolation > 19dB
- LO/IF Isolation > 39dB

All prescribed minimum performance specifications were met, and many of the design goals were also achieved.

2. Introduction

In selecting the mixer topology the first decision was between double balanced and single balanced approaches. The former affords excellent isolation and good VSWR over a wide bandwidth, but at the expense of greater conversion loss, higher LO drive level, and a more complicated layout due to the ring diode structure. Furthermore, the ring diode structure complicates DC biasing of the diodes.

A single balanced mixer, on the other hand, provides moderate isolation, good VSWR over a narrow bandwidth, and low conversion loss—all in a simple structure that lends itself well to DC biasing.

Given the emphasis on conversion loss and starved diode operation in this design, coupled with moderate VSWR and isolation requirements, a single balanced approach was the more judicious choice. A single balanced mixer is typically implemented in one of two ways: with a 90^0 or 180^0 hybrid (see Figures 1 and 2)[1]. While the conversion loss of the two varieties are similar, the LO/RF isolation of the 180^0 hybrid is determined mainly by the inherent isolation of the coupler, but the VSWR of the LO and RF ports is mainly set by the VSWR looking into the diode circuitry. The LO/RF isolation of a mixer using a quadrature hybrid, however, is mainly a function of the return loss of the coupler, while the VSWR is dictated by the quality of the terminations at the RF/LO frequencies. An important limitation of the 90^0 hybrid approach is that it cannot function simultaneously as an upconverter and downconverter. Since this dual capability was an important goal of this design, the 180^0 hybrid approach was favored. The inductors provide a DC path to ground as well as an IF return, while the capacitor provides an RF path to ground to allow the diodes to be pumped. To supply DC bias current, the inductors in the actual design are replaced with resistors.

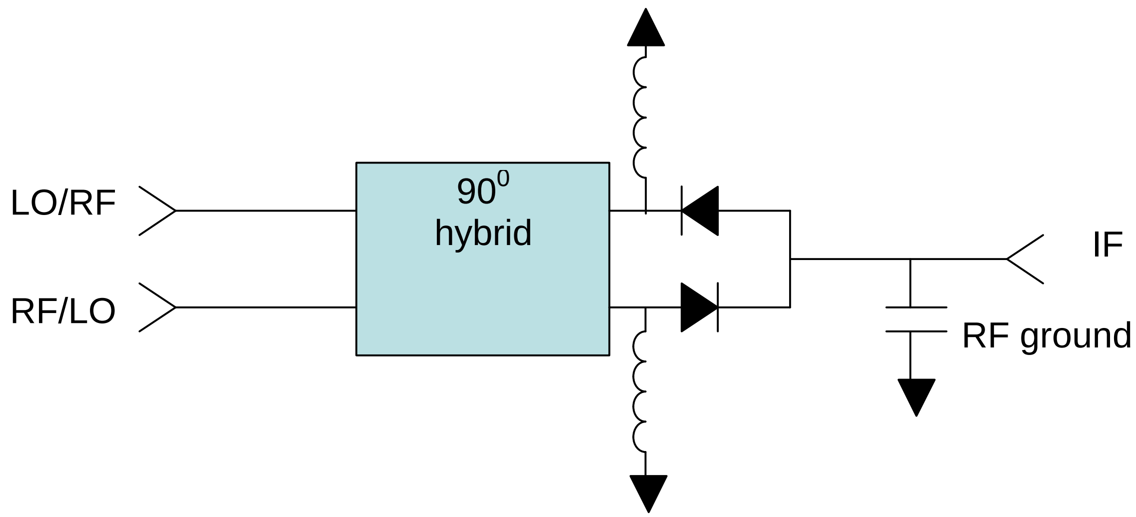

Figure 1: Single Balanced Mixer Using 90^0 Hybrid

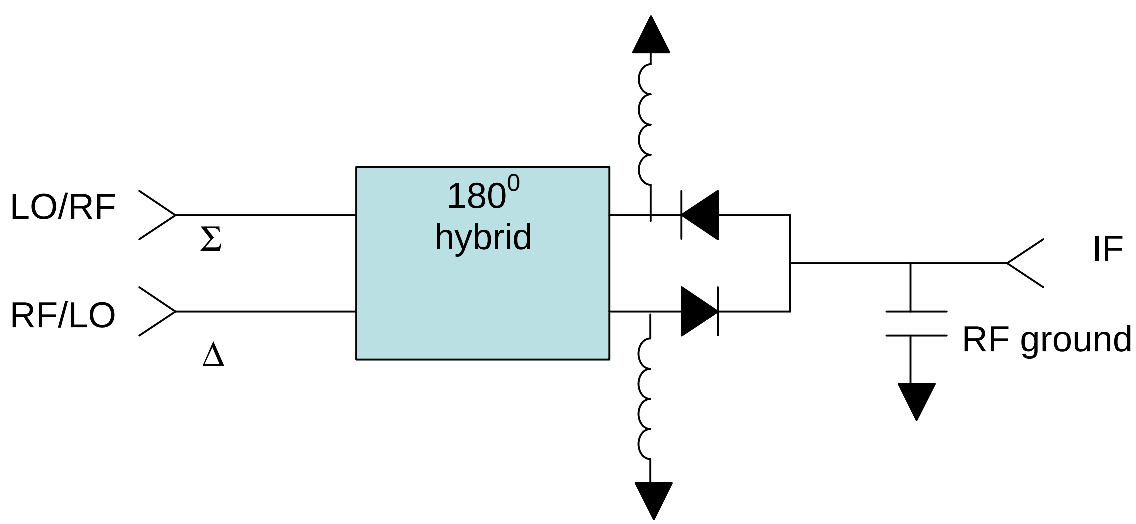

Figure 2: Single Balanced Mixer Using 180^0 Hybrid

3. Specifications and Modeled Performance

Table 1 contains the combined specifications for the S-band downconverter and upconverter alongside the modeled performance of the circuit extracted from the final layout. All specifications were met in addition to several of the design goals. The boldfaced results indicate that the design goals were achieved. Figures 3-8 display simulation data for upconversion and downconversion operation at the center frequency and the band edges. Table 1 includes worst-case results.

	Specs	**Goal**	**Modeled Results**
RF Frequency (MHz)	2300 - 2500	N/A	2300 - 2500
LO Frequency (MHz)	2140 - 2340	N/A	2140 - 2340
IF Frequency (MHz)	160	N/A	160
Isolation: LO/RF port (dB)	> 10	>=7	**27**
Isolation: IF/RF (dB)	N/A	N/A	**19**
Isolation: LO/IF (dB)	N/A	N/A	**39**
Conversion Loss (dB)	<= 10	<=7	10
LO power (dBm)	<= 7	0	**0**
VSWR (50 W): LO	<=2.5:1	<=1.5:1	1.6: 1
VSWR (50 W): RF	<=2.5:1	<=1.5:1	2.2: 1
VSWR (50 W): IF	<=2.5:1	<=1.5:1	2.1: 1
DC Bias Voltage (V)	0 -5	N/A	**5**
Die Size (mil x mil)	60 x 60	60 x 60	**60 x 60**

Table 1: Specifications and Modeled Results

4. Schematic, Design Notes, and Layout

Figure 9 depicts a stripped down version of the final design without transmission line elements. A lumped element realization of a ratrace hybrid designed at the center frequency of the combined RF-LO band (2140 – 2500MHz) performs the function of the balun, with the LO and RF attached to one pair of mutually isolated ports and the two diodes connected to the other pair.[2] The 10dB return loss bandwidth of the hybrid is roughly equivalent to the LO/RF band of the mixer. A pair of 30pF DC blocking capacitors (C26 and C27) and one 100pF capacitor allows DC current to flow through the diodes. The current through the diodes is set by the sum of two 1500Ω resistors and the composite DC resistance of the diodes. The optimum DC voltage is 5V. The diodes are overlap diodes rather than FETs with drain and source terminals shorted. A diode width of 80μm resulted in the optimal combination of RF/LO and IF VSWR as well as conversion loss.

Two 0.75pF capacitors to ground (C33 and C35) act as simple matching stubs to improve the VSWR at the LO and RF ports. The IF matching network consists of a single series 14nH inductor (L15). In fact, the optimal value would be close to 50nH, but the size of such a component would be prohibitively large. A 500pH inductor (L14) resonates with the bypass capacitor (C29) to provide an RF ground but also to present a high impedance at IF. A 100pF DC blocking capacitor (C30) is placed at the IF port. As large as this value is for a MMIC design, it still represents a compromise since it still appears as a significant impedance at IF. In keeping with the objective of requiring no off-chip components for this design, the largest DC blocking capacitor that could fit was selected.

To measure the large signal VSWR at each mixer port, dual directional couplers were placed at each port. Γ was found by calculating the ratio of incident to reflected voltage at the coupled ports of the couplers, and VSWR in turn was determined by the relation:

$$VSWR = (|\Gamma| + 1)/(|\Gamma| - 1)$$

The final layout submitted for fabrication appears in Figure 10. Each of the four ports is labeled appropriately. Each signal port is flanked on both sides by ground pads to accommodate test probes. The ratrace coupler occupies the upper half of the chip, with the bottom right consisting of the IF matching network and DC block. Care was taken to keep as much space between inductors as possible to minimize mutual coupling.

5. DC Analysis

Figure 11 presents a simplified DC schematic with DC annotations at each node. It is apparent that the DC bias is isolated from the ratrace coupler by the blocking capacitors. With the voltage supply set to 5V, the current flowing through the 80µm diodes is 1.29mA, safely below the maximum 10mA rating of the two 10µm bias resistors. This implies a DC diode resistance of roughly 440Ω. This indicates that the diodes are not fully turned on.

6. Test Plan

Figures 12-13 show the test setup for the mixer for upconverter and downconverter operation, respectively. Note that a spectrum analyzer and dual directional coupler need not be present at each port simultaneously. However, whenever a directional coupler is present at a port, each coupled port must be terminated in 50Ω.

For upconverter operation, the test plan is as follows:

1. Calibrate: determine insertion loss of directional coupler(s) and cables.
2. Set LO signal generator to midband frequency (2240MHz) and power level such that 0dBm is present at the LO port.
3. Set IF signal generator to 160MHz and power level such that –10dBm is present at the IF port.
4. Measure LO+IF, IF, and LO at RF port with spectrum analyzer. Add cable and coupler losses to calculate conversion loss, LO/RF isolation, IF/RF isolation. Vary bias voltage to obtain optimal values.
5. Calculate VSWR at LO and IF ports: Measure incident and reflected power at respective coupler ports; convert to voltage; and compute gamma and VSWR.
6. Repeat steps 2-5 at lowest LO frequency 2140MHz.
7. Repeat steps 2-5 at highest LO frequency 2340MHz.

(Optional) For downconverter operation, the test plan is as follows:

8. Set LO signal generator to midband frequency (2240MHz) and power level such that 0dBm is present at the LO port.
9. Set RF signal generator to 2400MHz and power level such that –10dBm is present at the RF port.
10. Measure IF, LO, and RF at IF port with spectrum analyzer. Add cable and coupler losses to calculate conversion loss, LO/IF isolation, IF/RF isolation. Vary bias voltage to obtain optimal values.
11. Calculate VSWR at LO and RF ports: Measure incident and reflected power at respective coupler ports; convert to voltage; and compute gamma and VSWR.
12. Repeat steps 2-5 at lowest LO (2140MHz) and RF 2300MHz frequencies.
13. Repeat steps 2-5 at highest LO (2340MHz) and RF 2500MHz frequencies.

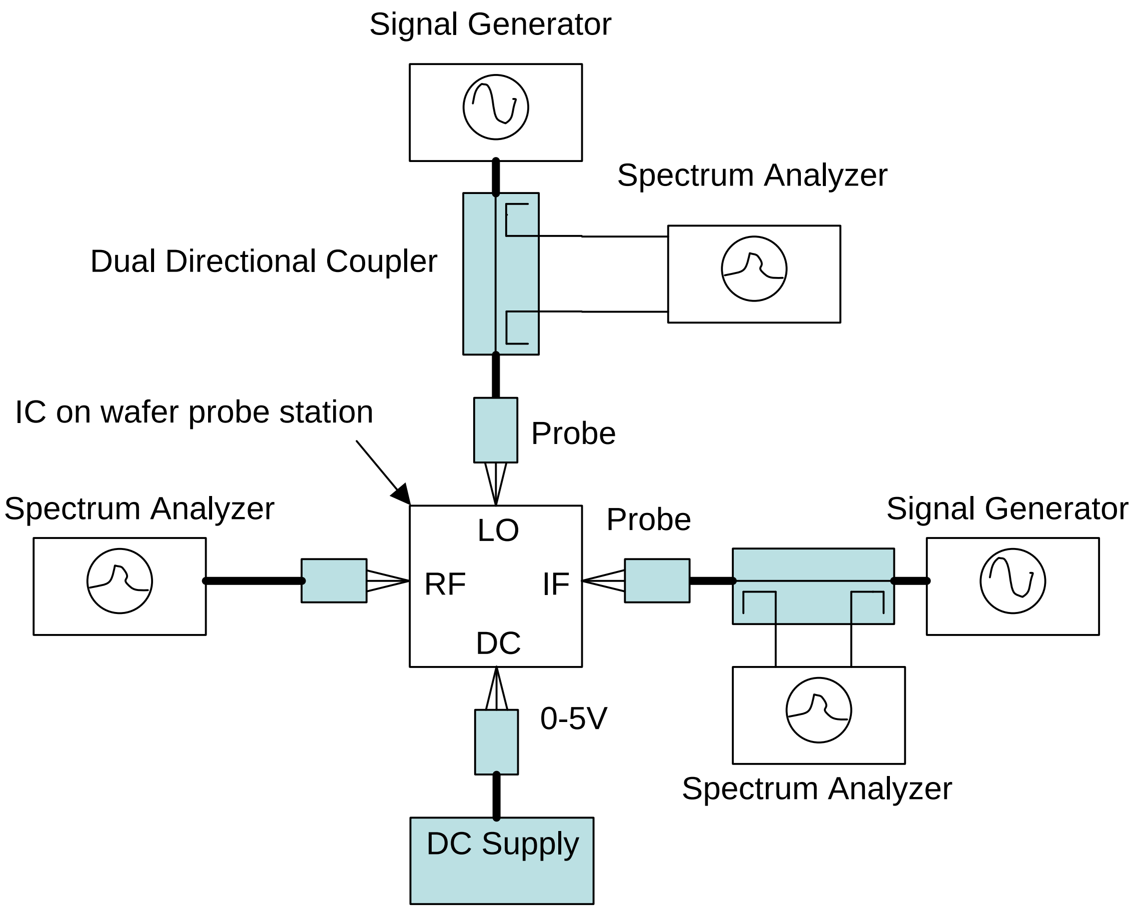

Figure 13: Test Setup for Upconverter Operation

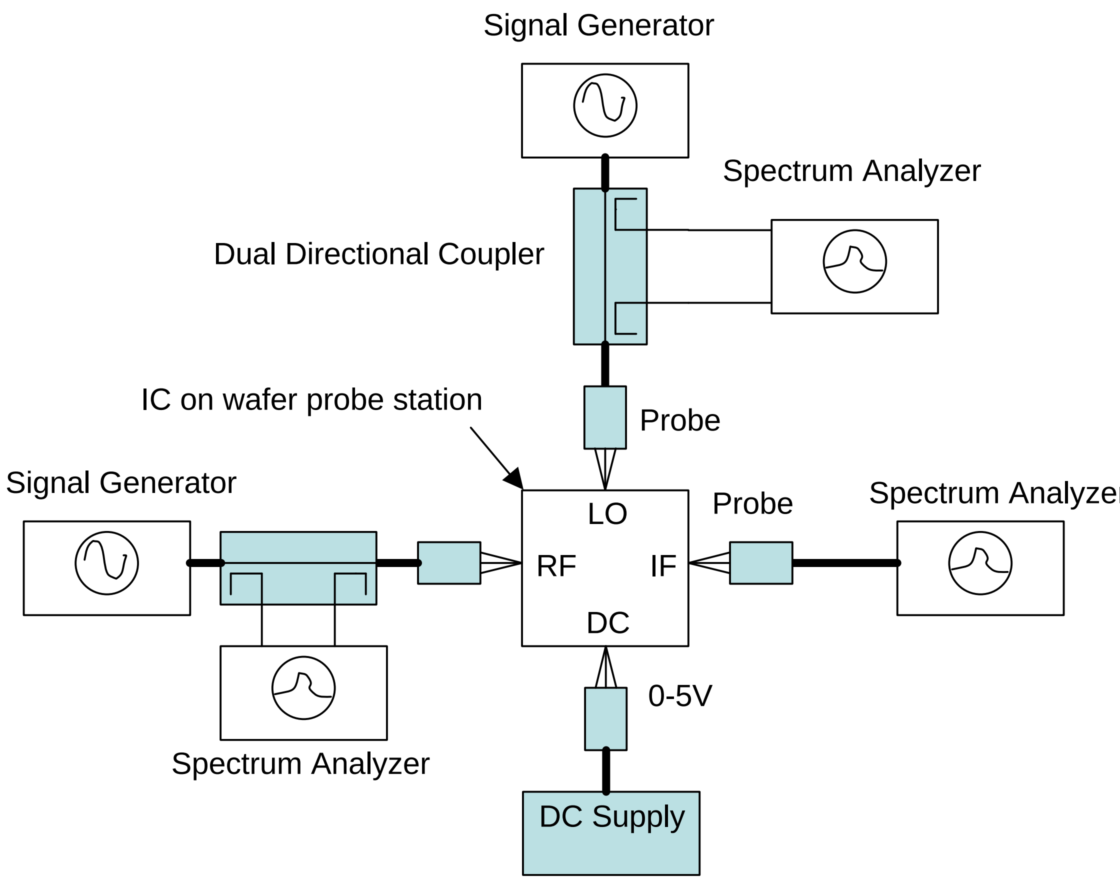

Figure 14: Test Setup for Downconverter Operation

Conclusions and Recommendations

Even though the MMIC was designed to operate without any necessary external components, the user should take the following precaution. A DC bias at the RF or LO port will not affect the performance of the mixer; however, the RF and LO ports are effectively shorted together at DC. Therefore, a DC blocking capacitor should be used if the user's LO and/or RF circuitry would present a DC bias to either port.

If desired, the IF VSWR can be reduced to below 1.5: 1 with the addition of a 43nH inductor in series with the IF port. The conversion loss will also drop by 0.2dB. Any value up to 43nH will improve the VSWR.

In the design of the mixer, prior to incorporating the DC bias a conversion loss less than 7dB was easy to achieve with an LO level of 7dBm. However, the conversion loss specification with DC bias and an LO level of 0dBm was met with little margin to spare. The DC analysis revealed that the diodes are not fully turned on with a 1.29mA bias. However, increasing the current by reducing the value of DC bias resistors lowers the impedance at the diode ports and results in greater conversion loss. This effect can be compensated by the insertion of series RF chokes, IC real estate permitting. A second attempt at this design should investigate this approach, making sure to maintain a symmetrical design to preserve a balanced circuit to ensure high isolation. In other words, the resistance and inductance in the bias path should be divided equally on either side of the diodes, as with the current design.

Finally, a layout oversight resulted in the omission of a 0.75pF tuning capacitor at the RF port. The inclusion of this capacitor lowers the RF VSWR to below 1.6: 1 and reduces the conversion loss by 0.5dB.

7. Bibliography

1. Vendelin et al, *Microwave Circuit Design: Using Linear and Nonlinear Techniques*, John Wiley & Sons, New York, 1990, pp. 536-552.

2. Stephen A. Maas, *Nonlinear Microwave Circuits*, IEEE Press, New York, 1997, p. 273.